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Analysis of GaN Series Capacitor Buck converter in point-of-load aerospace applications

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***Abstract*—Recently, atmospheric research has been increasingly conducted by both industry and universities by means of small spacecrafts, such as CubeSats, which offer an affordable cost due to the availability of the satellite inner components. Nowadays, nanosatellites include a huge variety of subsystems which require a substantial amount of computing power. Including such energy taxing components is a challenge on its own. In order to meet reasonable battery discharge rates, power converters for these devices have to meet requirements for both efficiency and reliability. In this research, a modified Series Capacitor Buck converter, that provides substantial benefits over traditional topologies, is proposed for point-of-load applications. This novel topology offers increased reliability for power systems feeding FPGAs and microprocessors inside spacecrafts. Simulation results validate the advantages of the proposed topology.**

***Index Terms*—Aerospace, Spacecraft, Nanosatellite, CubeSat, GaN, Series Capacitor, DC-DC converter.**

I. Introduction

Nanosatellites are an affordable standardised means of space exploration for universities and small private agencies [1]. They are built to a dimension constraint of 10 x 10 x 10 cm, which form a cell of one cubic unit, 1 U. They could be stacked, though, forming arrangements of 2 U, 3 U, etc. There is also a weight limit of 1.33 kg per cubic unit [1]–[3].

On the one hand, CubeSats include a number of different subsystems, such as an on-board computer, communications devices, command and data handling units, electrical power system, etc. As they are built with commercially available components, costs are kept reasonably low, but at the expense of poor reliability. On the other hand, there are a series of subsystems that should not fail in a satellite in order to succeed in their mission, like the Electrical Power Subsystem (EPS) [4], which acts as the power source of all the rest of subsystems and payload. However, they account as the most common sources of mission failure during the first 90 days of flight [5]–[7].

In this sense, the main source of energy in these satellites is obtained from solar panels and typically a pack of lithium-ion batteries, allowing the operation of the device during eclipses. The system is composed of a variety of DC-DC converters (Figure 1) for extracting power and generating the required payload voltages and currents. Moreover, there is an increasing demand of computer power for different tasks, for instance redundancy operation control, imaging or other research equipment. Very often they involve FPGAs and high performance microprocessors, demanding a fair amount of power. Increasing the efficiency in the feeding converters, battery charge and overall reliability can be maximised. In addition, less power losses involve less heat dissipation, which is difficult to manage in the vacuum of space.

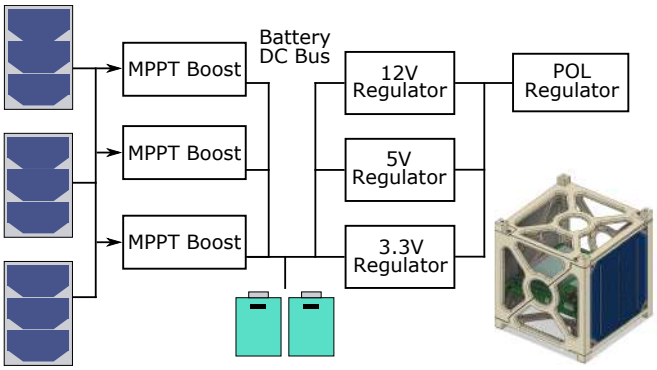


Figure 1: Typical EPS arquitecture of a CubeSat.

Point-of-load applications, like this, require fast transient response, precise regulation and low output ripple. In this sense, one of the most common among traditional topologies, is the conventional Buck converter (Figure 2), which allows for good regulation and efficiency [8]. However, obtaining very low output voltages imposes a lot of stress in power switches and overall efficiency in higher frequencies decreases. One solution is to use a tapped buck topology, but it also presents some disadvantages, such as voltage spikes, which require additional components [9].

In this paper, an alternative DC-DC topology to traditional multiphase Buck converters is used in order to address these issues and with its own set of advantages (Figure 3). It is called Series Capacitor Buck converter [10] or double step-down two-phase Buck converter [11]. The advantages of this topology have been validated in many POL applications and can be summarized as follows:

- For a given output voltage reference, duty cycle (D) is doubled compared to a conventional Buck converter, as the output changes with $D \cdot V_g/2$ (Figure 3). Thus, the performance of the converter under high step down operation is improved.
- Switching losses are reduced by a factor of two, as the voltage applied to the terminals of the semiconductors is also half the input voltage.
- The current in both phases of the converter is automatically balanced whereas interleaved Buck converters require additional control and sensors.

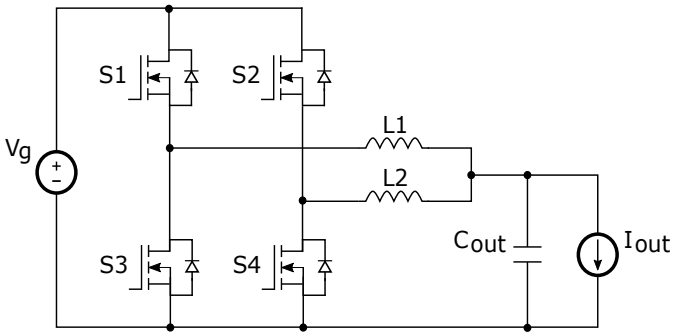


Figure 2: Buck 2-phase Topology.

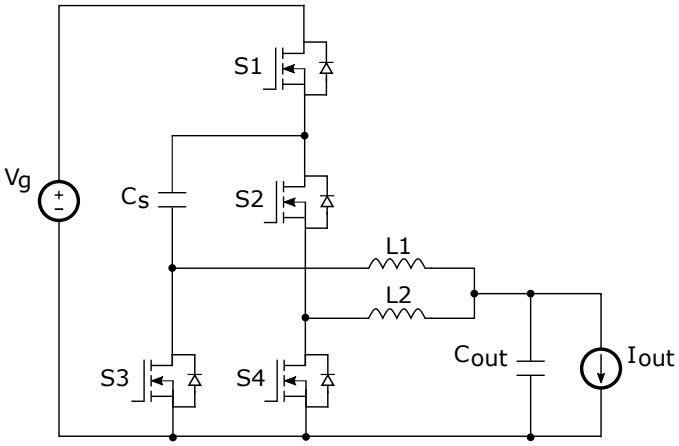


Figure 3: Series Capacitor Buck converter.

The Series Capacitor Buck (Figure 3) is built similarly to a conventional two phase Buck converter. It consists of two half bridge branches and an LC filter in the output, and it also introduces a series capacitor between the two switches of the first branch. This capacitor effectively divides the input voltage by two, making all the switches of the converter operate with a drain-source voltage of $V_g/2$. Thanks to this, the inductor current and switching losses are reduced, the duty ratio is doubled and the automatic balance of phase currents is achieved.

In this paper, the operation of both topologies is described and their respective advantages are compared. In addition, a modified version of the Series Capacitor Buck is proposed, achieving less conduction losses and improving heat distribution in power switches. These results have been validated by the development of simulation models for all of the topologies discussed in this paper.

II. Buck Converters Comparison

A. Converter operation and duty ratio doubling

The Series Capacitor works in the same way as a conventional buck. In the case of the latter, the output voltage varies proportionally to the duty cycle (D).

$$V_{out}(Buck) = D \cdot V_g \tag{1}$$

However, in the Series Capacitor, as soon as the intermediate capacitor reaches balance around $V_g/2$, conversion ratio is dictated by this voltage level.

$$V_{out}(Series\ Capacitor) = D \cdot \frac{V_g}{2} \tag{2}$$

In applications where extreme step down reduction is required, this is remarkably beneficial, as the duty cycle is doubled (Figure 4), and switching signals do not have to be that precise to maintain regulation. In the same manner, this limits the maximum theoretical output voltage to $V_g/4$ (figure 4) as the duty cycle is constraint to 50 %. Duty cycles above 50 % will cause unbalance on inductor currents, as it will be explained in section II-B.

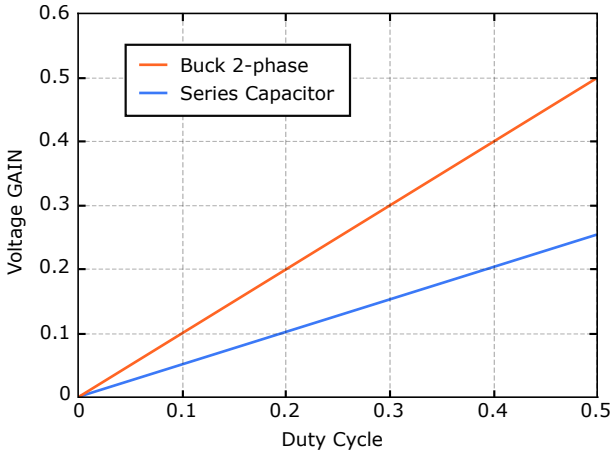


Figure 4: Theoretical voltage conversion ratio of compared converters.

B. Automatic inductor current balance

Accurate current sensing and phase balancing are a difficult challenge and require additional control resources [12]. Thus, the automatic inductor current balance is an important benefit of this topology.

Current balancing is achieved because the series capacitor average voltage in steady-state, is constant. This provides an inherent mechanism that ensures inductor current balance. If the inductor currents are not equal, the series capacitor voltage varies and charge balance is not maintained. The inductor currents eventually reach a level where they are both equal and the capacitor voltage is constant.

This also works in the case that inductance values of both phases are not the same. This is due to the fact that the charge given to or removed from the series capacitor does not vary with inductance (Figure 5). Inductance mismatch changes the peak-to-peak ripple current, but the area under the curve is still the same [12].

C. Inductor Current ripple

Reduction in inductor current ripple is one of the key benefits of this topology, as it is directly related with core losses and high frequency resistive losses in inductors. Thus, small reductions in inductor current ripple have considerable effects in core losses [10]. For a Buck converter, inductor current ripple is given by:

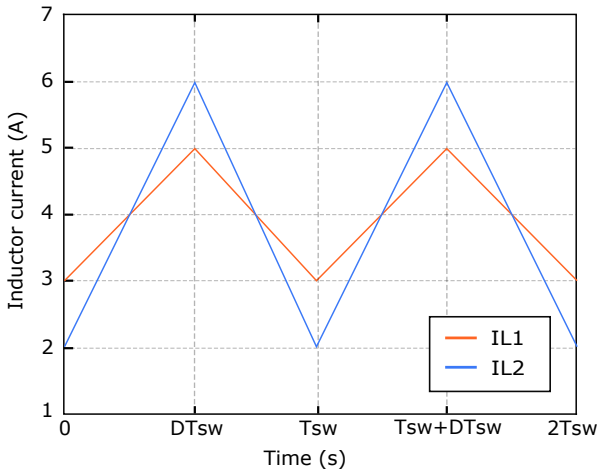


Figure 5: Inductor average current does not depend on inductance value, as the slope decreases with it.

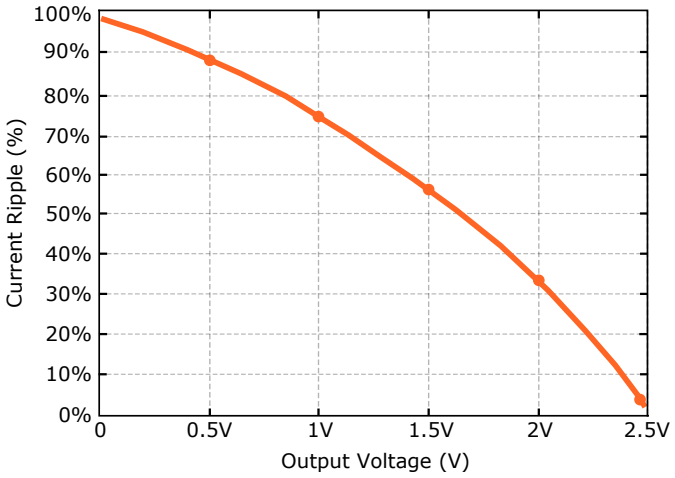


Figure 6: Output voltage ripple compared to Buck 2-phase with $V_g = 12\ V$.

$$\Delta I_L(Buck) = \frac{(V_g - V_{out}) \cdot D \cdot T_{sw}}{2L} \tag{3}$$

Whereas in the Series Capacitor, inductor current ripple equation is the same but the effect of the intermediate capacitor voltage has to be taken into account:

$$\Delta I_L(Series\ Capacitor) = \frac{(V_g - V_{CS} - V_{out}) \cdot D \cdot T_{sw}}{2L} \tag{4}$$

Since Series Capacitor charge to $V_g/2$, 4 is rewritten as:

$$\Delta I_L(Series\ Capacitor) = \frac{(\frac{V_g}{2} - V_{out}) \cdot D \cdot T_{sw}}{2L} \tag{5}$$

Depending on the output voltage, the Series Capacitor buck converter will have more or less output current ripple (Figure 6).

D. Output Current ripple

Since FPGAs and microprocessors require tight regulation in both voltage and current, the resulting output current ripple must be considered. The value of this term is given by the amplitude of the inductor current ripple and the output voltage. It is important for this application to choose inductance values that maximize the duty cycle in which the converter will work, and maintain, at the same time, moderate values of current ripple (Figure 6).

Output current ripple has also an effect in the resulting output voltage ripple. High values of ESR in the smoothing capacitor aggravate this problem.

E. Voltage waveforms

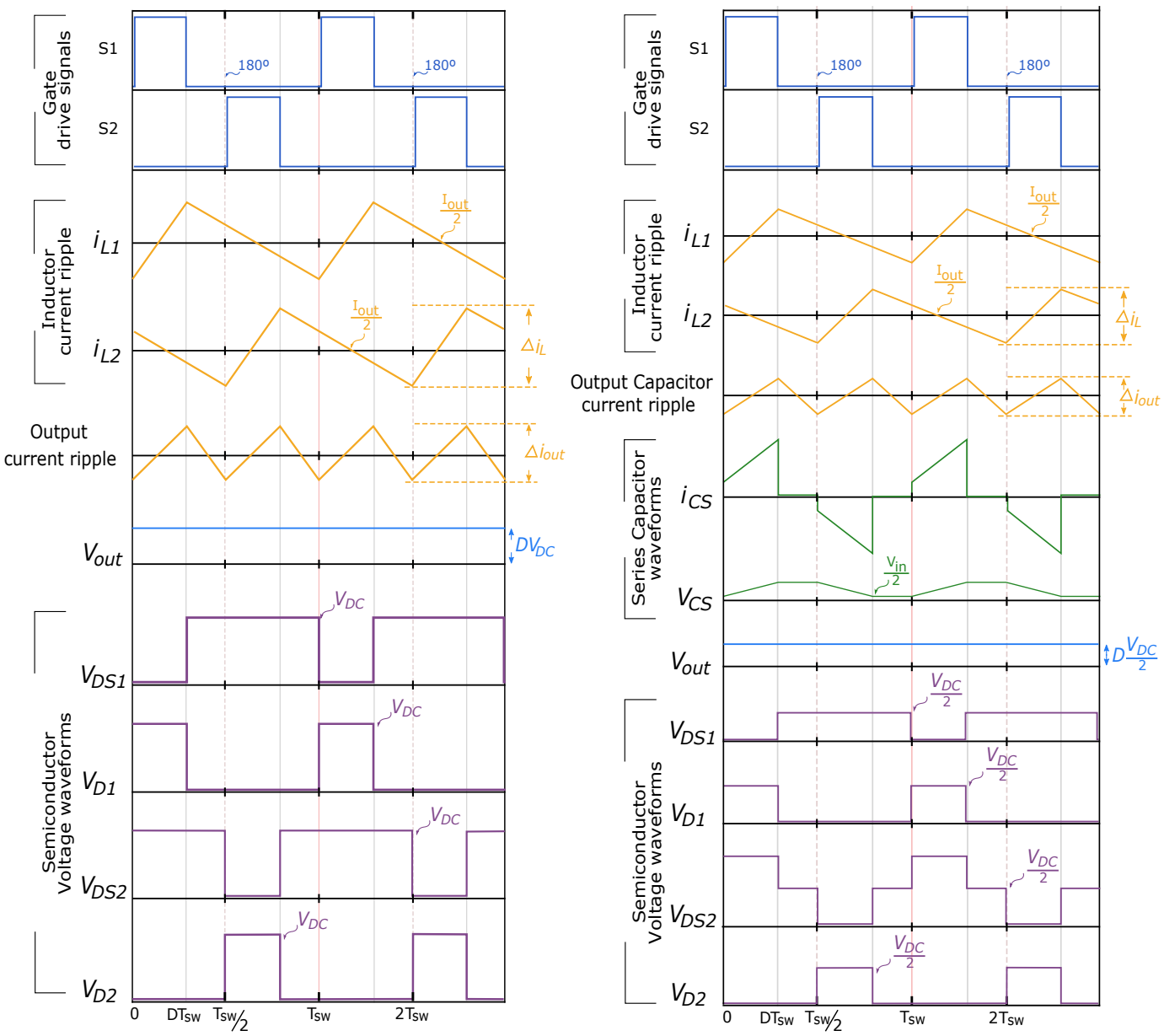
There is a difference in the switching voltage waveforms between the conventional Buck (Figure 7(a)) and the Series Capacitor configuration (Figure 7(b)). This is beacause in the Series Capacitor Buck, the intermediate capacitor makes all the power devices switch between $V_g/2$ and zero. Except Q2, which also has to withstand full V_g during part of the switching period.

III. Gallium Nitride consideration

During the last decade, some alternatives to traditional silicon semiconductor devices have arisen, promoting benefits in many fields of both industry and research. Wide-bandgap devices have started to be readily available recently, since the production processes are not mature and require exceptional efforts [13]–[15]. Gallium Nitride (GaN) and Silicon Carbide (SiC) have been the most popular technologies to replace silicon inside the power electronics industry, specially in low and medium voltage applications. However, upfront costs are delaying a massive adoption of these devices. Whereas the cost is higher compared with silicon devices of the same voltage and current ratings, it is possible to compensate higher costs with increased energy efficiency and robustness. In the same manner, GaN technology enables switching frequencies in power applications allowing better integration and overall efficiency. Although this is a desirable feature, removing heat from these devices is a challenge, and alternatives to traditional heatsinks have to be considered [16], [17].

Drawbacks such as increased costs and difficult integration have a considerable influence on engineers and designers not choosing wide-bandgap devices for new products or industral developments. However, this is not the case for aerospace or military applications, where meeting technical specifications and requirements is mandatory, regardless of overall cost and challenging development.

These applications, where dimension and energy constraints limit the capabilites of the mission, can substantially benefit from little improvements in efficiency of the different subsystems and many researchers have been evaluating GaN power switches in these environments [18]–[20]. For all these reasons, this research has conducted an implementation of an EPC2055 HEMT as the switching device for the proposed converter by means of simulation models that accounts for conduction and switching losses.



(a) Buck 2-phase waveforms

(b) Series Capacitor Buck waveforms

Figure 7: Operating waveforms of compared converters.

IV. Power Losses Analysis

A. Switching losses

Switching losses are one of the main drawbacks of the traditional Buck. The Series Capacitor Buck has a great advantage in this regard, and benefits significantly from higher switching frequencies [10], [11].

The benefit of a lower V_{DS} is that switching losses are reduced in a significant amount, since losses depend linearly on frequency and voltage. The intermediate capacitor maintains a DC voltage of half the input voltage across it, and, thus, semiconductors switching voltage is reduced by half compared to a conventional buck converter:

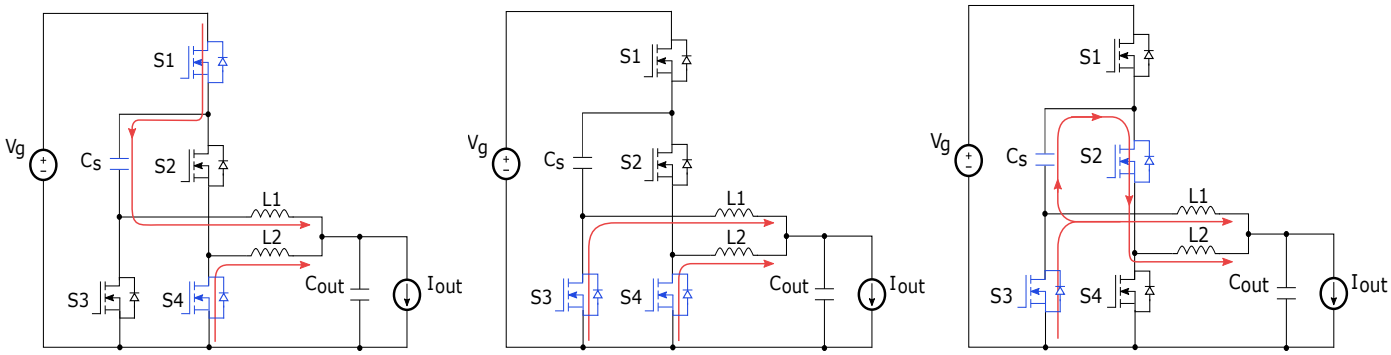
$$P_{sw}(Buck) = \frac{1}{2} \cdot V_{DC} \cdot I_{out} \cdot (t_r + t_f) \cdot f_{sw} \qquad (6)$$

$$P_{sw}(Series\ Capacitor) = \frac{1}{4} \cdot V_{DC} \cdot I_{out} \cdot (t_r + t_f) \cdot f_{sw} \quad (7)$$

This effect appears in all the switches during both turn-on and turn-off transitions, even though S2 has to block the whole V_g input, when S1 is *on*, S2 only has to switch between that and $V_g/2$ of the intermediate capacitor. As opposed to this, in the traditional Buck converter, all the semiconductors have to switch between the input voltage and ground.

B. Conduction losses

Conduction losses have a considerable effect in the global efficiency of the Series Capacitor Buck since resistive losses have an important effect in this topology, (Figure 8) specially since for a portion of the switching interval, S3 have to carry the full load current (Figure 8(c)).



(a) Stage 1 (b) Stages 2 and 4 (c) Stage 3

Figure 8: Operation stages in Series Capacitor Buck.

This causes severe power losses in this device, that are of much higher magnitude than for the rest of the switching semiconductors. A solution for this issue is described in Section IV-C to improve reliability. The ESR of the intermediate capacitor is something to be taken into account, as well.

C. Conduction losses optimization

The Series Capacitor Buck offers improvements in regulation and power losses over traditional multi-phase Buck topologies. However, as it has been explained in IV-B, power dissipation in S3 is considerably higher than in the other switches. Hence, a significant temperature mismatch between S3 switch and the rest is expected. This is an important topic to address since it is a potential source of malfunction in the converter. For this reason, in this paper, a second switch has been added in parallel with S3 (Figure 9) to reduce power losses up to a 50 % in this device, which helps keeping power losses under similar values as the rest of the switches in the converter (Figure 10(b)).

Paralleling devices is a challenging task, since there is a variety of concerns to take care of, i.e. providing good load sharing that guarantees balanced junction temperature distribution in all devices. In this regard, new GaN technology offers promising results at higher switching frequencies, as a thermal runaway is less likely to happen in paralleling applications [21], [22].

Adding an extra switching device slightly increases overall costs of the power converter, but the benefits obtained are considerable, as it remarkably helps reducing power consumption (Figure 11) and, thus, increasing battery charge during eclipses. Furthermore, a better temperature distribution is achieved in the converter, which reduces failure rates of EPS modules.

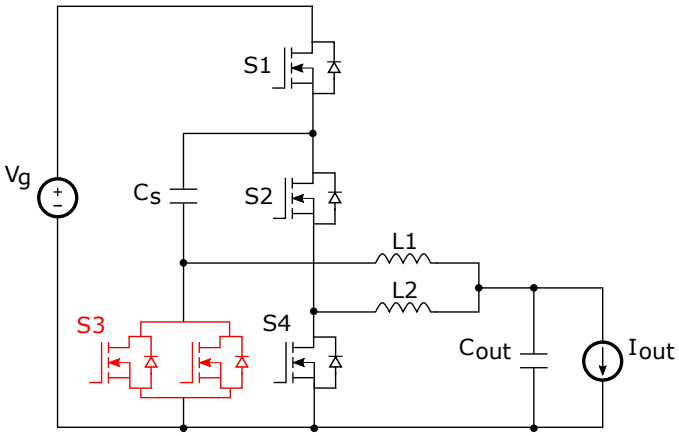


Figure 9: Modified Series Capacitor for increased reliability.

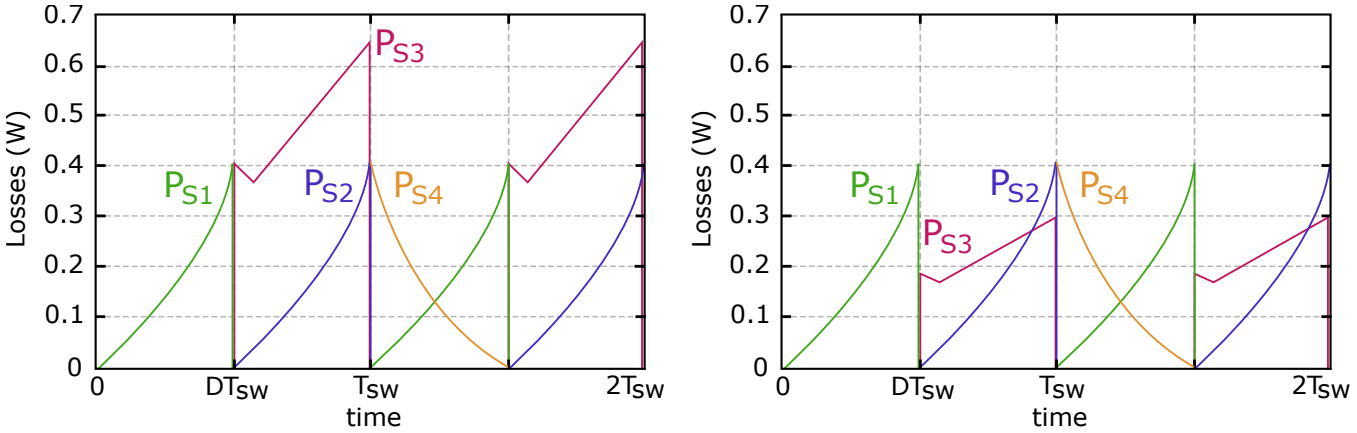
V. Conclusion

This paper has presented a comparison between the traditional two-phase Buck converter and the Series Capacitor Buck, in terms of power losses, current balancing and regulation. These are the main concerns in point-of-load applications inside spacecrafts, in a trade off between performance and efficiency.

The main benefits of the Series Capacitor Buck in this environment include a great reduction in switching losses, due to the lower value of V_{DS} imposed by the intermediate capacitor. This also leads to lower voltage grade semiconductors and enables for higher switching frequencies.

In addition, lower inductor ripple current can be achieved depending on the conversion ratio, phase currents are automatically balanced and the duty ratio is doubled. This offers better control of the output voltage and current regulation, as it makes the converter less sensitive to changes.

The main disadvantage involves conduction losses which account for the biggest source of power losses in this topology. Moreover, one of the power switches dissipates 50 % more power than the rest of semiconductors, which could potentially become a source of malfunction of the satellite EPS. In this sense, a modification of the Series Capacitor that addresses this problem has been proposed, which consists in the addition of another switch in parallel, reducing this effect by half and improving robustness and overall efficiency, which will maximize battery charge and success possibilities in a real mission. Simulation results have validated the proposed topology.



(a) Original power losses in Series Capacitor Buck at 50 % duty cycle.

(b) Power losses in Series Capacitor Buck with parallel S3 at 50 % duty cycle.

Figure 10: Semiconductor power losses difference with V_g= 12 V, V_{out}= 2.5 V, I_{out}= 12 A, f_{sw}= 1 MHz.

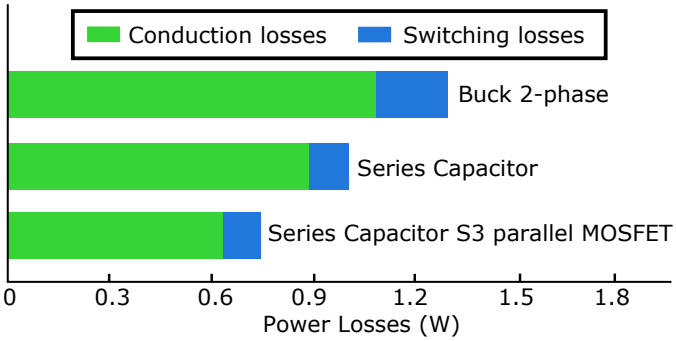


Figure 11: Power losses distribution in the different topologies with V_g= 12 V, V_{out}= 2.5 V, I_{out}= 12 A, f_{sw}= 1 MHz.

VI. Acknowledgement

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