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MASTER`S DEGREE IN

INTEGRATION OF RENEWABLE ENERGIES INTO THE ELECTRICAL POWER SYSTEM

MASTER'S THESIS

MODELLING OF RESISTIVE TYPE SUPERCONDUCTING FAULT CURRENT LIMITER FOR MULTI-TERMINAL HVDC SYSTEMS

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SUMMARY

The growth of electrical energy demand along with the CO_2 reduction requirements enhance the demand of new electrical energy generation and transmission systems. In the last decades renewable energy generation systems have rise considerably to face this challenge, especially wind energy and, lately, offshore win energy systems.

High Voltage Direct Current (HVDC) transmission systems are very suitable to integrate bast renewable energy generation into the main AC grid, as they are especially appropriate for long distance and undergrown / underwater transmission systems. However, one of the main disadvantages of these transmission systems are the lack of commercially available direct current circuit breakers for fault clearings since there is not naturally current zero crossing and the rise rate and final value of the current is very high under fault conditions.

The integration of current limiters, especially superconducting resistive type current limiters, into these transmission systems are seen as a promising solution to cope with the fault current clearing phenomena. Thus, this project is oriented to the modelling of this device, superconducting resistive type current limiter, and the simulation of this device in a real HVDC multiterminal grid.

RESUMEN

El aumento de la demanda de energía eléctrica junto con el requerimiento de reducción de emisiones de CO_2 generan la necesidad de nuevas tecnologías de generación y transporte de electricidad. A lo largo de las últimas décadas las energías renovables han tomado un papel importante para enfrentarse a este reto, especialmente la energía eólica, y últimamente la energía eólica offshore.

Los sistemas de transmission de alta tension en corriente continua son muy apropiados para integrar grandes cantidades de energía eléctrica al sistema electrico de potencia, ya que son muy aptos para transmisión a larga distancia y transmisión subterránea y submarina. Si embargo uno de los principales inconvenientes es la falta de interruptores automáticos para corriente directa, ya que en estas aplicaciones no hay paso natural por cero y la corriente alcanza valores muy elevados muy rápidamente en condiciones de falta

La integración de limitadores de corriente, especialmente los de tecnología superconductora resistiva, son considerados como una solución prometedora a este problema. Este proyecto esta orientado al modelado de limitadores de corriente de tecnología superconductora resistiva y la simulación de una red HVDC multiterminal con este dispositivo.

1. INTRODUCTION

Implementation of multiterminal high voltage direct current (MTDC) is seen as a key solution for the electrical energy demand increase and for integrating large scale renewable energies. Nevertheless, high voltage direct current (HVDC) technology is not mature enough to enable wide existence of this grids, and up to date most of the HVDC transmission systems are two-points lines.

One of the most challenging aspects of this technology is the fault clearing since DC currents have no zero crossing. One way to open the faulted circuit is to trigger the AC side breakers, however, this may lead to the full de-energization of the line or grid, making these systems unreliable, especially if overhead lines are desired.

Direct current circuit breakers are still under development, and they cannot withstand high current breaking capabilities, furthermore, due to the high rate of rise of the current, these devices must operate within few milliseconds, while in AC operate in several milliseconds.

Considering this, fault current limiters, limiting both rise rate and peak value, are of concern in this transmission systems. Several researchers have claimed the resistive superconducting fault current limiter as a promising solution for this technical limitation.

1.1 BACKGROUNG

Power systems should provide reliable electrical energy generated by different technologies to different load types. Power systems are complex grids exposed to several types of faults, some of them transient and some others permanent. Most common fault types are short-circuiting, which are the non-desirable connection between to terminals at different potentials, which may result in high currents. Short circuit current is defined by the short circuit power and the voltage level of the system. A high S_{SC} means a strong grid in terms of power quality, but it leads to high I_{SC} values [1].

$$S_{SC} = \frac{U_{AC}^2}{Z_{TH}}$$

Equation 1

$$I_{SC} = \frac{S_{SC}}{\sqrt{3}U_{AC}}$$

Equation 2

Fault currents are feed by the followings [2]: 1) Synchronous generators connected to neighbour buses (especially permanent current), 2) Large induction motors (especially transient), and 3) distributed generation (DG).

In the last years, the distribution grid has experimented a huge increase in DG, especially from wind farms, leading to the increment of the system I_{SC}. The contribution of I_{SC} of the DG depends on the technology, for instance, a PV panel connected via inverter can saturate the output power to 2 times the nominal current, whilst a windmill based on DFIG (converter on the rotor side) may reach 6 times the nominal current. The main negative effects of short circuits are the followings:

- Power interruption
- Damped mechanical oscillations on the electrical machine's shaft

- Negative rotational inertia and stress on the damping windings of the synchronous machines
- Increase in reactive power demand in the line impedance and leakage impedance of transformers
- Voltage drop in buses with sensitive loads
- Torque reduction in induction machines and increased demand in reactive power
- Thermal stress on equipment
- Voltage swell in faulted buses and sag in un-faulted buses
- Electromagnetic interference
- Increased unsupplied energy and economic losses
- Corrosion in the connection area
- Reduction in power system reliability
- Mechanical stress on the structures
- Etc…

Consequently, there is a need to limit the I_{SC} if no oversizing of the tolerable fault current (TFC) of the elements of the systems is desired. This can be achieved by network level strategies or device level strategies [3]. According to device level strategies, the use of fault current limiters (FCL) is a good technique to reduce I_{SC}.

Fault current limiters are widely used in AC systems. However, its application in HVDC systems is promising, considering the HVDC system inherent response to faults.

1.1.1 Fault Current Limiters

FCL are devices with virtually zero impedance during the normal operation of the system, but when fault occurs, the impedance of the devices increases to the set value. The requirements for being a good FCL are the following [4]:

- It should have low impedance during normal operation
- It should limit the fault current withing a short period of time
- It should take a short time to recover
- The FCL should limit the current in case of device fail
- In some applications (for instance, offshore applications), it should be compact and light
- It should be easily scalable to high voltage applications

There are several types of FCL, but they can be classified in four groups:

1. Solid-State Fault Current Limiters (SSFCL)
2. Superconducting Fault Current Limiters (SFCL)
3. Hybrid Fault Current Limiters (HFCL)
4. Other technologies

The integration of FCL in a power system brings the following advantages [2]:

- The power system equipment in general can be designed with lower TFC
- The is no need for replacing the current limiting devices (not applicable for fuses)
- In steady state conditions FCL does not imply voltage drop nor harmonic injection
- Low power losses during normal operation
- Transient stability is improved

- Reduction on thermal stress
- Fast voltage reduction is avoided, voltage stability improved
- Fault ride through of loads and generators is improved
- Allows high level of network interconnection
- Favours DG integration
- Etc…

Withing all the FCL types, SFCL are the most used technology and specially the resistive type ones, as depicted in Figure 1.

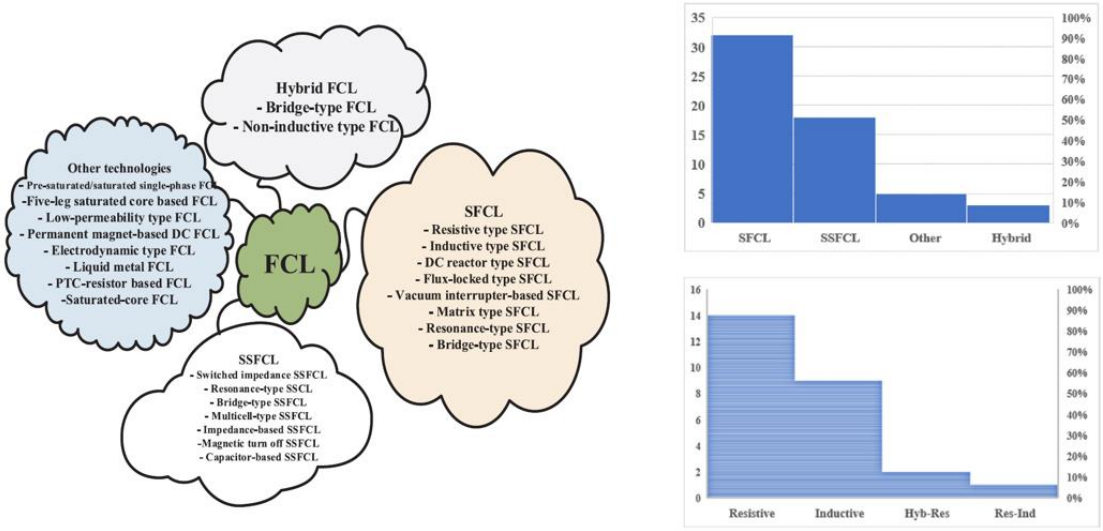

Figure 1 FCL Types and number of installed devices in real power systems [2]

Figure 2 shows a comparison between the technical characteristics of the different types of FCL technologies.

Parameters/FCL	SFCL	SSFCL	HFCL	Other
Operating voltage	220 V–510 kV AC, 500 kV DC	150 V–500 kV AC	15 kV AC	380 V–110 kV AC
Rated current	a few amperes to 10kA	a few amperes to 3kA	2kA	a few amperes to 2kA
Material technology	superconductor	semiconductor	superconductor and semiconductor	Low-impedance reactor
Time response	2.5 ms–10 ms	1 μs to a few ms	less than 1 ms to 2 ms	Less than 2 ms
Percent of transient overvoltage	0.6%-2.3% (A4)	about 2% (A3)	about 10% (A2)	2.5%-20.5% (A1)
weight	3–36 tones	a few kg- a few tones	from one to a few tones	from a few kg to one tone
Physical dimensions	The largest	The smallest	fairly large	large
Cooling system	high power ratings, voluminous, liquid nitrogen	heatsink, air ballast	heatsink, air ballast, liquid nitrogen	air ballast, natural
cost	the most expensive	the cheapest	fairly expensive	expensive
Manufacturing as a compact pack	No	Yes	No	No
Modular	No	Yes	No	No
Reliability	the most reliable	has the lowest reliability	reliable	fairly reliable
Harmonic generation	very low	very high	high	low
Loss	very low	low	high	very high
Voltage drop	very low	high	low	very high
No-load loss	very high	very low	low	high
Needs to maintenance	high	low	very high	very low

Figure 2 Technical comparison between FCL technologies

The main advantages of the SFCL are the applicability to high voltage and currents, reliability, low harmonics, losses, and voltage drop. These characteristics make them appropriate for high voltage and power systems, such as HVDC.

1.1.2 HVDC development

The increase of electrical energy demand after the second world war stimulated the research in high voltage direct current (HVDC) transmission systems, especially in Sweden and the

former Soviet Union. HVDC lines have been used for more than 60 years and offers advantages against conventional HVAC transmission systems depending on the applications and casuistry. The first commercial HVDC was built between the island of Gotland and Swedish mainland and was a 98km submarine cable with ground return, however, the first experimental HVDC line was built between Moscow and Kasira in 1950 and was a 116km length transmission line at 200kVdc [5].

The main reasons for using HVDC technology are the following ones:

1. An overhead DC line can be less costly per unit of length than an AC transmission system designed for transmitting the same amount of electrical power, furthermore, if very high voltages are achieved, the losses are decreased. However, DC converter stations are much more expensive, so there is a breakpoint at a determinate distance, as depicted in Figure 3. There are other environmental advantages as the electric and magnetic fields are in DC instead of AC.

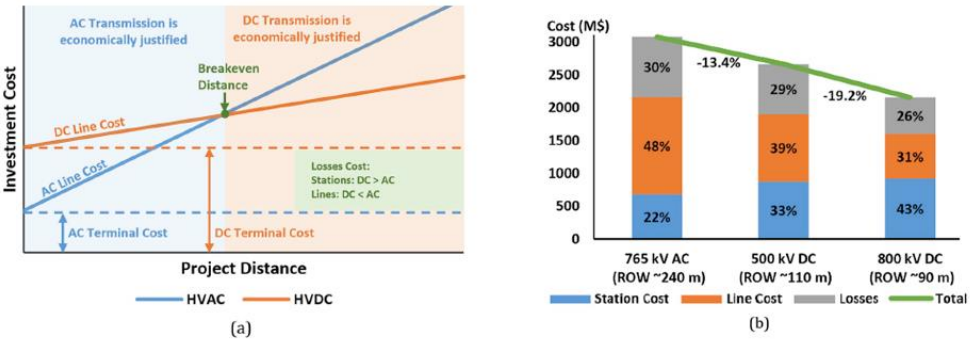

Figure 3 HVAC vs HVDC cost comparison: (a) economical breakpoint (b) Cost and ROW estimation for 6000MW transmission line of 2000km [6]

2. If transmission system is underground or submarine this breakpoint moves substantially to the left, which is usually at 50km. This is due to the huge increase of stray capacitance of underground or submarine cables. Thus, this technology can help in the integration of large offshore wind farms and the interconnection with oil and gas offshore platforms.

3. Some AC electrical systems are not synchronized even though they are physically close to each other, as occurs in Japan where half of the country's network is at 50Hz and the other is at 60Hz. By interconnecting these networks by a DC link, power flow can be achieved.

According to HVDC, two main technologies can be distinguished: Voltage source converters (VSC) and line commutated converters (LCC). The choice of converter technology depends on the casuistry and application. VSC technology is claimed to be the best technology for implementing multiterminal HVDC grids due to the following advantages [7]:

- Independent and fast active and reactive power control
- Absence of harmonic filters
- Suppression of commutation failure
- Connection of passive AC loads
- Lower footprints

- Operation without telecommunication between terminals
- Capability of power reversal without voltage polarity reversal in DC side

1.2 OBJECTIVES OF MASTER'S THESIS

The first objective of this master thesis is to evaluate the state of the art of HVDC systems, its main technological basis, grid configurations, fault phenomena and the applied circuit breakers operation.

The second objective is to evaluate the different superconducting resistive type of current limiter's models.

Finally, the main objective of this master thesis is to evaluate the HVDC grid response when a current limiter is integrated under fault conditions.

2. HVDC SYSTEMS

Over the last few years, there has been a huge increase in the cumulative HVDC power capacity. Figure 4 [6] shows the evolution of the cumulative HVDC system power in world, it can be noticed that in the last 15 years the growth has been exponential, specially due to China's projects.

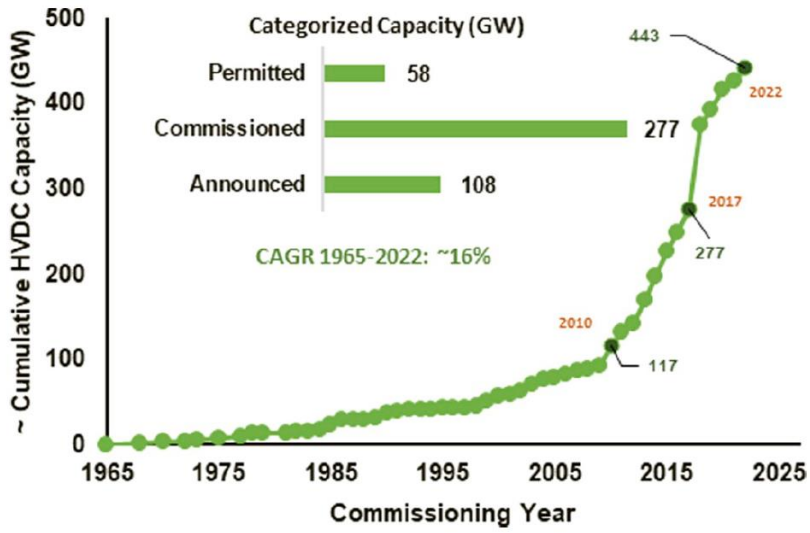

Figure 4 Evolution of cumulative HVDC capacity

HVDC system suppliers is dominated by ABB, Siemens, and Alstom Grid (whose energy business was absorbed by General Electric in 2015).

According to HVDC systems, converter stations can be technologically divided in two; current source converters (CSC) or line commutated converters (LCC), using thyristor-type valves, and voltage source converters (VSC), using IGBTs. Historically, HVDC systems has used LCC, but the improvement in the semiconductors devices (especially IGBTs) and the development of the digital signal processing techniques allowed the development of this kind of converters for these applications.

First VSC project was commissioned in Gotland (50MW +/-80kV), nowadays there are systems up to 900MW and with rated voltage up to 320kV, as can be shown in Table 1. ABB claim to have reached levels up to 525kVdc with its VSC technology [8], as in Zhangbei HVDC grid [9].

Projects	Year	Converter Type	Power Rating (MW)	Converter Losses (%)	DC Voltage (kV)	Supplier
Gotland	1997	Two-Level	50	3	±80	ABB
Eagle Pass	2000	Three-Level with PWM	36	2.2	±15,9	ABB
Estlink	2006	Two Level PWM	350	1.4	±150	ABB
Trans Bay Cable	2010	MMC	400	1	±200	Siemens
Nan'ao 3-terminal DC grid	2013	MMC	200/100/50	-	±160	Multiple
SW Link	2014	MMC	2x720	-	±300	Alstom Grid
Dolwin2	2014	MMC	900	-	±320	ABB

Table 1 HVDC projects evolution

Up to date, the largest commissioned line, based on LCC, is a 1100kVdc 12GW line of more than 3000km in China. It is a clear example of the usefulness of this technology as it is conceived to integrate the large amount of surplus renewable energy generation of the bast northwest of China into the more populated zones in east [10].

The selection of a LCC or VSC technology depends on the application and casuistry. Table 2 shows the attributes for each technology type [11]:

Function	LCC	VSC
Semi-Conductor Device	Thyristors, currently up to 8.5kV and 5000Amps. Not controlled turn off capability	IGBTs with anti-parallel freewheeling diode, with controlled turn-off capability. Current voltage rating 4.5 to 6kV and turn off current of 120Amps
DC Transmission Voltage	Up to +/- 800kV bipolar operation, 1000kV under consideration in China	Up to +/-320 kV to 400 kV
DC power	Currently in the range of 6000 MW per bipolar system	Currently in the range of 600 to 1000 MW per pole
Reactive Power Requirements	Consumes reactive power up to 60% of its ratings	Reactive power controllability
Filtering	Requires large filter banks	Requires moderate size filter banks or no filters at all
Black start	Limited applications	Capable of black start and feeding passive loads
Commutation failure performance	Fails commutation for ac disturbance	Does not fail commutation
Overload capability	Available if designed for up to any required design value	Does not have any overload capability
Applications with overhead lines		Can be applied but DC line faults are cleared by trip of AC breaker, or the use

	Can be applied and dc line faults can be cleared by converter control	of a dc circuit breaker. It has mostly been applied with cables
Small taps	Not economic and affects the performance	Economic and seems not affect the performance
Load rejection overvoltage	Large and must be mitigated because of the large reactive power support	Not large because of small size of filters if required
Footprint	Can be large	Small for the comparable rating to a LCC
Offshore wind farms	Can be applied with some dynamic voltage control	Straight forward application
Power Losses	Typically, 0.8% per converter station rated power	Typically, 0.8 to 1% per terminal with multilevel converters

Table 2 Comparison between LCC and VSC technology

2.1 Converter technology

This chapter will summarise the main differences between LCC and VSC converter stations.

2.1.1 Line Commutated Converters

Figure 5 shows the basic elements for LCC technology [12]:

- AC filters: These filters minimize the main AC harmonics (passive resonant shunt filters) and compensate the reactive power
- Three winding Y/Y-D transformer: Provides galvanic isolation and generates 30 degrees shifted 3 phase systems needed for the 12-pulse converter operation
- 12 Pulse Converter: Rectifies AC to DC minimizing the harmonic generation
- DC filters: Composed by smoothing inductances and passive shunt filters
- Other components: Earthing electrodes, protection devices…

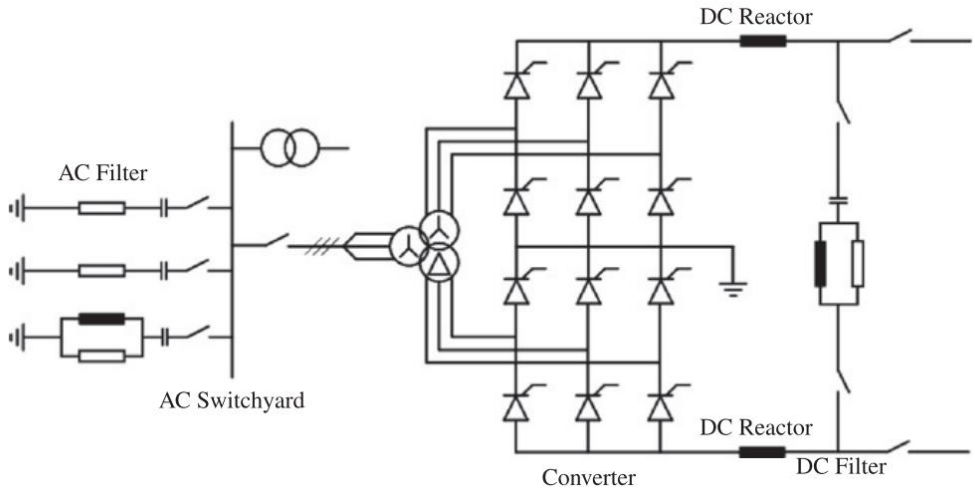

Figure 5 Schematic view of LCC-HVDC system

These systems are characterized by their robustness and high-power transmission capability. However, there is no controllability of the AC reactive power (it consumes) and the harmonic content is big, so there is the need for huge filters in AC and DC.

Furthermore, in LCC systems, a big short-circuit-ratio (SCR) is needed.

$$SCR = \frac{S_{SC}}{P_{DC_{HVDC}}}$$

Equation 3

$$S_{SC} = \frac{U_{AC}^2}{Z_{TH}}$$

Equation 4

This is due to the big amount of reactive power that is demanded by the converter and the effect of the SCR in the controllability of the DC link. The control of the HVDC link has an important impact on its interaction with de AC system.

The short circuit ratios can be classified as:

High	→	SCR > 5
Moderate	→	3 > SCR > 5
Low	→	SCR < 3
Very Low	→	SCR > 2

2.1.2 Voltage Source Converter

Figure 6 show the main components for VSC technology [12]:

- Transformer: Although it is not compulsory for the correct operation of the system, galvanic isolation is desired
- AC filter and phase reactor: Minimises the harmonic propagation through grid
- Converter: The trickiest component, rectifies AC signal by IGBTs commutating at high frequencies.
- DC capacitors: These capacitors are needed to stablish the voltage in the DC link.
- DC chopper: Its main function is to dissipate energy whenever is needed.

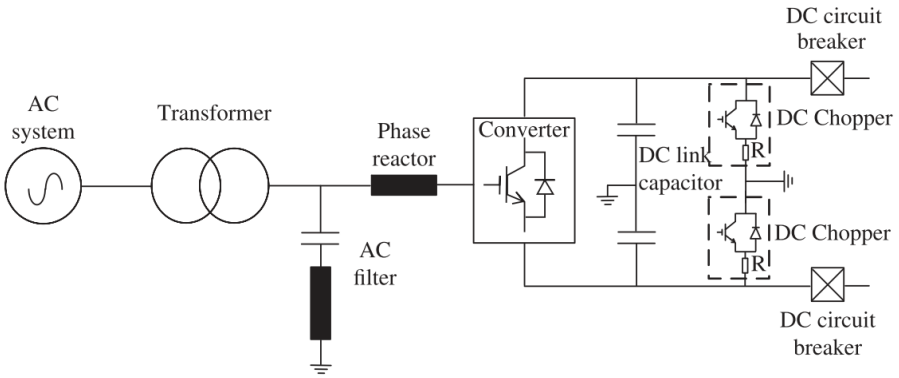

Figure 6 Main components of the VSC-HVDC system

The converter topology can vary; it can be two level converter, or multilevel converter. Two level converters are the less complex ones but generates high harmonic content and they have higher losses due to the need of high frequency commutation. Multilevel converters can be divided in neutral point clamped technology (NPC) or modular multilevel converters (MMC). According to NPC, theoretically they can have 3, 5, 7 and higher levels, but the complexity of

the converter increases drastically with the level increment, so for these applications only 3 level converters have been commissioned, as the shown in Figure 7.

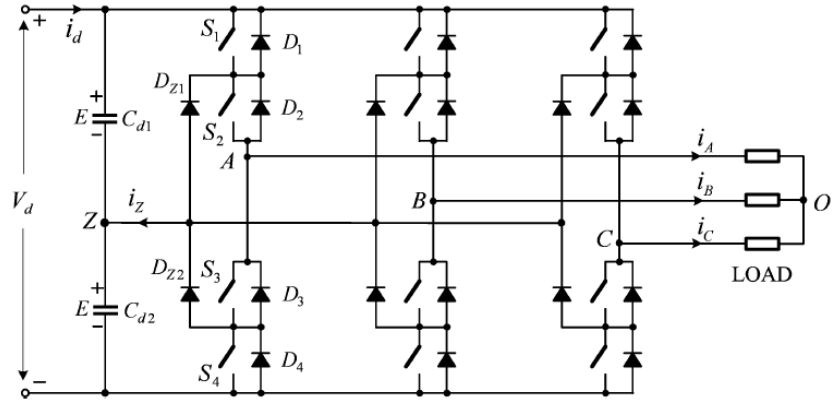

Figure 7 Conventional 3-Level neutral point clamped converter [13]

MMC converters may have much higher levels by serialising sub-modules (SM) as it is depicted in Figure 9 [14]. This SM can be made by different topologies, however, the most employed ones are half-bridge of full-bridge, as the ones showed in Figure 8.

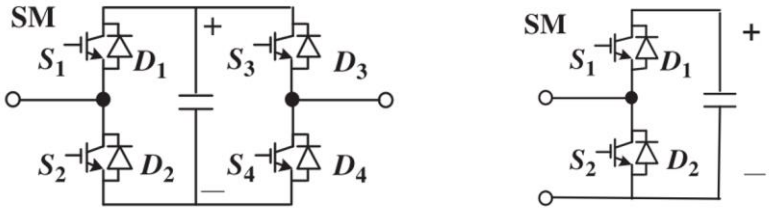

Figure 8 Most used SM topologies: Full-Bridge (Right), Half-Bridge (Left)

Half-bridge sub-module only offers two levels (Vdc o zero) while full-bridge topology offers three levels (Vdc, zero and -Vdc). This implies the main two following advantages:

- More Voltage levels with same SM number [13]
- AC infeed blocking capability [12] (as does the Alternate-Arm Converter, which is not treated in this document). This can be achieved by inserting an opposite voltage in AC side.

MMC converter topology offers more voltage levels (better harmonic content) with low commutation frequency at SM level (low losses and HF noise). Moreover, the smoothing reactance's in AC and DC limit the raising rate of current in case of fault. However, the complexity relapses in the individual control required for the SM and the number of independent capacitors.

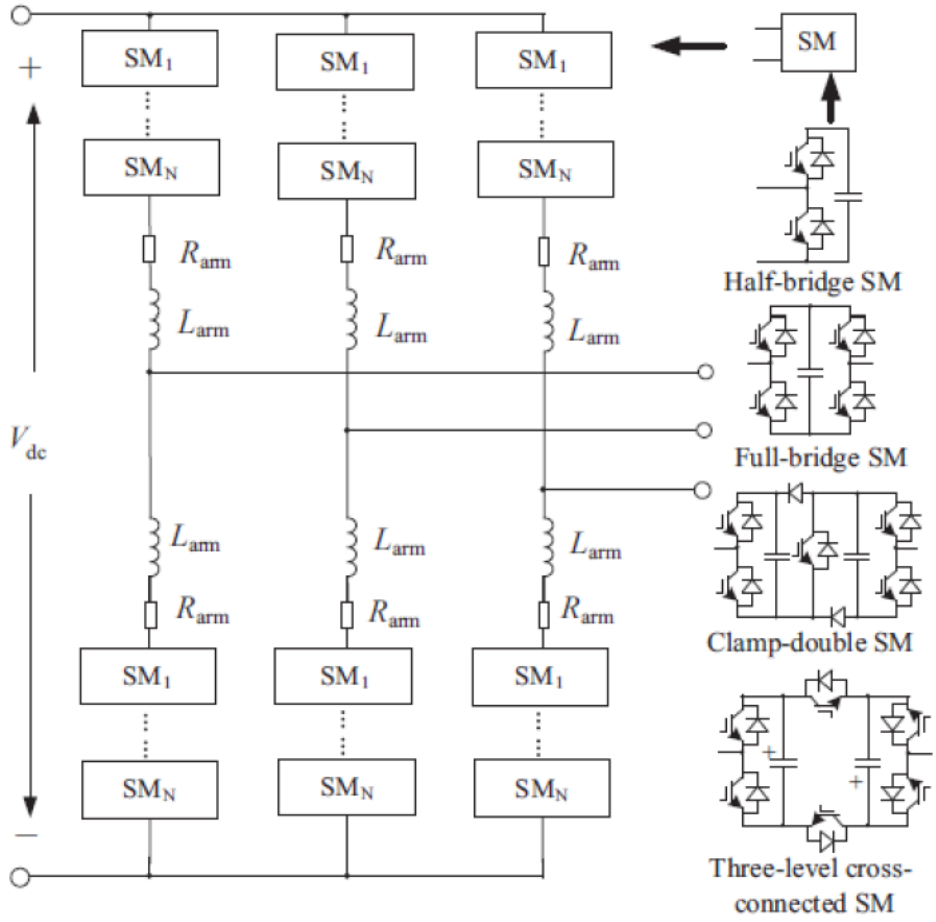

Figure 9 Schematic of MMC

Table 3 compares the attributes of the VSC different topologies for HVDC:

TWO-LEVEL CONVERTERS	MULTILEVEL CONVERTERS
Series-connected IGBTs and PWM	Multi-modular in cascaded connection
Conceptually simple circuit	Easily scalable
Requires PWM	More complex controls
High switching losses	Low switching losses
Harmonic problems from PWM	Virtually no harmonics

Table 3 Comparison between two-level and multilevel converters fod HVDC applications

From now on, it is only going to be considered VSC technology as is the most appropriate for MTHV.

2.2 Configurations and introduction to HVDC grids

Most of up to date HVDC systems are point to point [15]. However, the use of MTDC may provide the following advantages compared with a conventional HVDC transmission system between two points [4]:

- Improve reliability of the DC link
- Better handling of the intermittent nature of renewable generation
- Maximize use of converters

Table 4 shows actual projects of MTHV in China [6].

System Name	Terminals	Rated Power (MW)	Rated Voltage (kV)	Status
Nan'ao	3	200 / 100 / 50	± 160	Commissioned (2013)
Zhoushan	5	400 / 300 / 100 / 100 / 100	± 200	Commissioned (2014)
Zhangbei	4	3000 / 3000 / 1500 / 1500	± 500	Under Construction

Table 4 MTHV projects in China

This chapter will introduce the basics to understand the HVDC system configuration and grids.

2.2.1 System configuration

There are three basic configurations according to VSC; asymmetrical monopole, symmetrical monopole, and bipolar configurations [12].

Figure 10 [12] shows an asymmetrical monopole configuration, where a three-phase connection is to the DC converter midpoint, and in the DC side one pole is grounded. The current return can be done by a metallic neutral conductor or by ground where high ground currents are allowed. In case of a metallic return, the cable must be size for the total current, but lightly insulated. This configuration is the simplest one, but the disadvantages are that the transformer must withstands constant DC component and a failure in the high voltage cable leads to the complete disruption of the line.

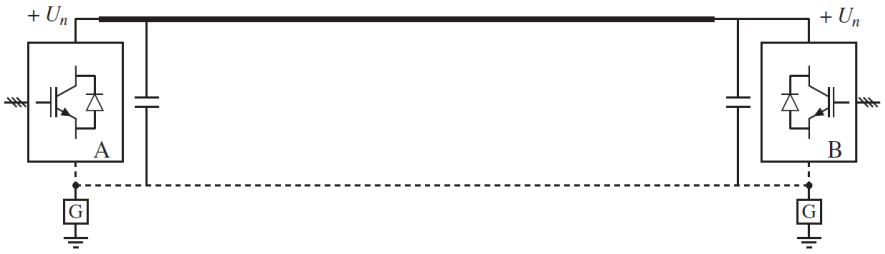

Figure 10 Asymmetrical monopolar configuration

The symbol G corresponds to the grounding, which can be done as shown in Figure 11 [12]. The grounding of the system can be done by direct grounding (a), resistive grounding (b), inductive grounding (c), capacitive grounding (d) and high impedance grounding (e). High impedance grounding is usually employed as fault currents are minimized with this configuration.

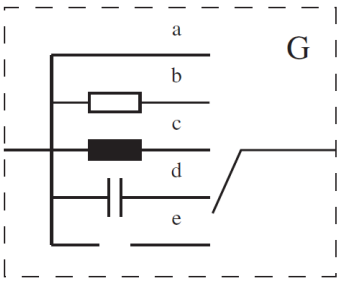

Figure 11 Grounding options

Symmetrical monopolar configuration is showed in Figure 12 [12]. The AC connection is made in the same way, but the two terminals of DC link are connected to two poles working with the same voltage level but in opposite sign. These poles must be rated to the duty current and full voltage. As DC voltage is symmetrical, the transformer does not experiment any DC voltage. The grounding can be done by connecting the midpoint of the DC bus to ground by a high impedance.

Figure 12 Symmetrical monopolar configuration

In case of pole to ground fault, the healthy pole can reach theoretically U_n, this must be considered for the insulation design of both poles. This configuration is widely used in VSC-HVDC. The loss of one converter or line leads to the disruption of the whole power transmission.

By last, Figure 13 [12] shows a bipolar configuration, by connecting two asymmetrical monopoles sharing ground and metallic neutral conductor. Its converter has its own transformer and can operate independently. In normal operation, no current flows through the metallic return path. In case of one converter failure, the return is made by the metallic path ensuring the 50% of power transmission.

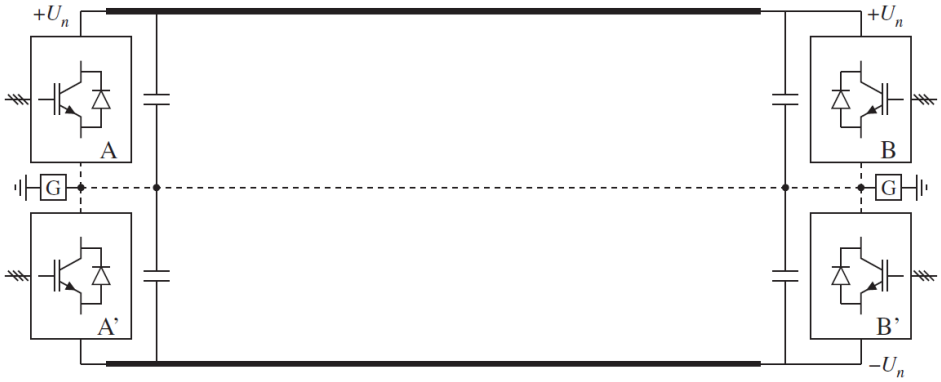

Figure 13 Bipolar configuration

2.2.2 HVDC grids

According to HVDC grids, they can be distinguished as radial topologies and meshed topologies. Radial topologies can be composed by strings or stars, as depicted in Figure 14 [12].

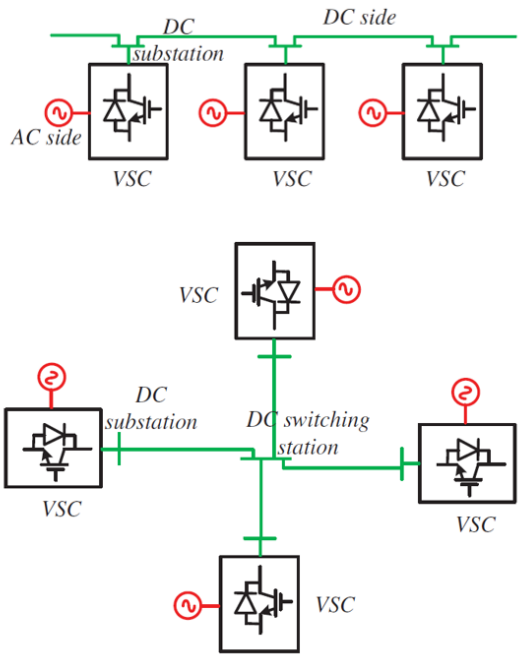

Figure 14 Radial topologies; String composition (up), star composition (down)

While meshed topologies can by created by the union of two or more radial topologies or by a real meshed grid composed by several nodes, as shown in Figure 15 [12].

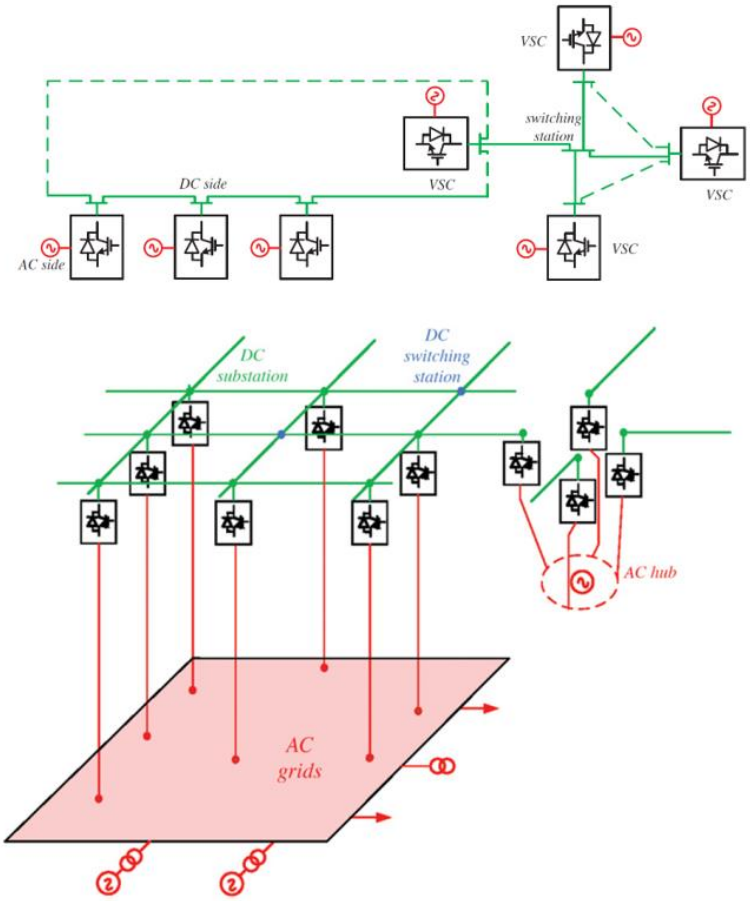

Figure 15 Meshed topologies

More detailed multiterminal grids, considering the possible configurations, are shown in Figure 16. Some possible HVDC grids could be (a) Asymmetric monopolar grid with earth return, (b) Symmetric monopolar grid, (c) Bipolar grid with metallic return, (d) bipolar grid with metallic return and asymmetric monopolar tapping, (e) bipolar grid with metallic return and symmetric monopolar tapings, (f) bipolar grid with metallic return and bipolar tapping with earth return.

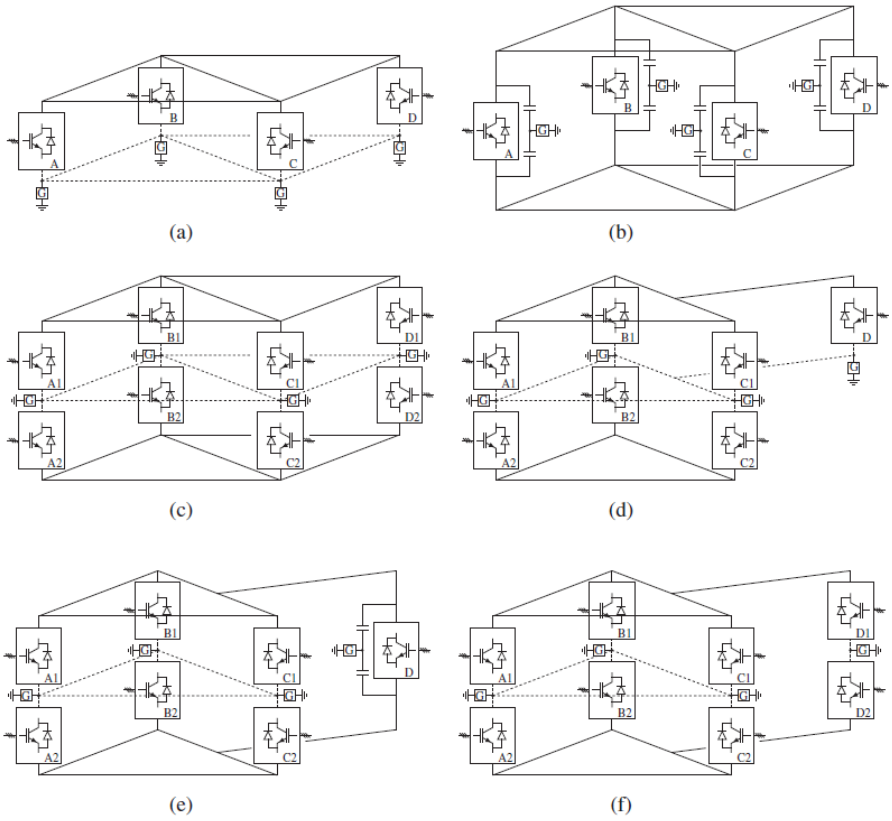

Figure 16 Possible HVDC grids

Figure 17 shows one of the typical case study multiterminal HVDC meshed grid, which interconnects offshore wind farms with mainland AC systems.

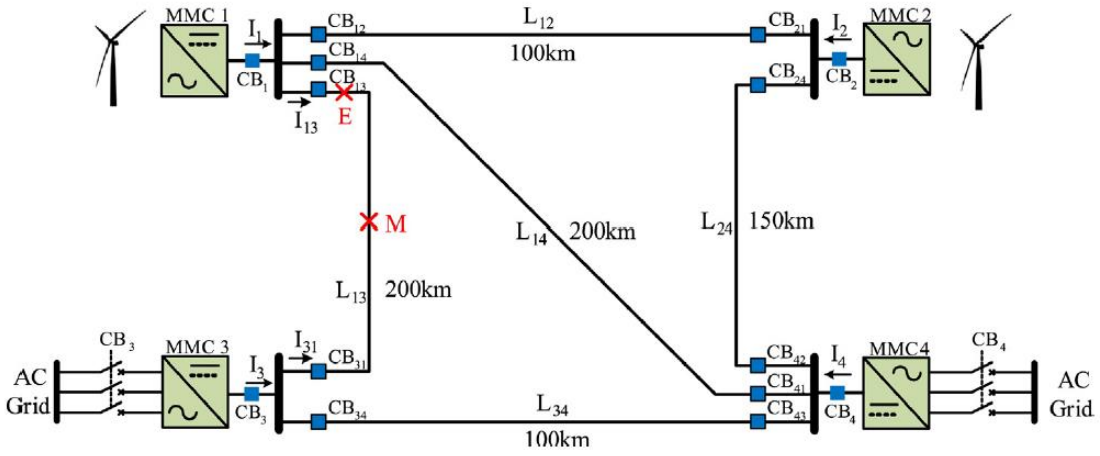

Figure 17 Four terminal HVDC meshed real grid [16]

This grid configuration could be considered as a real HVDC grids as if offers redundancy, meshed connections, and circuit breakers to isolate faulted lines.

The parameters of the grid are shown in Table 5:

Parameter	Conv 1,2,3	Conv 4
Rated Power [MVA]	900	1200
AC grid voltage [kV]	400	400
Converter DC voltage [kV]	$\pm$320	$\pm$320
Arm capacitance C_{arm} [uF]	29.3	39
Arm reactor L_{arm} [mH]	84.8	63.6

Table 5 MTDC grid parameters

The main impediment for the MTDC development is the lack of appropriate direct current circuit breakers for high voltage and current levels.

2.3 HVDC Faults

As every power system, HVDC grids are exposed to faults, especially in overhead lines. DC protection systems must fulfil the same objectives as AC protection [17].

- Detect and isolate the faulted line, equipment, or installation
- Detect and alarm about the undesirable situations in lines, equipment, or installations
- Detect and alarm about the abnormal situations in lines, equipment, or installations

The requirements of a DC protection systems are the same as the AC ones:

- Sensitivity: Capability of being able to operate under the minimum fault condition
- Selectivity: Capability of being able to distinguish the faults when the protection device must act, so the smaller number of protection devices is tripped.
- Speed: This is essential for minimizing the hurt provoked by the fault in the protected equipment.
- Reliability: Grade of reliance of the protection device.

DC faults are characterized for the high rate of rise, large steady state value and no zero natural zero crossing, furthermore, power electronic components might suffer irreversible damages. Considering all this, the fault clearing time lies in the order of milliseconds (< 5ms), comparing with the relatively large clearing time in AC system (2-3 grids cycles) due to the exploitation of the natural zero crossing.

The prospective steady-state DC fault current is mainly determined by fault type and system grounding and configuration. The main DC faults can be classified as following [12]:

- Pole to ground faults (a)
- Pole to neutral faults (b)
- Pole to pole faults (c)
- Bus faults (d)
- Neutral to ground faults (e)

Figure 18 [12] illustrates the placement of each fault type in a HVDC system. The most common faults are pole to ground and pole to pole.

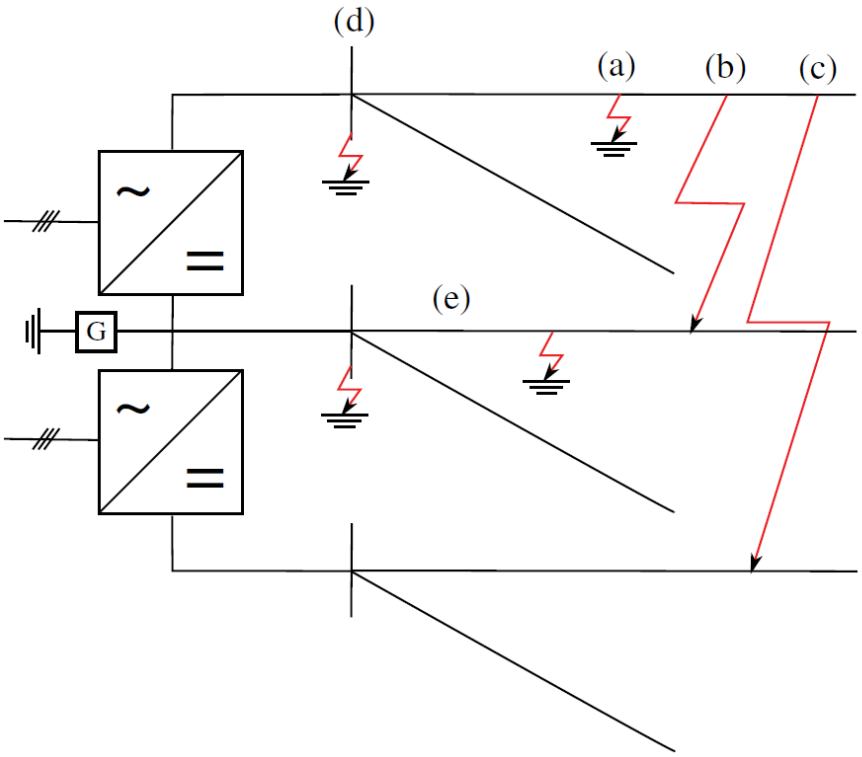

Figure 18 DC Fault types

Figure 19 [12] shows an example of DC fault in HVDC grid. The system response can be evaluated as a DC switched voltage to a RL circuit, which is characterized by the steady state prospective current U_{dc}/R_{line} and the transient rise is determined by the time constant $\tau = L_{line}/R_{line}$. Figure 20 [12] shows the current during the fault and all the events until the fault is cleared by the protection system (PS).

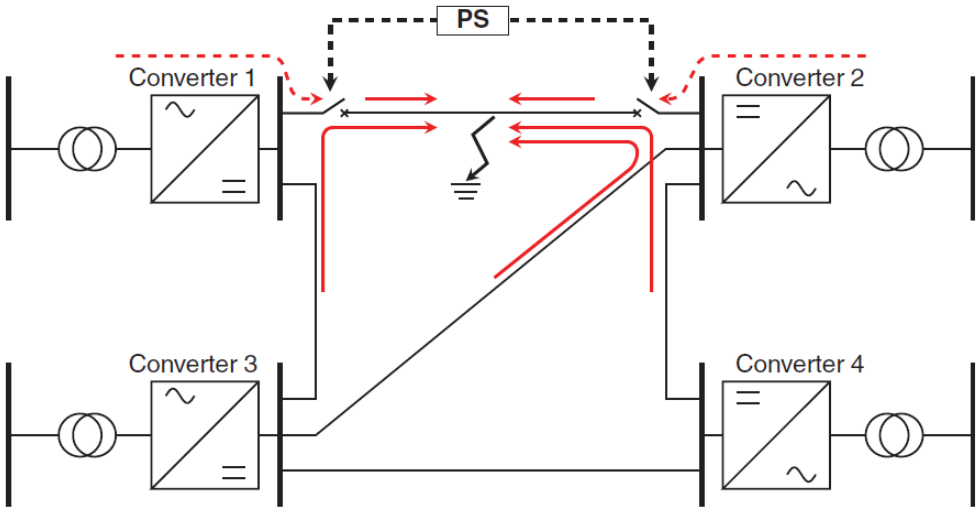

Figure 19 Fault in HVDC grid

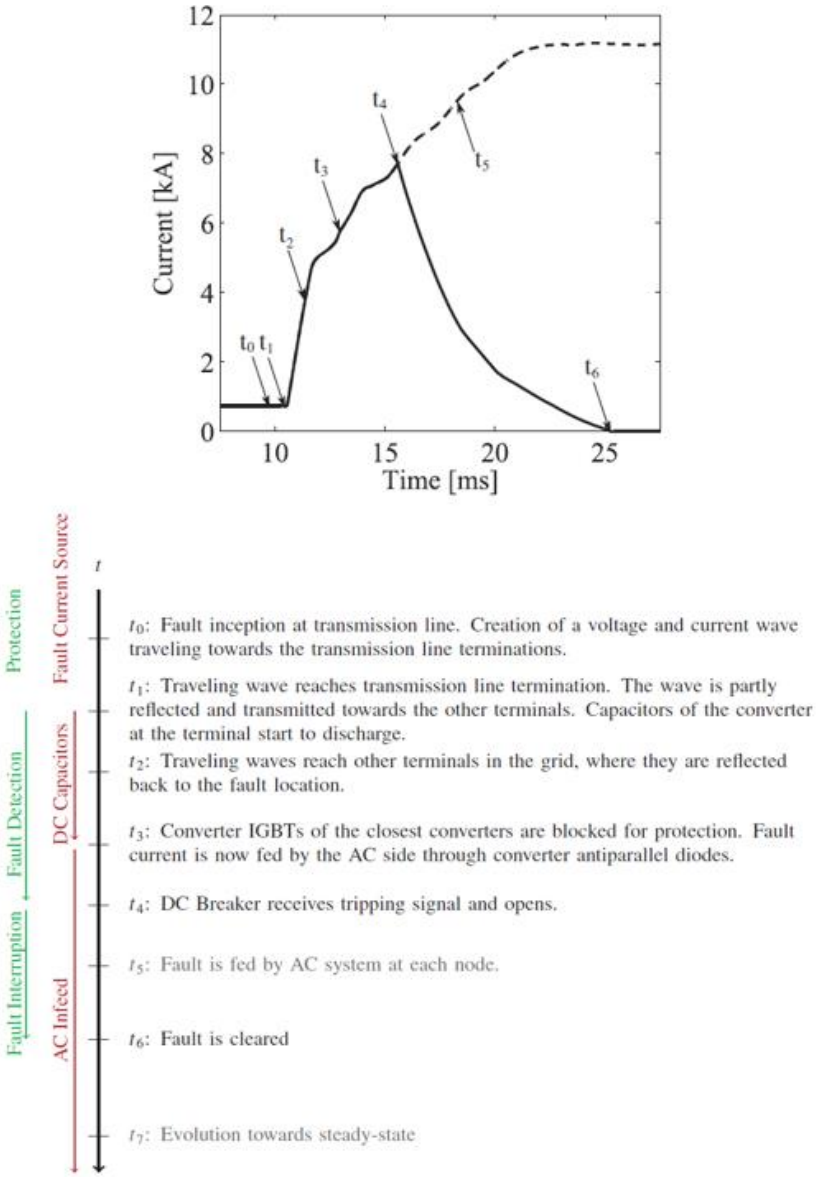

Figure 20 Events during DC fault

When, for instance, a solid pole to ground fault occurs, the voltage decreases from U_{dc} to zero, but this decrease is not measured instantaneously at the line end, this is due to the travelling wave phenomena. The travelling wave speed is dependant of the inductance and capacitance of the line, as is the characteristic impedance. The propagation speed for overhead lines and cables is around the speed light (approximately $3 \cdot 10^8 m/s$) and half of the speed light, respectively.

$$Z_c = \sqrt{\frac{L}{C}}$$

Equation 5

$$v = \frac{1}{\sqrt{LC}}$$

Equation 6

Once the wave has reached the line end, this voltage drop is seen in the terminals and the converters connected to that terminal starts feeding the faults. Part of this wave is reflected to the same line and the other part travels through the other terminals of the HVDC grid, and the other converters connected to the grid will feed the fault as the travelling wave reaches them.

Once analysed the behaviour of the line, analysis on the converter must be done, as it is the fault feeding element. Figure 21 show the behaviour of the converter, which is characterized by four stages.

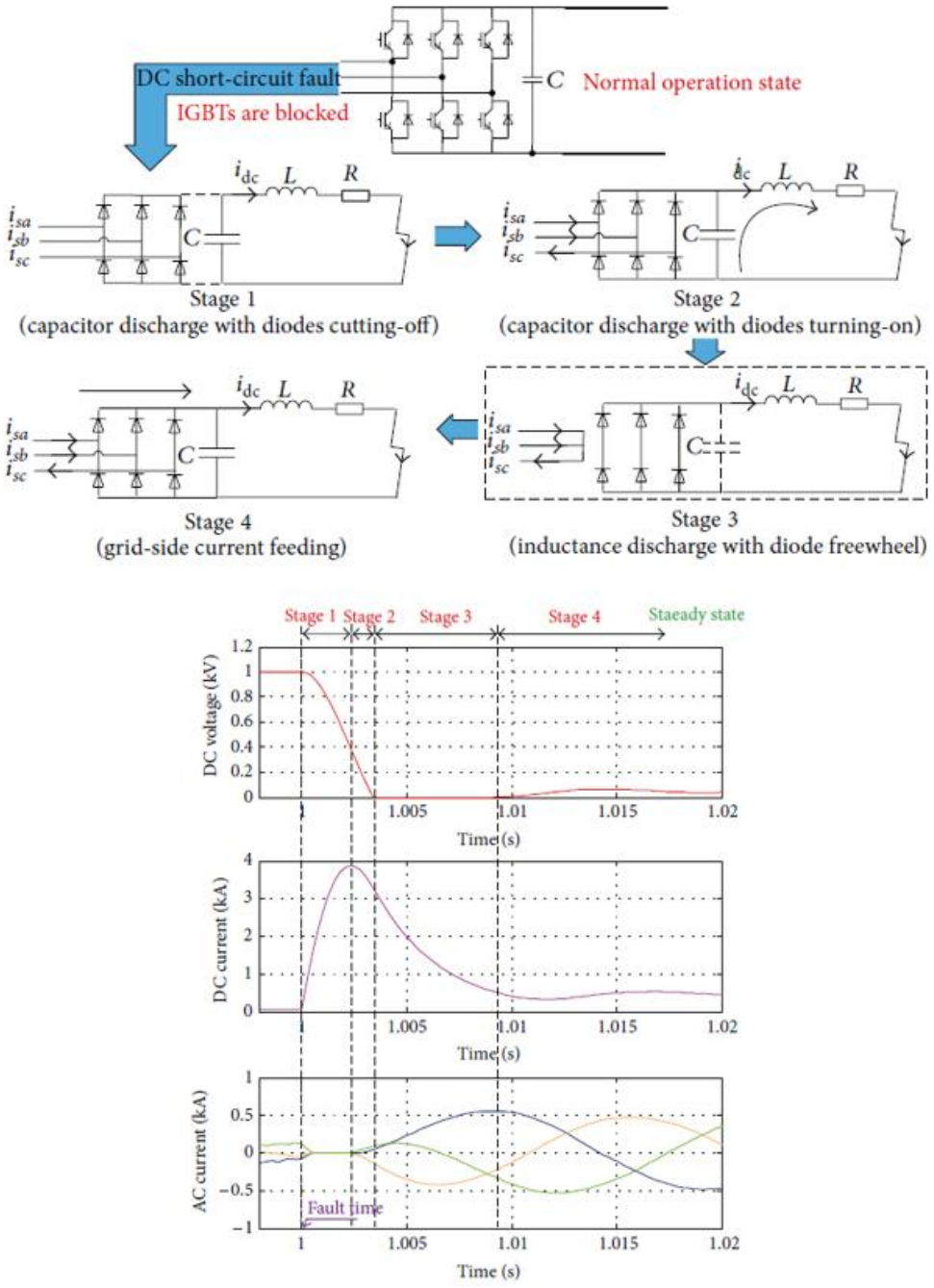

Figure 21 Behaviour of the VSC during DC faults

For simplifying the analysis, a schematic of a two level VSC is shown, however, there are several scientific papers explaining the behaviour of other, and more complex, converters, such as MMC (half-bridge or full bridge) and three level NPC.

As soon as the current passes the current threshold, which is usually two times the nominal current, the IGBTs are blocked for avoiding damaged due to thermal stress. The first and second stage are characterized by the discharge of the capacitors, which provides a large current. Once the capacitor voltage is below the peak AC voltage value, the diodes get polarized and the AC side starts feeding the fault, as does the capacitor. When the capacitor is fully discharge, only the AC side feeds the fault and the converter behaves like a rectifier with an extremely high load, this is, extremely low resistance in parallel with the capacitor. Voltage measured in converter's terminals will be:

$$V_{fault} = I_{fault} \cdot Z_{fault}$$

Equation 7

2.4 Direct current Circuit Breakers

One of the main barriers against the development of VSC based MTHV is the high vulnerability to short circuit.

DC fault interruption process is much more complex that the interruption of AC fault current. Conventional AC circuit breakers interrupt the current with the help of natural zero crossing, which does not exist in DC systems.

Moreover, due to the small impedance of the DC system, DC fault current is characterized by high steady state value and rise rate, as stated above in this chapter. Considering this, direct current circuit breakers (DCCB) must open fault current in few milliseconds.

Two-point HVDC transmission line can cope with short circuiting by opening the AC side breakers and de-energizing the whole line, however, this is not desirable for MTHV as the whole system must be de-energized.

This leads to demand of a development of direct current circuit breakers (DCCB) which differs from the AC ones. The acceptance of HVDC networks regarding efficiency, reliability and controllability will strongly depend on the availability of HVDC circuit breakers.

In principle, it is possible to connect many AC nodes to one point generating a so-called multiple-pair configuration as is depicted in Figure 22 [15], where black boxes are DCCB and white boxes are converters. However, there are several advantages by connecting the nodes on DC side [15], as in the right side of Figure 22:

- Number of converter stations could be reduced, significantly reducing the cost and the losses of the total system
- Each station can transmit power individually and can even change from receiving to sending power without requiring that the opposite converters does so
- There is more redundancy and lines can be decoupled individually, maintaining the converters in normal operation.

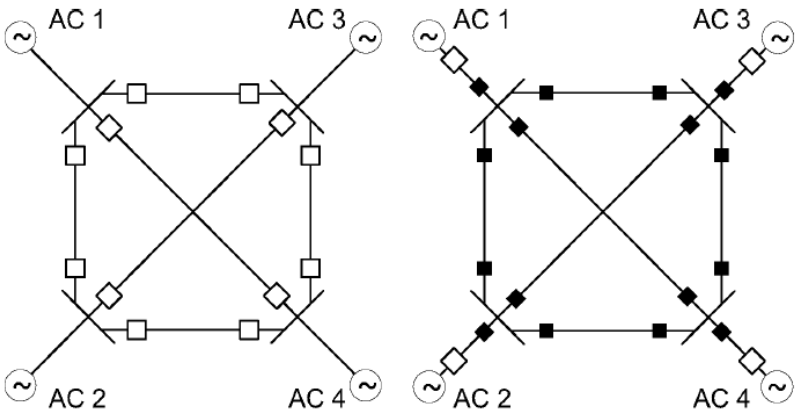

Figure 22 Comparison of point-to-point system grid (left) and real MTDC (right)

Nevertheless, DCCB for high voltage are not commercially widely available today. The main requirements for DCCB are the following ones [18]:

- Create a zero-crossing current to interrupt it (case of conventional hybrid and mechanical)
- Very fast breaking action (due to the high rate of rise)
- Minimal conduction losses (and voltage drop)
- Reliable protection
- Prevent excessive overvoltage
- Minimal arcing
- Provide enough isolation capability to system rating
- Long lifetime
- Less maintenance and, in case, capability to bypassing the current to prevent service interruption

Direct current circuit breakers are usually composed by three parallel paths: the nominal current path, commutation path and energy absorption path. According to DCCB technology, there are mainly three types:

1. Mechanical circuit breakers (M-DCCB)
2. Solid-State circuit breakers (SS-DCCB)
3. Hybrid technology circuit breakers (H-DCCB)

2.4.1 Mechanical DC circuit breakers

Passive mechanical CB are divided in two groups depending on how they create the zero crossing. This zero crossing can be generated by passive or active current injection.

Passive mechanical CB was the first technology developed and was thought for LCC converters. Figure 23 [18] shows the schematic of a M-DCCB, when a fault occurs CB is opened, and the current is commutated to the commutation path. The spark created by the opening of the CB of the nominal current path triggers the resonance between L_c and C_c, DC current is superposed to the resonant current until the amplitude is high enough for creating a natural zero-crossing. This zero-crossing is enough for interrupting the current, however the clearing time is about 60ms, which is very high.

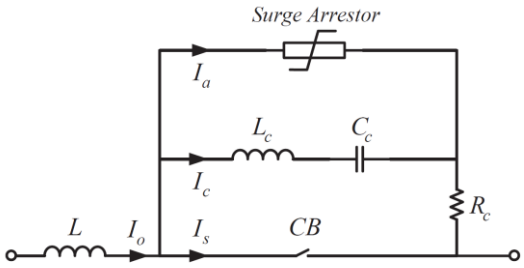

Figure 23 Passive resonant mechanical CB

According to active current injection M-DCCB, Figure 24 [18] illustrates the first (left) and second (right) variants of this technology. The main difference with the former M-DCCB is that the zero crossing is generated with a pre-charged capacitor, C_c, discharging through an inductance, L_c.

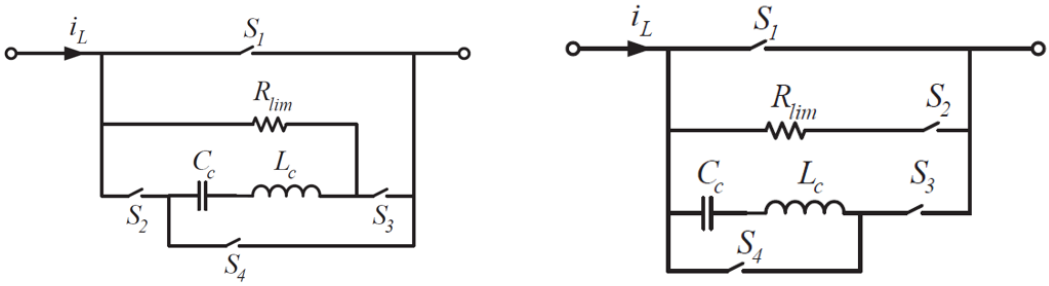

Figure 24 Active resonant mechanical CB

According to first generation topology, when an ordinary operation only S_1 is closed, but when a fault occurs, S_1 opens and immediately S_2 and S_3 closes generating a zero crossing through the commutation path.

2.4.2 Solid State DC circuit breakers

Fast and ultra-fast switching time of semiconductor devices make them very strong candidate for DC fault interruption. This technology is the fastest amongst the DCCB. In pure SS-DCCB IGBTs or other semiconductor are series-parallel connected to support voltage and current during normal and fault condition.

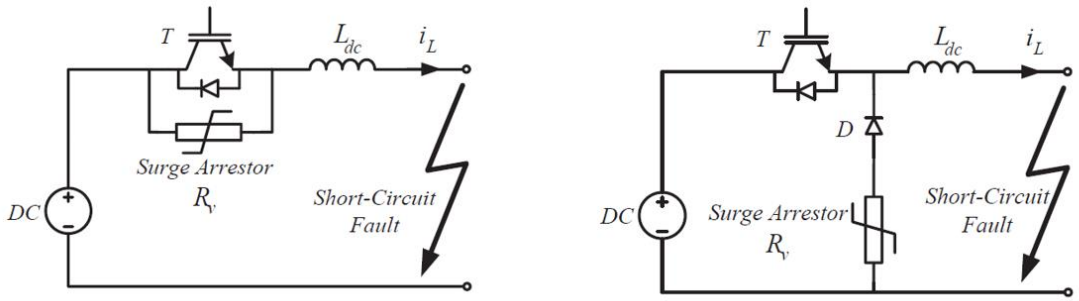

Figure 25 Solid-State CB

Figure 25 [18] shows the first (left) and second (right) topologies of SS-DCCB. In both topologies, T is opened as soon as the fault is detected, and the energy stored in the system

inductance is discharge in the surge arrester. In the second topology, due to the free-wheeling diode, the dissipating capability of R_v is reduced.

2.4.3 Hybrid technology DC circuit breakers

By integrating solid-state devices in a mechanical CB many advantages can be achieved. Recent developments in semiconductor technology such as break-down voltage, conduction losses, switching time and reliability allows the integration of this devices with mechanical pure CB. This combination is traduced in a faster operation than classical M-DCCB with lower operation losses compared with the SS-DCCB.

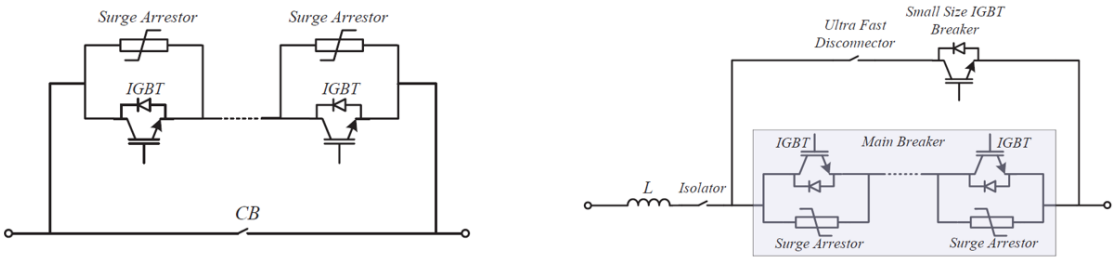

Figure 26 First topology (left) and second topology (right) hybrid circuit breaker

Figure 26 [18] shows the two main topologies for hybrid circuit breakers. During normal operation, current flow through the bypass, this is, ultra-fast disconnector (UFD) and small size IGBT breaker. When DC fault occurs, auxiliary breaker commutates and UFD opens, commutating current to the parallel branch. When this occurs, the main breaker opens and the UFD is exposed to the voltage defined by the protective level of the arrester.

2.4.4 Comparison

Nowadays DCCB technology has many limitations for being considered fully appropriate for a reliable and cost effective MTDC protection. Table 6 [19] compares the main attributes of each DCCB technology.

Feature	Active M-DCCB	SS-DCCB	H-DCCB
Internal current commutation time (ms)	< 5 - 8	0.4	2 - 3
Interruption capability (kA)	2 - 10	19	7.5 - 16
Voltage rating (kV)	< 400	132	320
On-state losses	Negligible	High	Low
Rate of rise of fault current (kA/ms)	1.6 - 2	47	2.9 – 6.7
Installation Costs	Low	High	High
Maintenance	Required	Low	Required

Table 6 Comparison between DCCB tehcnologies

There are no DCCB that meet all the desired requirements. Many future research needs are detected in [15], such as the combination of circuit breakers with current limiters.

The use of high voltage current limiters is stated as one promising solution to cope with the troublesome of the fast-clearing time and current breaking capability.

Specifically, current limiting reactors and resistive type superconducting current limiters in operation with circuit breakers can adjust the response of the system favourably to the maximum breaking capacity and clearing time.

2.5 HVDC grids and protections

As mentioned in the document, HVDC multiterminal systems imply the necessity of fast and high current-voltage capability DCCB, in this section real examples HVDC grids and their implementation of CB breakers are going to be discussed as well as one proposal with R-SFCL.

2.5.1 Real example HVDC grids and protections

As showed in Table 4, up to date there are three multiterminal systems in China.

2.5.1.1 Zhoushan Multiterminal System

Figure 27 [20] shows the MTHV of Zhoushan archipelago, rated to ±200kV, which began commercial operation in 2014. The annual power load of Zhoushan is expected to reach 2000MW this year (2020) due to the economic development of China.

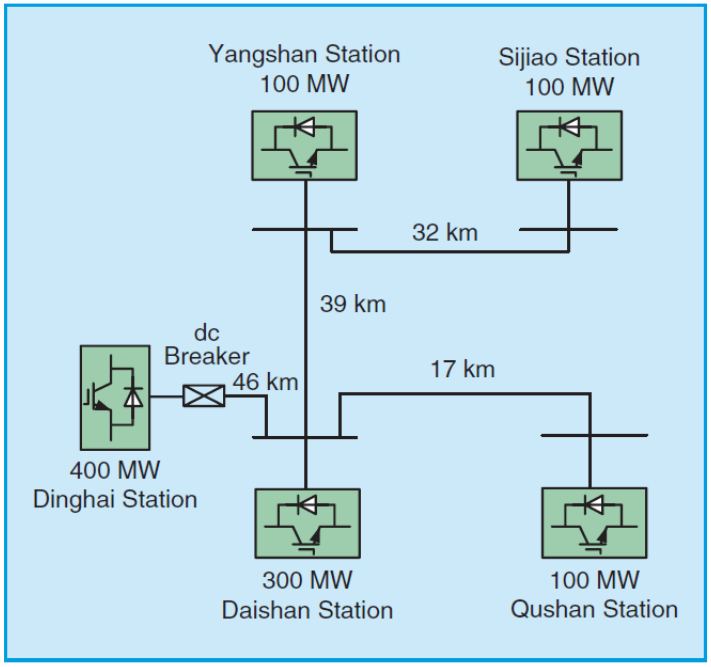

Figure 27 Diagram of Zhoushan archipelago five-terminal HVDC transmission grid

Originally, the faults were cleared by the slow operation of the ac side breakers, which result in many technical problems. In 2016, to improve the grid's reliability, security and efficiency, a hybrid CB rated 200kV with 15kA breaking capability was installed.

Figure 28 [20] shows the installed H-DCCB prototype, which is composed of:

1- Nominal current branch containing an UFD and a full-bridge submodule (FBSM)
2- Main interrupting branch containing 36 FBSM
3- Energy absorber branch to limit the transient voltage

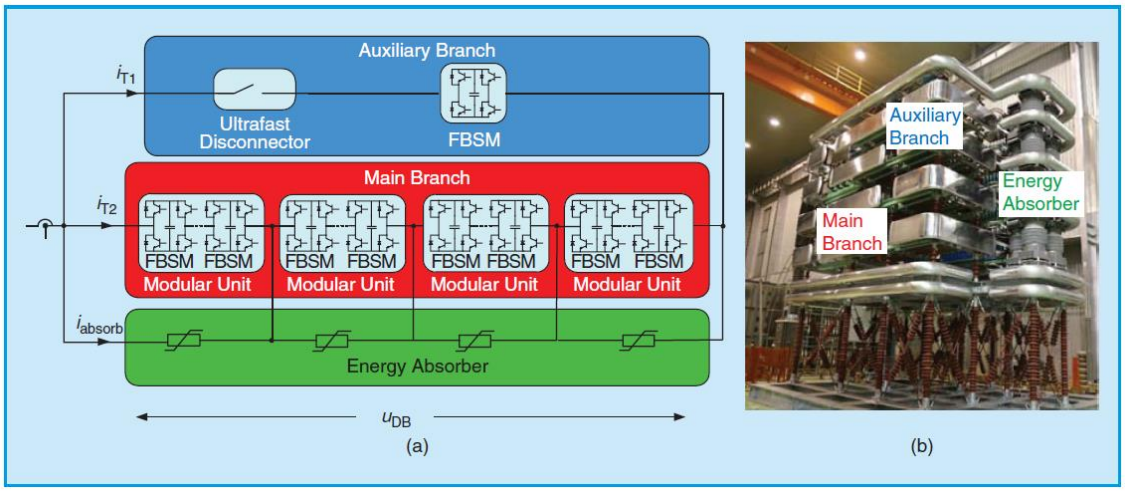

Figure 28 a) Topology b) prototype of the hybrid circuit breaker

The H-DCCB passed the test in which a 15kA short circuit current was interrupted in 3ms with a transient interruption voltage of 320kV.

2.5.1.2 Nan'ao Multiterminal System

Nan'ao multiterminal system, with a ±160kV rated voltage, was put into operation in 2013. The original strategy for fault clearing was the same one as in Zhoushan. Thus, the project was upgraded in 2017 by adding a mechanical circuit breaker with active current injection. The M-DCCB was installed in the overhead line between Jinniu Station and Qingao Station, as shown in Figure 29 [20], as the overhead lines are more propense to faults.

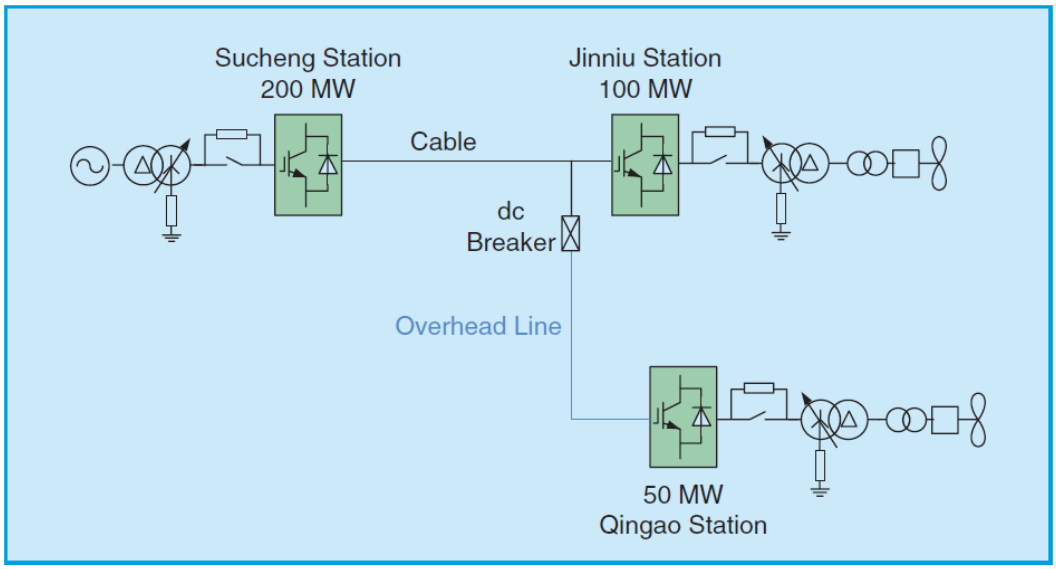

Figure 29 Diagram of Nan'ao three terminal HVDC grid

The installed prototype 160kV M-DCCB consist of the following elements

1- Main branch with four 40kV rated vacuum interrupters. The voltage across these devices is balanced by adding parallel resistances and capacitances, as shown in Figure 30 [20].
2- Current injection is made by an auxiliary low voltage circuit. The unstoppable power supply (UPS) charges the capacitance through and current limiting resistances and a

halfwave rectifier (single diode). When fault occurs, the capacitance is discharge through the transformer that acts as inductance (leakage inductance) and provides galvanic isolation

3- The energy absorber consists of a bank of surge arresters (metal oxide varistors)

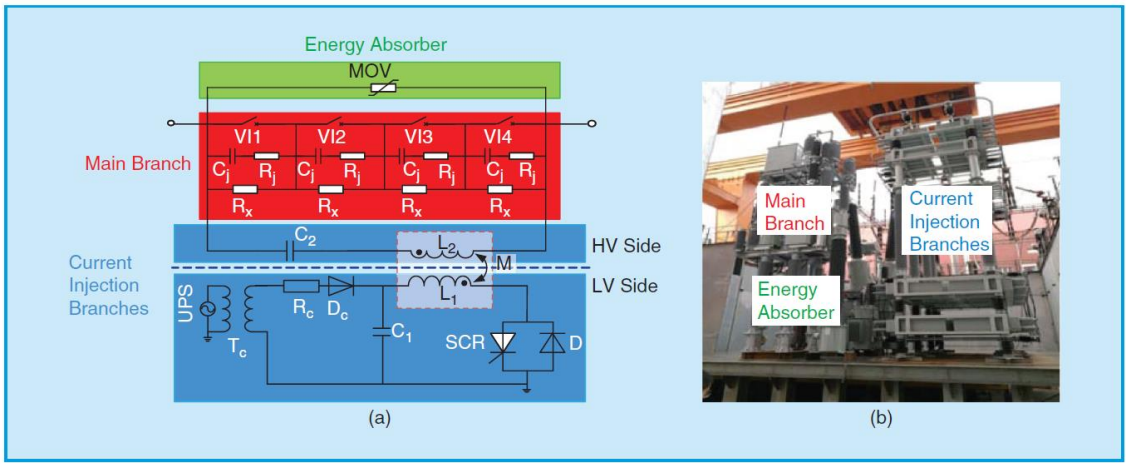

Figure 30 a) Topology b) prototype of the M-DCCB

Compared to conventional M-DCCB, this prototype is less costly and more compact due to the low voltage current injection auxiliary circuit. Experimental results show that the M-DCCB successfully interrupted 9,2kA fault current with a peak transient voltage of 272kV in 3,9ms.

2.5.1.3 Zhangbei HVDC grid

Zhangbei region in northern China has housed many wind projects in the last years and it is expected to grow its installed wind power at least up to this year. However, this wind generation is far from the high consuming points, moreover the variability of wind generation imposes challenges to the proper integration of this electricity into the grid.

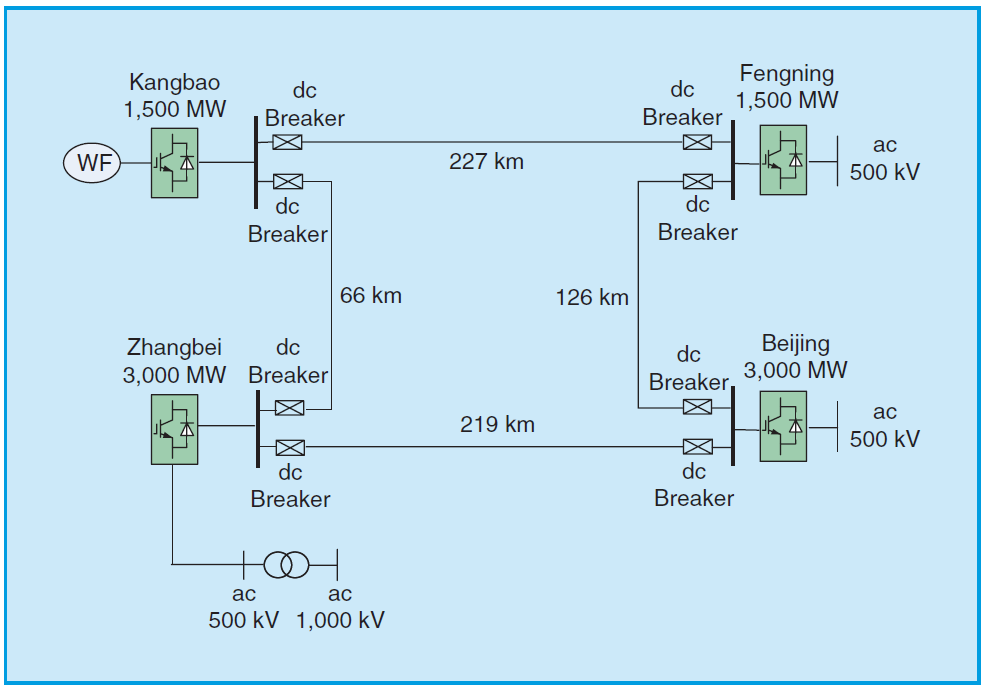

Figure 31 Diagram of four terminal grid of Zhangbei

This can be addressed with the implementation of a multiterminal grid with correct placement of circuit breakers. Thus, a ±500kV, 3000MW four terminal grid was commissioned as the one shown in Figure 31 [20]. Fengning substation is connected to a pumped storage hydro plant, which can even out the fluctuations of wind power.

The project is considered as the first real HVDC grid in world as it has a proper positioning of CB which ensure efficiency and reliability and offers redundancy.

The circuit breakers were developed in 2018. Figure 32 [9] show the H-DCCB implemented in both ends of each line.

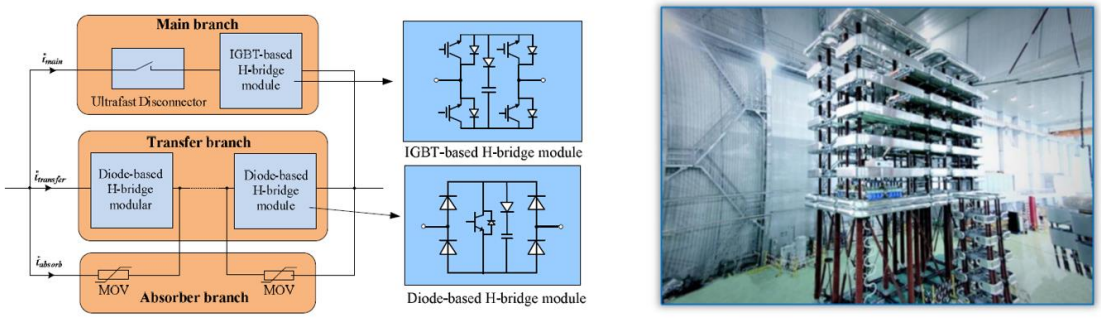

Figure 32 a) Topology b) Prototype of H-DCCB

It has a 535kV rated voltage with 25kA breaking capacity. Breaking time is < 3ms and it can withstand 800kV in open state.

2.5.2 Proposed protection scheme

In [16] the system response is evaluated when a R-SFCL device is add together with a DCCB. Figure 33 [16] shows the evolution of the fault current in different scenarios, depending on the systems parameters, such as fault location, line inductance and CB opening time.

The following assumptions are considered:

- Equal circuit breaker interruption time for systems with and without SFCL
- Having less current limiting inductance with SFCL than in the system without SFCL (Reduction of this element is one of the expected advantages)

In a) the response without SFCL is depicted (less di/dt than other cases). In b) the response with a SFCL is depicted, but the transition time is longer than the CB operating time and di/dt is big enough (due to less inductance) for reaching higher current values that the a) case. In c) the transition time of SFCL is shorter than CB operating time, but still transition time is long enough and the developed resistance is small enough for reaching higher values that a) case. Therefore, it can be concluded that b) and c) cases are undesirable.

Desired system response is depicted in d), where the transition time is fast enough for limiting the current (small time with big di/dt) and the developed resistance is high enough to limit the value under I_{peak1}.

As mentioned above, this response depends on system characteristics, but also in SFCL device characteristics, so this analysis should be considered for designing an appropriate SFCL for each system.

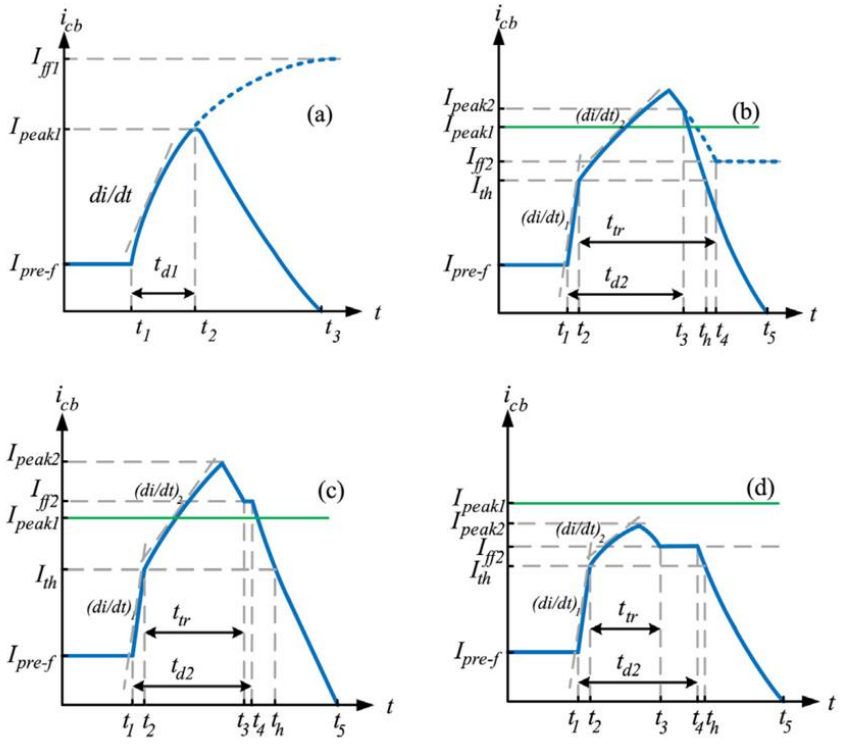

Figure 33 Fault current evolution in different scenarios

In [19], M-DCCB (active injection), SS-DCCB and H-DCCB performance are evaluated with the combination of a current limiting reactor (CLR) and a R-SFCL.

Figure 34 shows the fault currents of all scenarios evaluated in [19], it can be concluded that, firstly, the integration of R-SFCL limits substantially the fault current. Secondly, superconducting SS-DCCB have the smallest maximum current. By last, the maximum current with active injection M-DCCB and H-DCCB is the same.

This is because the current has reached the maximum value U_{dc}/R_{dc} when the M-DCCB and H-DCCB operates, whilst the clearing time of SS-DCCB is small compared even to time constant $\tau = L_{dc}/R_{dc}$ of the faulted circuit and operates before reaching the steady state fault current value.

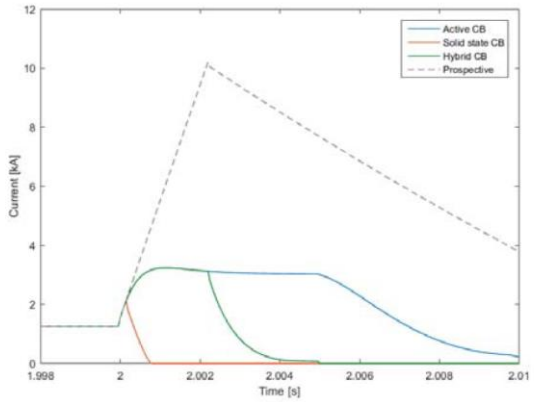

Figure 34 Currents for all scenarios

It can be concluded that the main benefit of the R-SCFL is that the response of M-DCCB and H-DCCB are equalized as more clearing time does not imply higher currents. A similar scenario as

the one depicted in Figure 33 d) is achieved, where the developed resistance limits substantially the current, and the transition time is short enough.

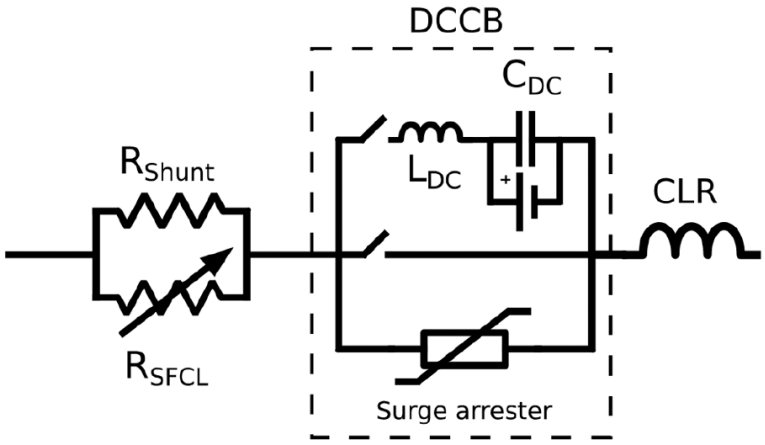

Figure 35 Superconducting M-DCCB with CLR

Furthermore, considering Table 6, it can be concluded that the best choice under the employment of a R-SCFL could be the active injection M-DCCB in series with a CLR, as the one depicted in Figure 35 [21].

3. STATE OF THE ART OF R-SFCL

Superconductivity was first discovered in 1911, when it was observed that some materials loss their electrical resistance at temperatures near absolute zero (4K). In 1986, high temperature superconductivity (HTS) was discovered by observing that some materials offer the same superconducting properties as the former ones, but at much higher temperatures around 70K [3]. In 2020, a research team of the University of Rochester claimed to have created a superconducting material at room temperature, this material is mainly composed by carbonaceous sulfur hydride which show superconducting attributes at 284,5K [22]. Materials with no electrical resistance are very interesting for power system applications.

Another interesting characteristic of the superconducting materials is the Meissner effect. Meissner effect is the repulsion of the magnetic field, this characteristic can be used for magnetic levitation.

Superconducting materials are used for the so called “bullet-train” allowing them to levitate and achieving speeds up to 600 km/h being almost impossible to derail [23]. These materials are also considered key element for allowing the nuclear fusion, where powerful electromagnets are needed so the plasma can levitate using the less amount of energy [24].

According to power system applications, four main promising applications can be distinguished [25]:

1. Superconducting Cables: Superconducting cables allow low losses in power transmission. Nowadays most HTS cables are projected to AC system, DC HTS cables are in early stage but with promising results.

2. Superconducting Magnetic Energy Storage: Energy storage is important for allowing renewable energies integration and for power quality issues. These devices allow the storage of magnetic energy in a superconducting coil with low losses.

3. High Conducting Superconducting Generators: These generators have extremely highly efficient ratios and are very compact. These properties make them very appropriate for offshore wind farm applications where weight is crucial.

4. Superconducting Fault Current Limiters: Superconducting fault current limiters provide one of the most promising solutions for limiting currents. Compared with other technologies, they have negligible losses in normal operation, very high transition from superconducting to normal conductance and automatic triggering and recovering.

The most used superconducting materials in commercial FCL applications are, within the first generation HTS, the Bismuth Strontium Calcium Copper Oxide material (BSCCO), and, within the second generation of HTS, Yttrium Barium Coper Oxide material (YBCO) [26].

3.1 Superconducting fault current limiters

As stated in 2.5.2, current limiters are promising technology to cope with MTHV protection schemes. Current limiters are devices with negligible impedance in normal operation but under fault conditions they insert a series impedance (resistive or inductive), different technology types of current limiters are numbered in 1.2.1.

According to SFCL technology, there are different types [2]:

- Resistive type SFCL
- Inductive type SFCL
- DC reactor type SFCL
- Flux-locked type SFCL
- Vacuum interrupted based SFCL
- Matrix type SFCL
- Resonant type SFCL
- Bridge type SFCL

However, in general, they can be divided into resistive type and inductive type as they insert a resistive impedance or inductive impedance in series with the faulted circuit. The ideal current limiter requirements for HVDC system can be summarized as following [27]:

- Minimum impedance during normal operation. Resistance during normal operation would produce extra heating
- Fast fault current limitation, the FCL is required to change to high impedance in a short time to limit the peak or/and rise rate
- Quick automatic recovery
- Fail safe, in case of fail of the device it should limit the current
- Applicable to high voltages
- Cost effective

Superconducting FCL are appropriate considering these requirements. However, the two main obstacles for the development of this technology are the cryogenic cooling system and the superconductor material cost.

As stated in [27], the efficiency of the AL600 cryocooler at 30K is only 0.87% whilst at 80K is 5.21%, this power is small comparing with the total transmission power but economically is

not attractive. According to material cost, Table 7 shows typical HTS material price together with copper price as reference.

Material	Nominal Operating Temperature [K]	Approximate material cost [$/kAm]
Copper	Tamb	15-25
BSCCO	77	180
YBCO	77	400
MgB2	25	13

Table 7 Price comparison of copper with superconducting materials

Note that even if MgB2 is much cheaper superconductor, the cryocooler efficiency drops for those temperatures.

Table 8 shows the latest projects up to 2016, the most active countries in the development of SFCL are South Korea, China, Germany, the UK and USA.

MANUFACTURER	DATA	TYPE	SUPERCONDUCTOR	FIELD TEST	FUNCTION
Innopower (China)	220 kV, 300 MVA	Saturated core	BSCCO tape	Yes (2010)	--
Kepco (Korea)	22.9 kV, 3 kA	Hybrid	YBCO tape	No (2010)	Transformer protection
Nexans (Germany)	12 kV, 800 A	Resistive	BSCCO bulk	Yes (2011)	Feeder protection
RSE (Italy)	9 kV, 3.4 MVA	Resistive	BSCCO tape	Yes (2012)	Feeder protection
AMSC, Nexans, Siemens (USA)	115 kV, 1.2 kA	Resistive	YBCO tape	No (2012)	--
Zenergy (USA)	138 kV, 1.3 kA	Saturated core	BSCCO tape	Yes (2012)	Transformer protection
Nexans (Spain)	24 kV, 1005 A	Resistive	YBCO tape	Yes (2013)	Bus-bar coupling
Nexans (UK)	12 kV, 1600/1050 A	Resistive	YBCO tape	Yes (2015)	Bus-bar coupling
RSE (Italy)	9 kV, 15.6 MVA	Resistive	YBCO tape	Yes (2016)	Transformer protection

Table 8 Latest projects of SCFL up to 2016 [28]

3.1.1 Principle of operation

According to the principle of operation, the superconductor remains in the superconducting state if the following conditions are met:

- The temperature is below the critical temperature, T_C
- The magnetic field, whether self-induced or applied, is below the critical magnetic field, H_C
- The current is below the critical value, I_C

Figure 36 shows the dependence of these variables with the superconducting state.

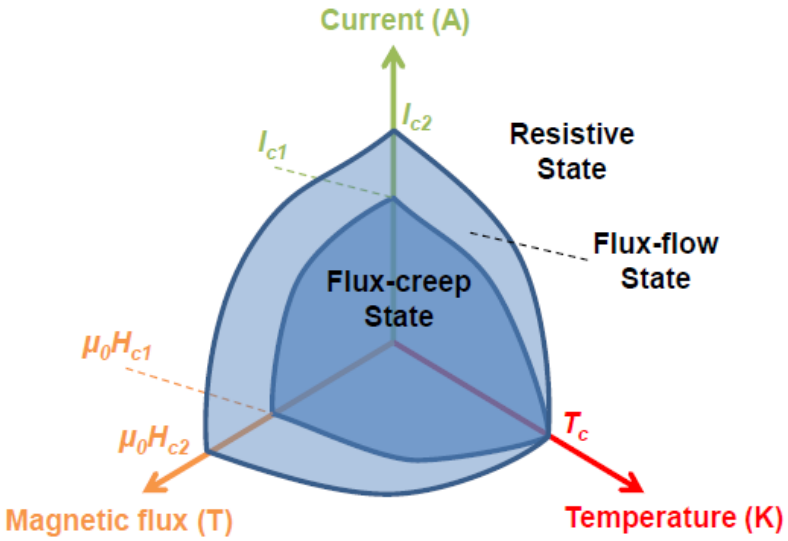

Figure 36 Conditions needed for superconductivity

For a better understanding of the behaviour of the superconducting material, the so-called power law of E-J is usually employed. Superconducting materials have a non-linear relationship between current density and electric field across it, as depicted in Figure 37 [29], which is traduced in a non-linear resistive behaviour.

For the whole range of current density, three main stages can be distinguished:

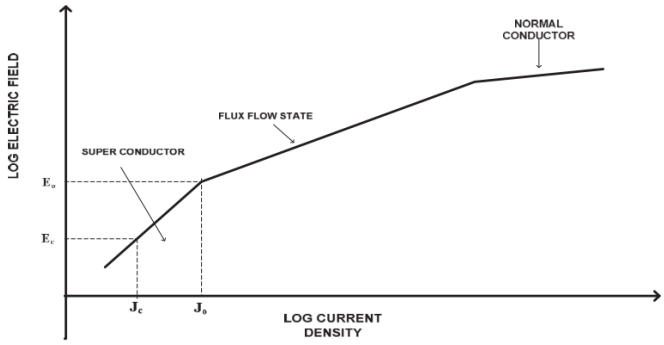

Figure 37 E-J characteristic of HTS materials

a) Superconducting State: For being in this state, as mentioned previously, the HTS material must fulfil the following conditions.

$$T < T_C \qquad H < H_C \qquad I < I_C$$

When current density J exceeds the critical value J_C an electric field E starts to develop across the device, if this J is low enough, it will remain superconducting with a negligible resistance and voltage droop (related to E).

$$E(J,T) = E_C \left[\frac{J}{J_C(T)}\right]^{\alpha}$$

Equation 8

$$J_C(T) = J_C(77K)\left[\frac{(T_C - T)}{(T_C - 77)^{1.8}}\right]$$

Equation 9

b) If J continues increasing and J and E overcomes the threshold values E_o and J_o (related to I_c), the device gets into the flux-flow state and some resistance starts developing. Due to this resistance, the device starts heating, which causes a further increase in resistance and electric field, this state is considered self-enhancing. In this state, the electrical field can be calculated as shown:

$$T < T_C \qquad I > I_C$$

$$E(J,T) = E_o \left(\frac{E_C}{E_o}\right)^{\left(\frac{\beta}{\alpha}\right)} \frac{J_C(77K)}{J_C(T)} \left(\frac{J}{J_C(77K)}\right)^{\beta}$$

Equation 10

c) The device develops more and more resistance and increases its temperature more and more until the critical temperature is surpassed. In this stage the superconductor behaves as a normal conductor and the electric field and the resistance can be calculated as shown where the electric field is linearly proportional to current density and temperature

$$T > T_C \qquad I > I_C$$

$$E(J,T) = \rho(T_c)\frac{T}{T_C}J$$

Equation 11

$$\rho(T) = \rho(T_c)\frac{T}{T_C}$$

Equation 12

Figure 38 shows the resistance development during the quenching process for a rare earth barium copper oxide (REBCO) [30].

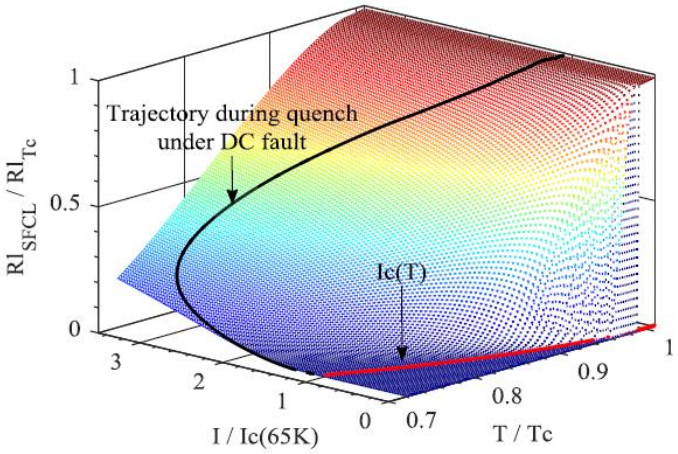

Figure 38 Resistance during quenching process for REBCO

3.1.2 Types of SFCL

As mentioned, there are mainly two types of SFCL, resistive type and inductive type. Resistive type are stated as the more promising ones due to their advantages over inductive ones.

3.1.2.1 Inductive Type

There are two types of inductive SFCL [27], shielded iron-core and saturated iron-core SFCL. However shielded iron core was abandoned due to bulky iron core and difficulties for making the quenching phenomena uniformly in the superconducting cylinder.

Figure 39 shows an inductive saturated iron-core, it consists of two iron cores, which are driven into saturation by a DC bias supply. The two iron cores are needed to limit the current in both directions. During normal operation the inductance seen from the power system is very low because the iron core is saturated, however, when a fault occurs, the increased current will drive one of the cores out of saturation, increasing the inductance.

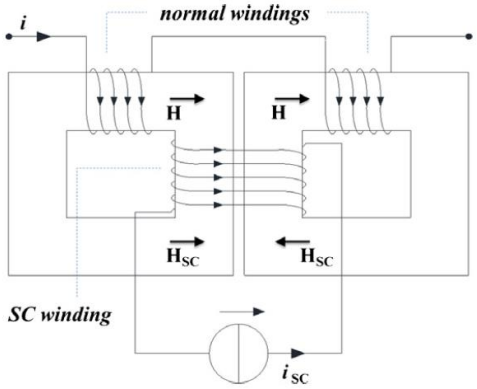

Figure 39 Inductive saturated iron-core [26]

L-SFCL are used to limit the rise time, giving more time to the tripping of the DCCB.

The advantages of the L-SFCL are:

- Inherently fail safe, if DC supply fails, the device will de-saturate offering inductance
- Fast recovery, after fault clearing the unit recovers instantaneously as the DC winding stays superconducting
- No need for cryogenic interface in power line, this is especially advantageous.

The disadvantages of L-SFCL are the followings:

- Bulky and very heavy due to the need of iron core
- Slow efficiency due to losses in primary winding
- Complex current supply for the DC coil

3.1.2.2 Resistive type SFCL

R-SFCL are the simplest and most compact SFCL [27]. Figure 40 [27] shows the schematic of a R-SCFL, with shunt impedance. The R-SFCL uses the natural characteristics of the superconductivity to limit the current increasing the resistance of the device automatically when the current threshold is overcome.

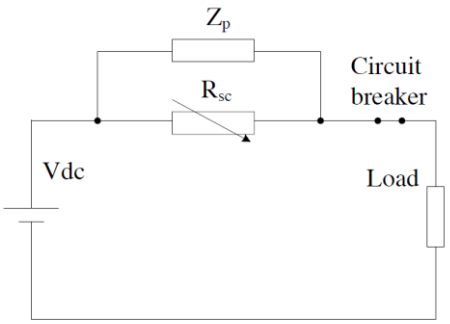

Figure 40 Electric circuit of a resistive SFCL with parallel impedance

Shunt resistance or inductance is used to protect the device from over-voltages and to limit the temperature when quenching and, therefore, decreasing the recovery time. This shunt impedance is connected in parallel out of the cryogenic environment and limits the voltage across the device and reduces the cooling demand because part of the heat is dissipated directly to ambient. However, it reduces the current limitation as the equivalent resistance is decreased [4]. Inherent shunt resistance can also be considered as a bounded metal used to avoid hotspots in the superconducting material [3].

R-SCFL can be designed so they have no stray inductance, or they can be designed so they have a limit value of inductance. Figure 41 [31] shows the configuration of a R-SFCL based on several non-inductive “pancakes”. This is achieved by facing the “in-out” current to each other, so the magnetic flux is cancelled out.

Series and parallel configuration of these “pancakes” determine the quenching resistance and rated current.

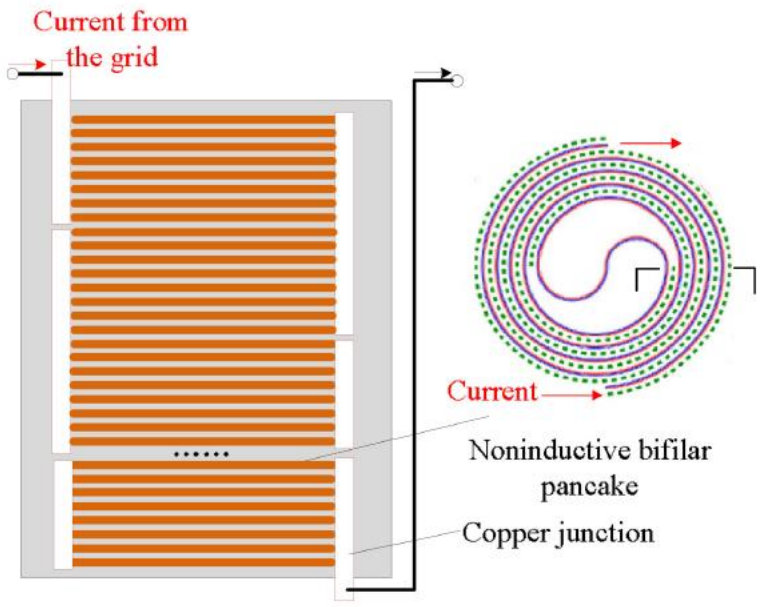

Figure 41 Configuration of R-SFCL based on non-inductive bifilar pancakes

The advantages of the R-SFCL are summarized as follows:

- Compact structure, simple design and light weight, as is an air cored coil
- Automatic triggering, inherently more reliable because no control or signal fail is considered

- Fast and effective current limitation when critical current is overcome
- Intrinsically safe
- Variable inductance coil, it can be designed for minimum value or a finite value

The disadvantage of the R-SFCL are:

- Long length of superconductor wire required
- Hot spot problem, impossible to guarantee uniform quenching
- High energy dissipated in the SFCL coil during the recovery
- Long recovery time due to the heat dissipation and, therefore, temperature hop
- Big cryogenic interface with power line is required

R-SFCL is considered as mature technology, but it has a great potential. Figure 42 show some commercial options for AC systems [32].

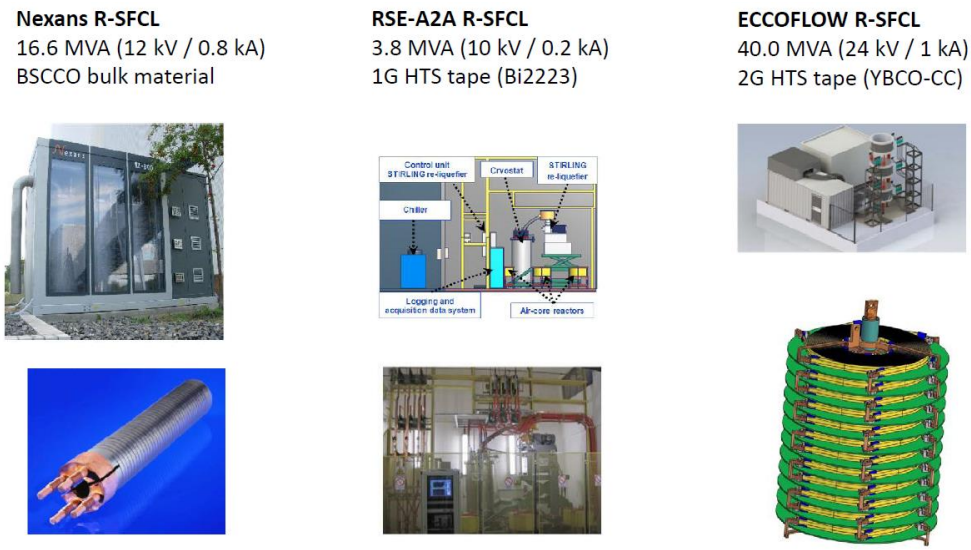

Figure 42 Commercial options of R-SFCL for AC applications

3.1.3 Design Considerations

As depicted in Figure 43 [33], superconductor layer is design when its three dimensions (length, width and thickness) are known based on some considerations. The physical properties of the superconductor material depend on the superconductor type which will affect also in the final dimensions.

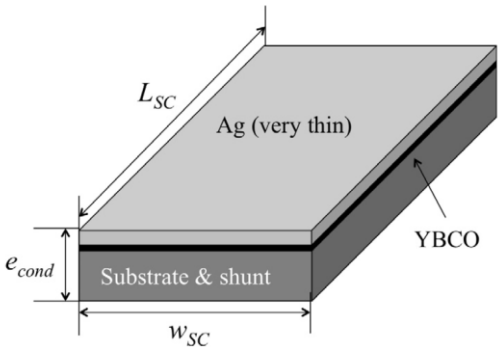

Figure 43 Simplified cross section of the YBCO coated conductor

3.1.3.1 Conductor Width

Superconductor width is set by the desired triggering current, which depends on the set power system normal operation. I_a is defined as the rated current of the system, but this current is commonly overstepped in normal operations of the system (power transformers energization, IM starting etc…). The superconductor triggering current, I_c, must be higher than these current values, so a system curve of overcurrent versus duration time must be considered to set this I_c properly.

A k_a factor is used to simplify the analysis and relate system nominal current to superconductor triggering current, as shown in Equation 13.

$$I_c(T_o) = k_a I_a$$

Equation 13

A relevant superconductor parameter is the critical current per unit width. The critical current of the device must be set by setting the width considering this parameter, the bigger the critical current per width unit, the shorted the width it is, as it can be deduced in Equation 14. The width must be compound paralleling the off-the-shelf tapes available today (typically 6 and 12mm)

$$w_{SC} = \frac{k_a I_a}{I_{c\_w}(T_o)}$$

Equation 14

Thus, a high value of $I_{c\_w}(T_o)$ is desired to minimize the superconductor size. $I_{c\_w}(T_o)$ depends not only on superconductor material but also in temperature. The critical current of YBCO at least doubles when reducing the temperature from 77K to 65K, whilst cryogenic penalty (efficiency reduction at lower temperatures) is only the 20%. This relation can be used to minimize the width, or to operate at variable triggering currents depending on the stablished superconductor temperature.

3.1.3.2 Conductor length

Length is mainly determined by thermal considerations. In normal operation, there are few losses in the superconductor, but as soon as the critical current is overcome a thermal runaway occurs. Power dissipation can reach 2000 kW/m^2 whilst cooling capacity can oscilate around 100-200 kW/m^2. Rapidly it can be concluded that by increasing the length (heat exchange surface) the heat evacuation is enhanced.

According to the following development, superconductor length can be approximated.

$$R_{cond} i_{sc}(t)^2 = \frac{v_{sc}(t)^2}{R_{cond}} = \frac{v_{sc}(t)^2}{\rho(T)\frac{L_{sc}}{A_{cond}}} = c_P(T) A_{cond} L_{sc} \frac{dT}{dt}$$

Equation 15

By clearing L_{sc}, we get Equation 16.

$$L_{sc} = \sqrt{\frac{\int_0^{\Delta t} v_{sc}(t)^2\, dt}{\int_{T_c}^{T_{max}} \rho_{cond}(T) c_P(T) dt}} = V_{SC} \sqrt{\frac{\Delta t}{\rho c_P \Delta T_{max}}}$$

Equation 16

Where Δt is the fault clearing time and ΔT_{max} the maximum temperature hop.

Normally superconductor do not suffer significant degradations for transient temperatures of 720K, but the higher is the maximum temperature, the bigger is the recovery time. Thus, normally 400K are considered as maximum, it is of special interest that the superconductor recovers before 300ms so the line can be reconnected with the device in superconducting state.

As mentioned in this document, shunt resistance also plays an important role as it deviates current out of the superconductor after the triggering. This shunt can be an external resistance of composed by superconductors additional substrate layers (typically Hastelloy) or a combination of both.

3.1.3.3 Conductor Thinkness

The R-SFCL must operate at variable fault currents, from maximum fault current to nominal current value, depending on the fault current resistance. A few percentages of fault currents are solid faults (no fault impedance).

The superconductor element is not totally homogeneous according to critical current; this value can vary up to 7%. Thus, there is a range of currents where the quenching phenomena will be asymmetrical, the stretch with the smallest critical current will quench the first generating a hotspot. According to Figure 44, if a 2kA fault current occurs, theoretically the B1 stretch will quench the first whilst B5 will not.

If the fault current is much higher than the average quenching current, the quenching can be considered homogeneous as the current is far higher than all the quenching currents along the superconductor.

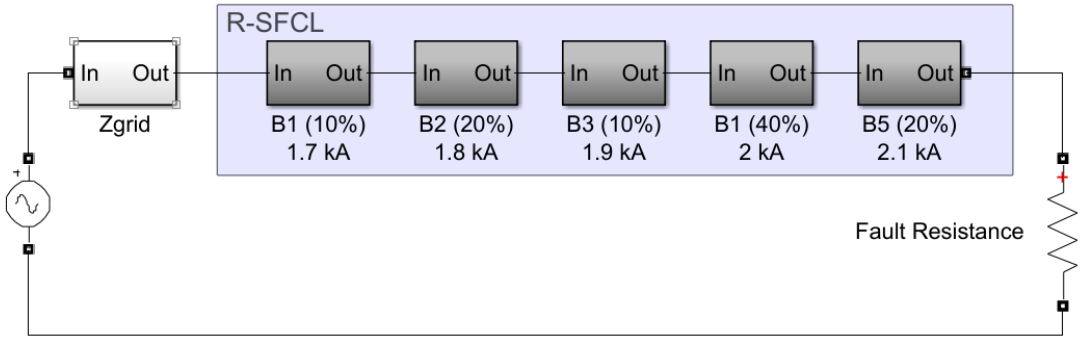

Figure 44 Critical current asymmetries of R-SFCL

The thickness is set to avoid this hotspot for intermediate fault current values. Developing Equation 17, it can be concluded that maximum temperature hop can be limited with the thickness.

$$\rho(T)\frac{L_{sc}}{A_{cond}}i_{sc}(t)^2 = c_P(T)A_{cond}L_{sc}\frac{dT}{dt}$$

Equation 17

$$\left(\frac{i_{sc}(t)^2}{A_{cond}}\right)^2 dt = \frac{c_P(T)}{\rho(T)}\frac{dT}{dt}$$

Equation 18

Integration of Equation 18 gives.

$$\frac{i_{sc}(t)^2}{A_{cond}}\Delta t = \int_{T_C}^{T_{max}} \frac{c_P(T)}{\rho(T)} dt = \frac{c_P \Delta T_{max}}{\rho}$$

Equation 19

Clearing the superconductor surface from Equation 19 we get Equation 20.

$$A_{cond} = I_c \sqrt{\frac{\rho \Delta t}{c_P \Delta T_{max}}}$$

Equation 20

If Equation 20 is expressed according to critical current per width

$$e_{cond} = I_{c-w} \sqrt{\frac{\rho \Delta t}{c_P \Delta T_{max}}}$$

Equation 21

It can be concluded that the higher is the thickness, the smaller the temperature hop will be. From Equation 21, an alternative for I_c is obtained.

$$I_c = A_{cond} \sqrt{\frac{c_P \Delta T_{max}}{\rho \Delta t}}$$

Equation 22

3.1.3.4 Conductor Volume

Volume can be calculated as shown in Equation 23.

$$Vol_{cond} = w_{sc} L_{sc} e_{cond} \approx k_a I_a V_{SC} \frac{\Delta t}{\Delta T_{max}}$$

Equation 23

The superconductor element volume has very few free parameters. Grid requirements fix many parameters, whilst ΔT_{max} cannot vary to much (about 400K). The only free parameters is Δt, which will strongly depend on the CB technology (from few milliseconds to dozens of milliseconds)

3.1.3.5 Design summary

Figure 45 [33] shows three remarkable points fixed by the three dimensions of the superconductor.

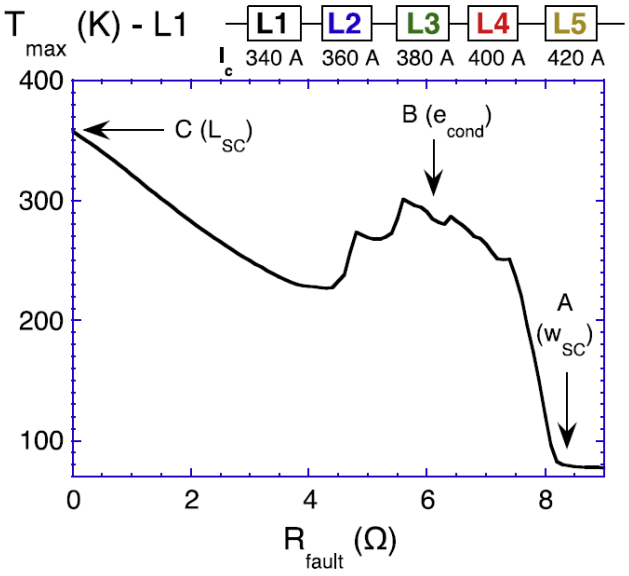

Figure 45 Maximum temperature Vs Fault resistance (fault current level)

A) Starting temperature rise (I_c)
B) Maximum temperature for intermediate prospective current
C) Maximum temperature for maximum prospective current

These three dimensions define the design of the superconductor, the expressions for these variables are grouped in Table 9 [33].

VARIABLE	EXPRESION
Width (w_{SC})	$w_{SC} = \frac{k_a I_a}{I_{c\_w}(T_o)}$
Length (L_{SC})	$V_{SC}\sqrt{\frac{\Delta t}{\rho c_P \Delta T_{max}}}$
Thickness (e_{cond})	$I_{c-w}\sqrt{\frac{\rho \Delta t}{c_P \Delta T_{max}}}$
Volume (Vol_{cond})	$k_a I_a V_{SC} \frac{\Delta t}{\Delta T_{max}}$

Table 9 Design expression summary

3.1.4 Implementation of Real R-SFCL

In this section, a commercial tape for multiple purpose is specified as well as two types of R-SFCL, one for AC and the other one for DC applications.

3.1.4.1 Commercial Tapes

With the purpose of implementing superconducting properties in different applications, there is a range of commercial tapes available. *SuperPower (a Furukawa Company)* manufactures superconducting tapes made of second generation HTS by an automated procedure [34].

The tape integrates buffer and protective layers, as shown in Figure 46 [34]. These layers enhance the performance of the superconducting material and provides additional protection.

Depending on the applications, some layers are more relevant and some other can be even avoided. For FCL applications, copper stabilizer can be avoided and silver overlayer can be modified for better thermal behaviour.

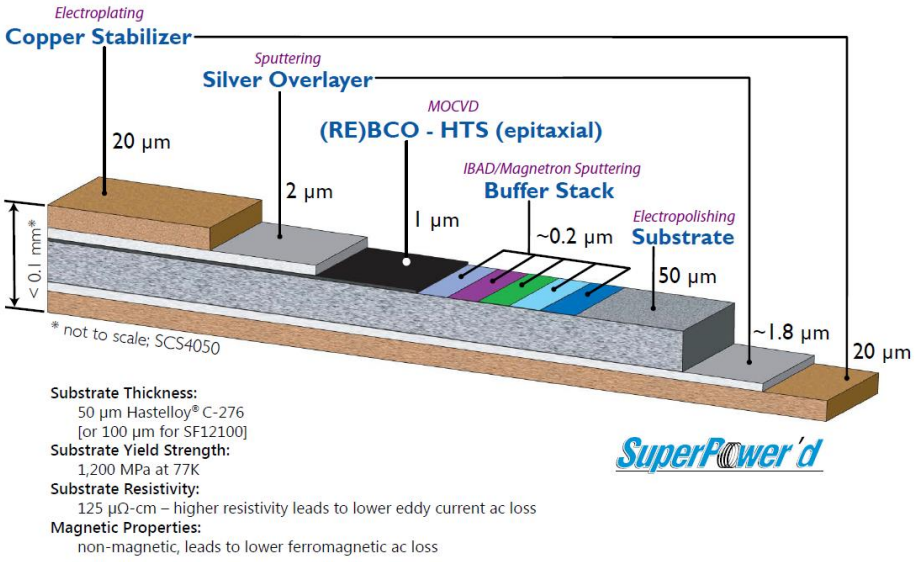

Figure 46 Commercial superconducting tape from SuperPower

Figure 47 [34] shows the specifications of the superconducting tape.

	Minimum Ic measured by continuous direct current	Width	Total Wire Thickness	Critical Axial Tensil Strain at 77K	Critical Bend Diameter in Tension (40µm) @ room temp	Critical Bend Diameter in Compression (40µm) @ room temp
SF = Stabilizer Free *(standard 2µm of silver)*						
SF2050	50 amp	2 mm	0.055 mm	0.45%	11 mm	11 mm
SF3050	75 amp	3 mm	0.055 mm	0.45%	11 mm	11 mm
SF4050	100 amp	4 mm	0.055 mm	0.45%	11 mm	11 mm
SF6050	150 amp	6 mm	0.055 mm	0.45%	11 mm	11 mm
SF12050	300 amp	12 mm	0.055 mm	0.45%	11 mm	11 mm
SF12100*	300 amp	12 mm	0.105 mm	0.40%	25 mm	25 mm
SCS = Surround Copper Stabilizer *(standard 2µm of silver and 40µm of copper; critical tensile stress of >550MPa at 77K)*						
SCS2050	50 amp	2 mm	0.1 mm	0.45%	11 mm	11 mm
SCS3050	75 amp	3 mm	0.1 mm	0.45%	11 mm	11 mm
SCS4050	100 amp	4 mm	0.1 mm	0.45%	11 mm	11 mm
SCS6050	150 amp	6 mm	0.1 mm	0.45%	11 mm	11 mm
SCS12050	300 amp	12 mm	0.1 mm	0.45%	11 mm	11 mm

* 2G HTS wire type SF12100 with highly resistive substrate, flexibility in wire stabilization options and very tight current uniformity is suitable for fault current limiter (FCL) applications. First peak limitation demonstrated with fast response time, low quench current, and rapid recovery.

Figure 47 Specifications of superconducting tape

3.1.4.2 ECCOFLOW R-SFCL

ECCOFLOW resistive fault current limiter was built up with the tapes mentioned above [35]. It was specified to operate in the Spanish and Slovakian AC power system, but for different applications (bus bar coupler in substation and in-line in the outgoing of a feeder of a HV transformer).

Five parallel conductors of about 16-meter length are wound in bifilar arrangement allowing an operating current of 1005 Arms, maximum voltage across the device is 800V. As depicted in Figure 48 [35], shunt air cored reactance is considered in this design (apart from the inherent shunt resistance composed by the buffer and protection conducting layers) in addition to two circuit brakers, CB1 will clear fault current while CB2 is used for decoupling from the system.

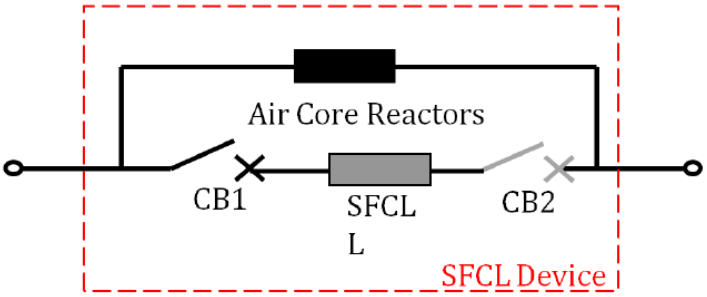

Figure 48 Schematic of the device

Figure 49 [35] shows a 3D model of the device, focusing on the superconducting modules and the modules inside the cryogenic environment.

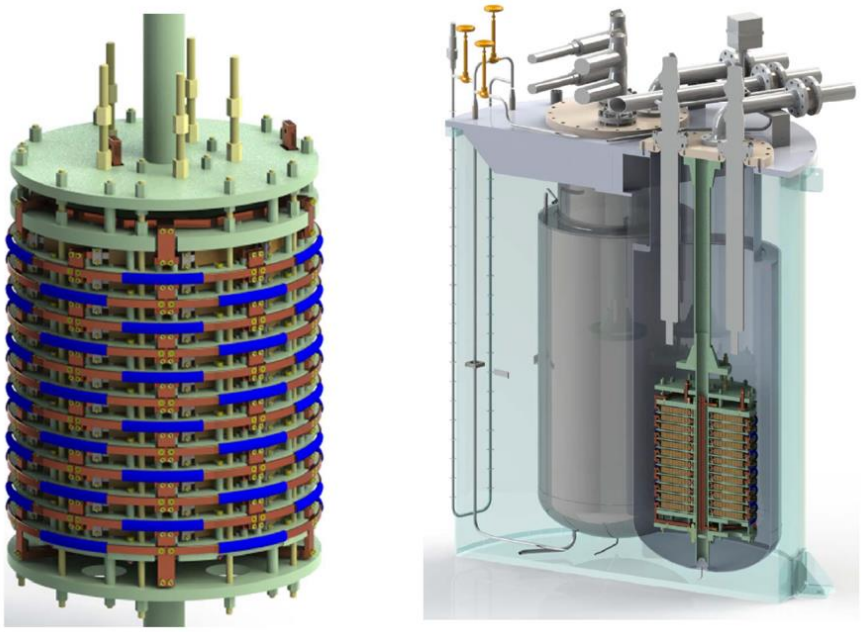

Figure 49 3D Model of ECCOFLOW

As mentioned, the critical current must be homogeneous to ensure a homogeneous transition. Figure 50 [35] shows an example of the homogeneity measured each 5 meters along a 600-meter conductor.

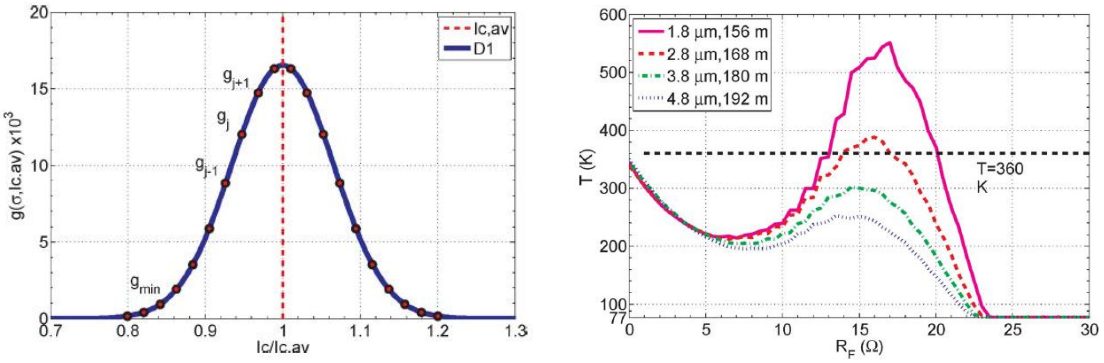

Figure 50 Distribution of Ic along a conductor with average Ic = 380A (left) and maximum temperature Vs fault resistance (right)

It can be deduced that it is not normal to have a deviation higher that 20% and most of the conductor is the ±10% range and how maximum temperatures are given for intermediate fault resistance levels due to the inhomogeneity.

Figure 51 [35] shows the whole system; air cored inductance (outside), cold heads, compressors, water chiller and control system (ISO-container).

Figure 51 Complete ECCOFLOW system

3.1.4.3 40kVdc/2kAdc R-SCFL Prototype

In [36] a DC application 40kV/2kA R-SCFL prototype is exposed. It is composed by 4 branches in parallel, each branch is made by serialising 4 coil modules, as shown in Figure 52 [36]. These coils are made by YBCO tape, each coil has a critical current bigger than 260 amperes at 77K, so the total critical theoretical current at 77K would be larger than 1560 A.

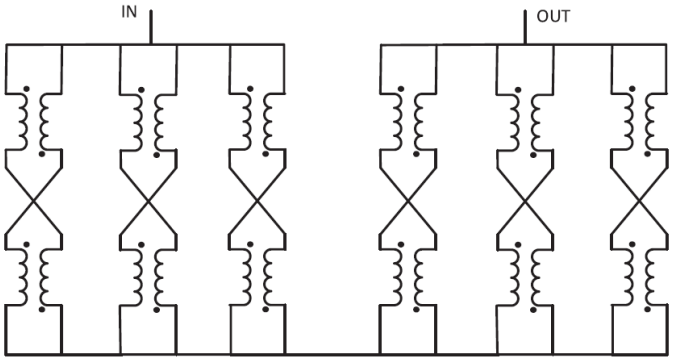

Figure 52 Coil connection of the R-SFCL

Figure 53 [36] shown the structure and assembly of the R-SFCL, inner and outer diameter of each coil is of 176mm and 216mm and the total height of the device is 1600mm approximately.

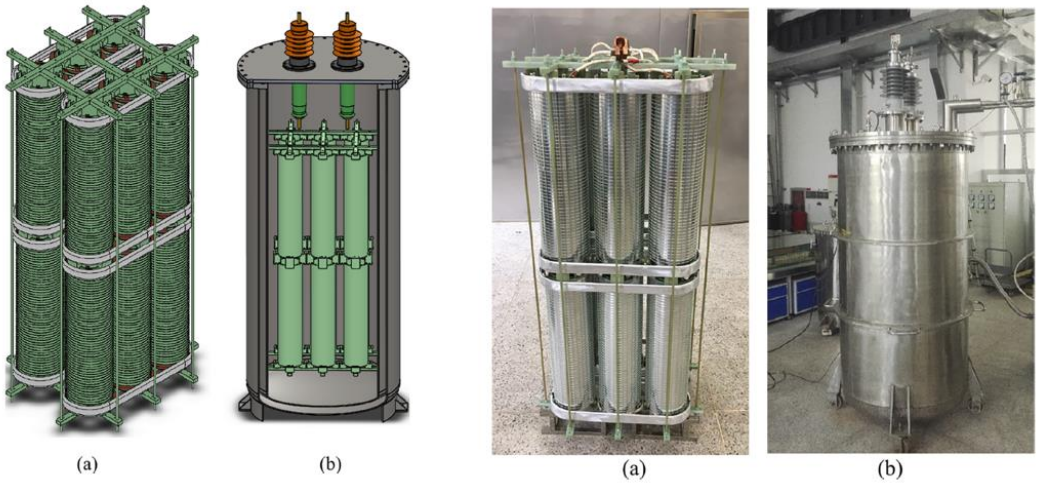

Figure 53 Structure of R-SFCL (a) and assembly (b)

Table 10 [36] shows the specification of the device:

Parameters	Designed Value
Number of parallel branches	6
Number of series branches	4
Number of coils	24
Diameter of one solenoid coil [mm]	216 (out) / 176 (in)
Number of turns of one solenoid	52
Height of one solenoid coil [mm]	727
Thickness of interturn insulation [mm]	1.5
Total height of SFCL [mm]	1600
Length of tapes [m]	800
Operating temperature [K]	65-77
Terminal voltage [kV]	40kV
Resistance at toom temperature [Ohm]	>2.5
Critical current [A]	>1000@77K; >2000@65K

Table 10 Key specification values

To study the flux distribution in the device a 2D FEM analysis was carried out, the results are shown in Figure 54 [36]. Only two coils from different branches are considered on the simulation because of computational cost.

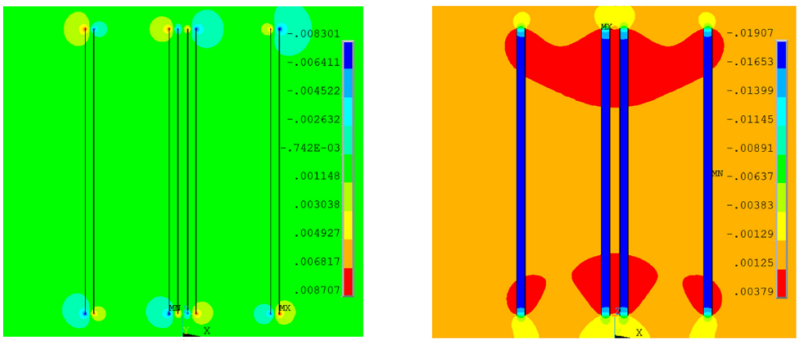

Figure 54 Magnetic field distribution of R-SFCL; radial component (a), axial component (b)

According to radial component, the maximum is found in the end of the coil with a value of 0,009T. Whilst the axial component is maximum between inner and outer coil, with a value of 0.019T.

Test is performed for evaluating the quenching phenomena. For this purpose, by a RLC circuit, a peak current is injected leading to quenching, and by measuring current and voltage across the device the resistance can be calculated, as can be seen in Figure 55 and Figure 56 [36].

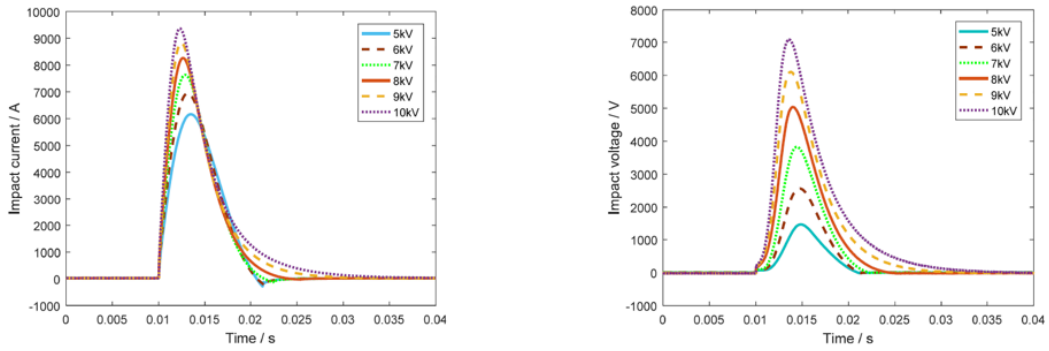

Figure 55 Current and voltage across the R-SFCL

Next, the recovery time can also be evaluated. To ensure that the SFCL is ready for a hypothetical next operation, recovery must be performed before 250-300ms for enabling a reclose of the DCCB. Moreover, the shorter is the time, the less energy is dissipated.

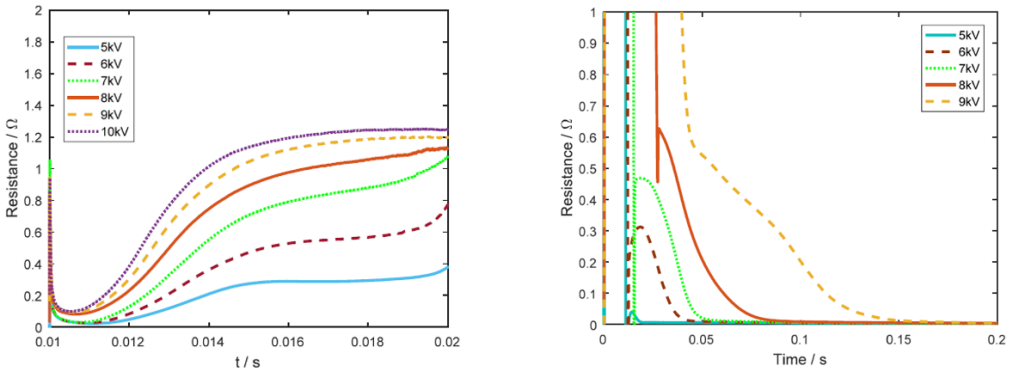

Figure 56 Evolution of resistance value of R-SFCL

3.2 Modelling of the R-SFCL

For analysing the advantages of the R-SFCL, reliable simulation models are needed. The complexity of the model usually lies on a compromise between the accuracy and simulation time.

R-SFCL models can be classified into 4 main groups [25]:

- Simplified Models
- Magneto-Thermal Models
- Finite element modelling (FEM)
- Hardware in the loop (HIL)

For evaluating MTDC systems, most of the models employed are magneto thermal models with different levels of complexity and, therefore, accuracy. For a more accurate thermal or electromagnetic accuracy FEM models are prevalent.

3.2.1 Simplified Models

Simplified models consider the resistance current dependant, so the influence of temperature and magnetic field is not considered. Obviously, this approach is wide far from reality, but it is characterized by its simplicity and in some cases, it can be reasonably accurate.

Simplified models are composed by binary models. According to the binary models, three main models can be considered. The first model consists of a step model [25].

$$\left| \begin{array}{ll} R_{SFCL} = 0 & |i(t)| < i_C \\ R_{SFCL} = R_{MAX} & |i(t)| > i_C \end{array} \right|$$

Equation 24 Step model

A second model can be considered as an exponential model without recovery, which emulates a transition between the superconducting state and normal conduction state.

$$\left| \begin{array}{ll} R_{SFCL} = 0 & |i(t)| < i_C \\ R_{SFCL} = R_{MAX} \cdot \left(1 - e^{e^{\frac{t_o - t}{\tau}}}\right) & |i(t)| > i_C \end{array} \right| \quad where\ t_o\text{: time of fault inception}$$

Equation 25 Exponential model without recovery

The third simplified model can be the exponential model shown in Equation 26 with the addition of a recovery slope.

$$\left| \begin{array}{ll} R_{SFCL} = 0 & |i(t)| < i_C \\ R_{SFCL} = R_{MAX} \cdot \left(1 - e^{\frac{t_o - t}{\tau}}\right) & |i(t)| > i_C \\ R_{SFCL} = R_{SFCL} - a \cdot t_1 & |i(t)| > i_C \ \rightarrow \ |i(t)| < i_C \end{array} \right|$$

Equation 26 Exponential model with recovery

t_1 is the clearing time of the fault and a is the slope, additional slopes can be considering by adding more time intervals.

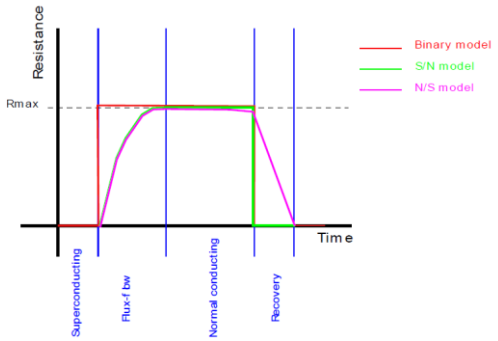

Figure 57 Evolution of resistance for different models

Figure 57 [25] shows the evolution of the resistance for the different simplified models.

3.2.2 Magneto-Thermal Models

Many different magneto thermal models have been detected, having different complexity and accuracy. In summary and for decreasing the number of models evaluated, they can be classified in 4 electrical approaches, each approach makes its considerations. The first three approaches are magneto thermal models indeed, whilst the last approach is based on an

experimental R-Q curve (dependence between the dissipated heat Q and the developed resistance R), which is another tendency of R-SFCL modelling.

3.2.2.1 1st Electrical Approach

The schematic of the R-SCFL is shown in Figure 58 [37], where an additional shunt resistance can be connected to protect the superconducting device from over-voltages and extreme temperature hops.

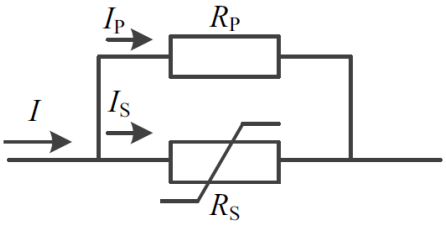

Figure 58 R-SCFL equivalent circuit

According to [37] and [38], the critical current of the R-SFCL I_c is a temperature dependant parameter that can be expressed by Equation 27.

$$I_c(T) = \begin{cases} I_c(0)\left[1 - \left(\frac{T - T_0}{T_c - T_0}\right)^2\right] & T \leq T_c \\ 10^{-7} & T > T_c \end{cases}$$

Equation 27

The voltage of the superconducting material, in this state, increases exponentially with the increasing current as quantified in Equation 28. Transition time from superconducting to normal conduction is generally 1-2ms once the critical current is overcome.

$$U = I_S R_S = U_c \left(\frac{I_s}{I_c(T)}\right)^n$$

Equation 28

When normal state, voltage is proportional to current and temperature, as expressed in Equation 29.

$$U = \rho_{TC} I_c \left(\frac{T}{T_c}\right)$$

Equation 29

The simulation flowchart based on this approach is shown in Figure 59 [37].

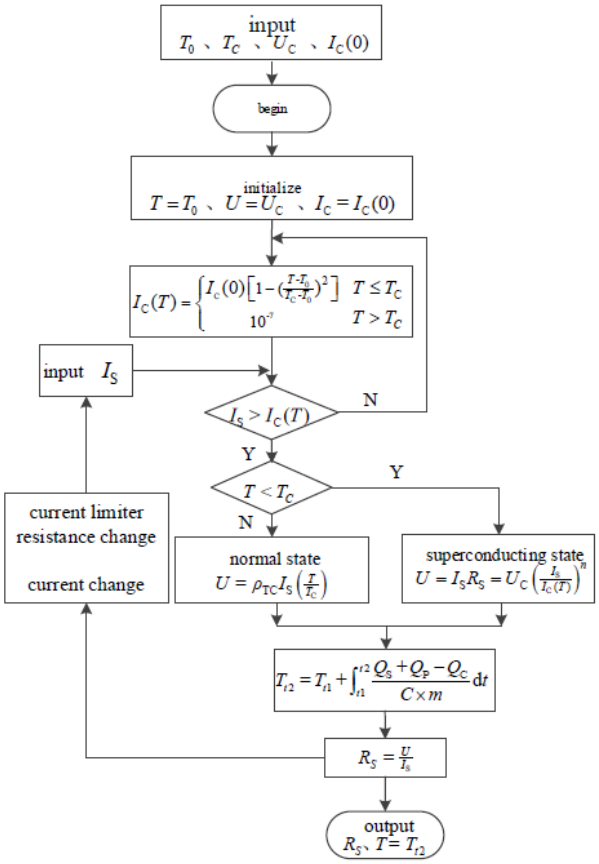

Figure 59 Flowchart of simulation model

According to [38], the resistance evolution of the device under a fault in a PSCAD simulation of Nan'ao MTHV demonstration project is represented in Figure 60.

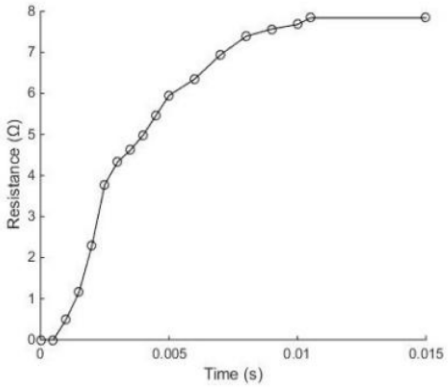

Figure 60 1st Approach model resistance evolution

This model considers an approximated expression for voltage across the device and critical current. Derived from these voltage/current approximations, the total resistance is calculated.

3.2.2.2 2nd Electrical Approach

In [39] and [40], the superconducting is modelled as a sum of resistances. ρ_o represents the superconducting resistivity, ρ_{PL1} and ρ_{PL2} represents the resistivity when the current density increases and ρ_{sat} represents the resistivity in normal state. The equivalent circuit is shown in Figure 61 [40].

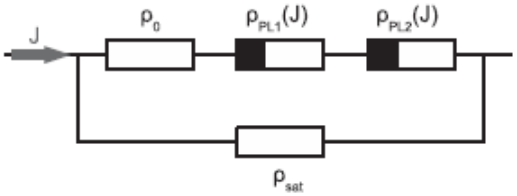

Figure 61 Representation of R-SFCL as sum of resistances

The total equivalent resistance at any instant can be calculated as in Equation 30.

$$\rho = \frac{(\rho_{PL1} + \rho_{PL2} + \rho_0)\rho_{sat}}{\rho_{PL1} + \rho_{PL2} + \rho_0 + \rho_{sat}}$$

Equation 30

The variable resistances ρ_{PL1} and ρ_{PL2} can be calculated by Equation 31 and Equation 32.

$$\rho_{PL1} = \begin{Bmatrix} 0 & J < J_c \\ \frac{E_0}{J}\left(\frac{J}{J_c} - 1\right)^{n_1} & J \geq J_c \end{Bmatrix}$$

Equation 31

$$\rho_{PL1} = \begin{Bmatrix} 0 & J < \gamma J_c \\ \frac{E_0}{J}\left(\frac{J}{J_c} - \gamma\right)^{n_2} & J \geq \gamma J_c \end{Bmatrix}$$

Equation 32

The parameters of Equation 31 and Equation 32 are showed in Table 11 [40].

Element	Value
ρ_0	$\rho_0 = 10^{-14}\Omega cm$
ρ_{PL1}	$n_1 = 2.8$ $E_0 = 0.1 V cm^{-1}$
ρ_{PL2}	$n_1 = 30$ $E_0 = 0.1 V cm^{-1}$ $\gamma = 2$
ρ_{sat}	$\rho_{sat} = 90\mu\Omega cm$

Table 11 Parameters of 2nd approach model

Critical current density dependence with temperature is shown in Equation 33, where typical α value for BSCCO and YBCO materials is 1.5.

$$J_C(T) = \begin{Bmatrix} J_C(T_{ref})\left[\frac{(T_C - T)^\alpha}{(T_C - T_{ref})^\alpha}\right] & T_{ref} < T < T_c \\ 0 & T \geq T_c \end{Bmatrix}$$

Equation 33

The total resistance temperature dependence is shown in Equation 34.

$$\rho(T) = \rho(T_{ref})(1 + \beta(T - T_{ref}))$$

Equation 34

This model expresses a direct calculus of the resistivity (ρ_{PL1} and ρ_{PL2}) by the division of E and J and a power law with different index. It does not consider the chance of the electric field $E(J,T)$.

In [25] a simplified model por this approach is proposed. The resistivity of the SFCL is expressed as in Equation 35.

$$\rho = \begin{vmatrix} 0 & J < J_C, T < T_C \\ \rho_C \cdot \dfrac{J}{J_C} & J > J_C, T < T_C \\ \rho_{HTS} & T > T_C \end{vmatrix}$$

Equation 35

Where

$$\rho_C = \frac{E_C}{J_C}$$

Equation 36

And

$$J_C = J_C(77K) \cdot \frac{(T_C - T)}{T_C - 77K}$$

Equation 37

3.2.2.3 3rd Electrical Approach

The approach developed in [4] and [7] can be considered as the most extended magneto-thermal model, where the different expression for E are considered depending on the state of the superconducting material.

The E value when superconducting is expressed in Equation 8, while flux flow state in represented by Equation 10 and when normal conducting is expressed as in Equation 11.

Thus, the flowchart showed in Figure 62 [4] can be constructed considering these equations and the conditions for each state.

This model considers the $E(J,T)$ dependence.

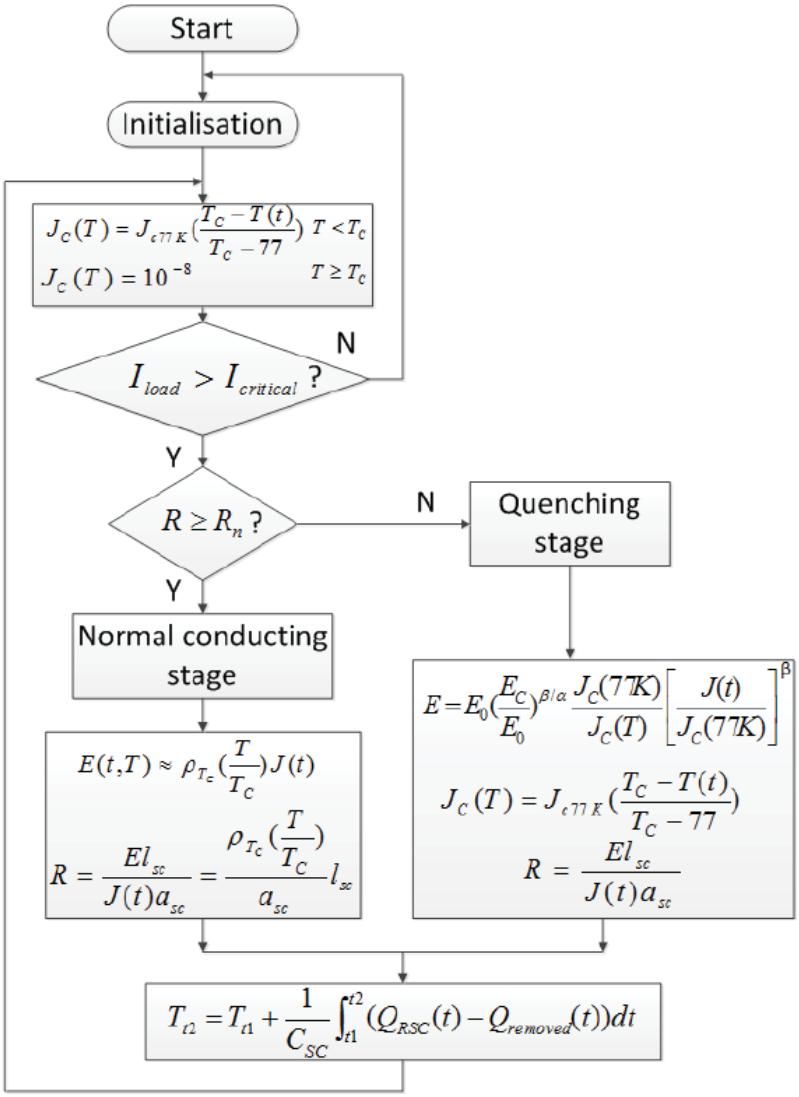

Figure 62 3rd Approach model flowchart

3.2.2.4 4th Electrical Approach

As mentioned, this models differs substantially from the previous ones as it is a model developed from an empirical experiment as the ones carried out in [41] and [39].

Quenching phenomena is a multi-physical process, but from the macro perspective of power system, the R-SFCL can be considered as a variable resistor. From experimental results, it has been observed that there is a relation between the generated heat Q and the developed resistance R under the same cryogenic environment.

Figure 63 [41] shows R-Q curve for a YBCO superconducting type R-SFCL. It can be noted that the curve shape is the same regardless the current value.

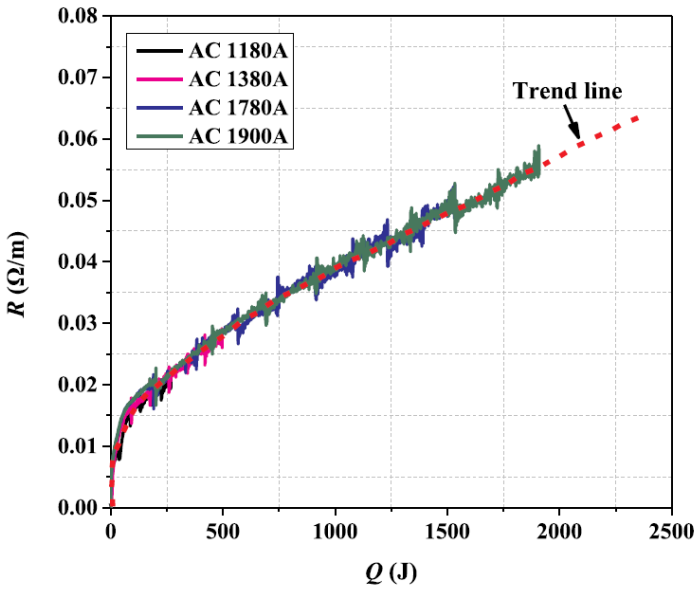

Figure 63 First R-Q curve for different currents

Figure 64 [39] shows the same developed curve for different current values, also for a YBCO superconducting type R-SFCL. Once again, the resistive value is the same regardless the current value, and both curves have the same shape.

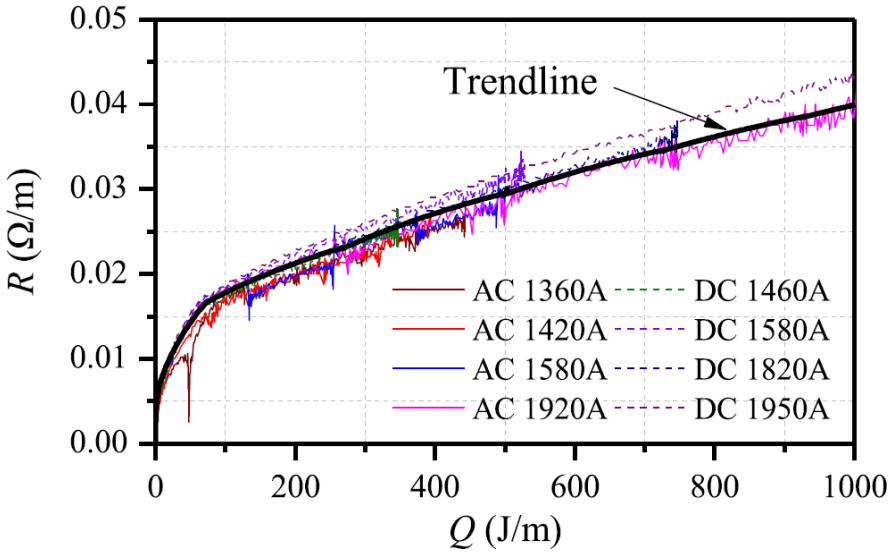

Figure 64 Second R-Q curve for different currents

These curves give sufficient information to implement a look-up-table enabling the calculation of the resistive value in a simplified way, as shown in Figure 65.

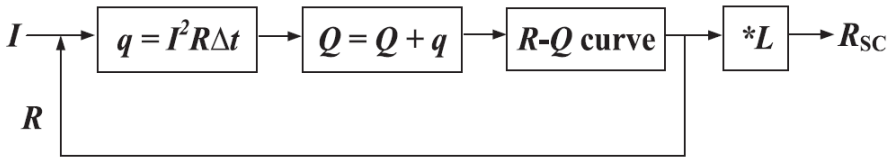

Figure 65 Resistance calculation method with R-Q curve

This model does not consider the change of electric field $E(J,T)$.

3.2.2.5 Thermal Model

Many different thermal models have been evaluated, but only one model has been selected due to is simplicity but dependence with device parameters and the availability of the required data.

The generated heat can be calculated as in Equation 38.

$$\dot{Q}_{R_{SFCL}} = R_{SFCL} \cdot I^2 \quad [W]$$

Equation 38

In the other hand, the removed heat is shown in Equation 39

$$Q_{Removed} = \frac{T - Ta}{R_{th_{SC}}} \quad [W]$$

Equation 39

Where the thermal resistance is geometrically dependant and can be calculated by Equation 40.

$$R_{th_{SC}} = \frac{1}{k \cdot L \cdot D \cdot \pi} \quad [\frac{K}{W}]$$

Equation 40

$$k\left[\frac{W}{K \cdot m^2}\right] \qquad C_v\left[\frac{J}{K \cdot m^3}\right] \rightarrow J = W \cdot s$$

Where k (The coefficient of heat transfer to cooling reservoir) and C_v (The superconductor volumetric specific heat) are thermal parameters of the superconducting material.

The total specific heat can be calculated as in Equation 41.

$$C_{sc} = L \cdot A_{sc} \cdot C_v \quad \left[\frac{J}{K}\right] = [\frac{W \cdot s}{K}]$$

Equation 41

So, the instantaneous change in temperature can be calculated as expressed in Equation 42.

$$\frac{dT}{dt} = \frac{Q_{R_{SFCL}} - Q_{removed}}{C_{sc}} \qquad \left[\frac{K}{s}\right]$$

Equation 42

Therefore, the instantaneous current will be the integral, Equation 43.

$$T(t) = \int \frac{dT}{dt} dt \qquad [K]$$

Equation 43

3.2.3 Finite Element Modelling

Finite element modelling (FEM) is a general numerical method applied to many fields in engineering and physics. FEM allows the computation of differential equations applied to

complex geometries by dividing the system into a high number of sub-domains (finite element). The only basic requirement for this method is to know the differential equation which determinates the physical phenomena.

It is commonly applied to complex simulations in the fields of heat transmission, fluid dynamics, structural mechanics, and electromagnetics. According to electromagnetics, maxwell equations are implemented to model complex electromagnetic systems.

Table 12 shows the main maxwell equations [42], there are several expressions derived from them.

Equation	Interpretation
$\vec{\nabla} \cdot \vec{E} = \frac{\rho}{\varepsilon_o}$ (1)	Gauss Law: A charge in the space generates a divergent electric field, this is, a source or a sink of electric field
$\vec{\nabla} \cdot \vec{B} = 0$ (2)	Gauss Law for magnetic field: Magnetic field divergence equals 0. No monopoles can exist, magnetic field lines close by themselves.
$\vec{\nabla} x \vec{E} = \frac{\partial \vec{B}}{\partial t}$ (3)	Faradays Law: One of the curl equations. Change in magnetic field induces rotational electric field. In the same way rotational electric field generates a change in magnetic field.
$\vec{\nabla} x \vec{B} = \mu_o \vec{J} + \mu_o \varepsilon_o \frac{\partial \vec{E}}{\partial t}$ (4)	Ampere Law: A current induces a rotational magnetic field, or a rotational magnetic field induces current. Another curl equation
$\vec{D} = [\varepsilon]\vec{E}$ & $\vec{B} = [\mu]\vec{H}$	Constitutive relations: Represent the effect of the electric and magnetic field on determined materials with a determinate ε and μ value.

Table 12 Maxwell Equations

By this method, SFCL can be evaluated in an accurate way, typical software for this porpoise can be Flux of COMSOL Multiphysics.

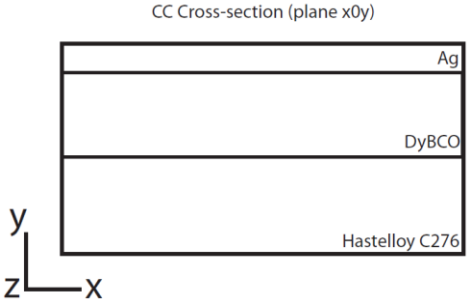

Figure 66 2D geometry of the commercial tape

In [43], a 2D geometry is defined to evaluate the thermal stability of a commercial coated HTS tape. Typically, cross section of superconductor tapes is not fully made of superconducting materials, for instance, to avoid hot spots and to stabilize the superconductor. Figure 66 [43] shows the 2D geometry of the commercial tape, composed by a thick conductive substrate made of Hastelloy C276, which is typically isolated from the superconducting material; a MgO buffer layer, a superconducting film made of DyBCO and a silver stabilizer.

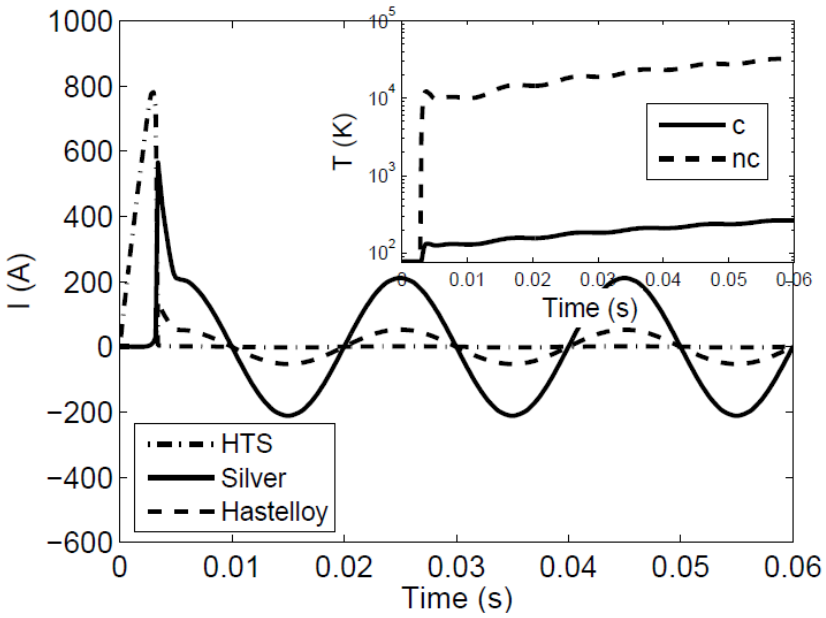

Figure 67 Current distribution through parallel paths (C shunted - NC not shunted)

By FEM, the effect of thicknesses of the different materials on thermal stability can be evaluated, considering Hastelloy C276 and silver as shunt resistances. Once the SFCL has quenched, the developed resistance is higher than the one of the parallel path, so the current will circulate to those parallel paths as observed in Figure 67 [43]. The heat should be transmitted to nitrogen environment if thermal stability and fast recovery is aimed.

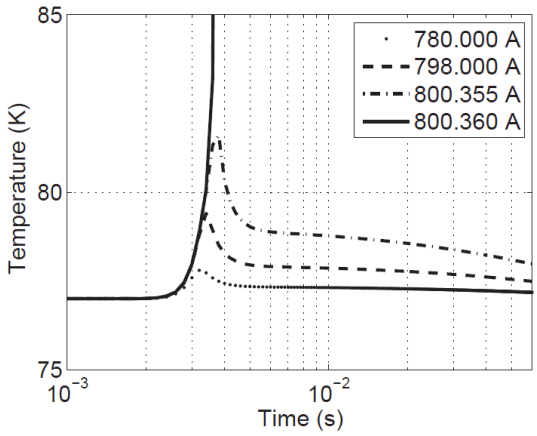

Figure 68 Thermal stability analysis

Figure 68 [43] shows the current threshold for thermal stability around 800A, for the model analysed.

3.2.4 Hardware in the Loop

Hardware in the loop (HIL) experiment is well known for testing real prototypes of the device under test (DUT) without the necessity of building a complete setup of the system to be analyse.

It is composed by the DUT (hardware) and the simulated system interconnected by an interface (in the loop). With this philosophy, the DUT is tested under real electrical conditions and the response of the system due to the DUT can be evaluated in simulation.

According to power applications, power hardware in the loop is applied (PHIL), where high voltage and current are needed. In PHIL for SFCL testing, the current limiter will be in the high voltage-current environment, whilst the simulated system will be the power system.

In Figure 69 [44] the set up for testing a 10-meter YBCO superconductor module is presented. The measured voltage across the SFCL due to the resistance development is feedbacked to the simulated system. The simulated system will respond in accordance with this voltage change across the SFCL and the simulated resulting current will be sent as reference to feeding converter.

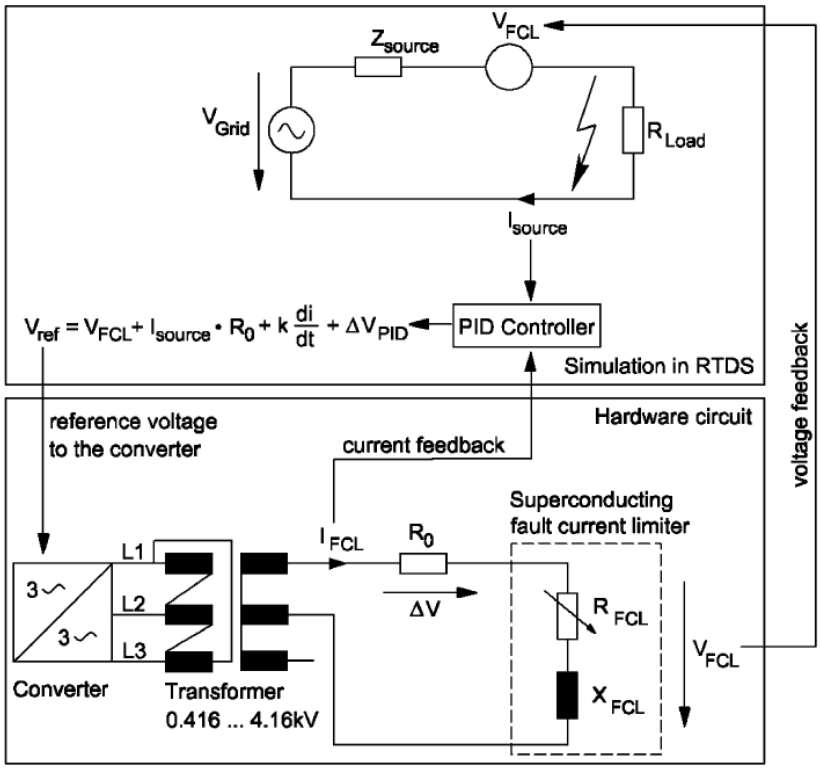

Figure 69 Conceptual PHIL setup [44]

With this approach, the transient behaviour of the SFCL can be evaluated rigorously under different conditions.

4. R-SFCL MODELS SIMULATION

To evaluate the performance of each model *MatLab&Simulink* has been employed. Step model, exponential model, magneto-thermal model, and 4th approach model based on R-Q curve have been implemented.

Figure 70 shows the basic test bed employed for testing the models; in contains case study R-SFCL model, a direct current breaker, line impedance, system load and a generic mechanical circuit breaker for emulating a short circuit with a defined fault resistance.

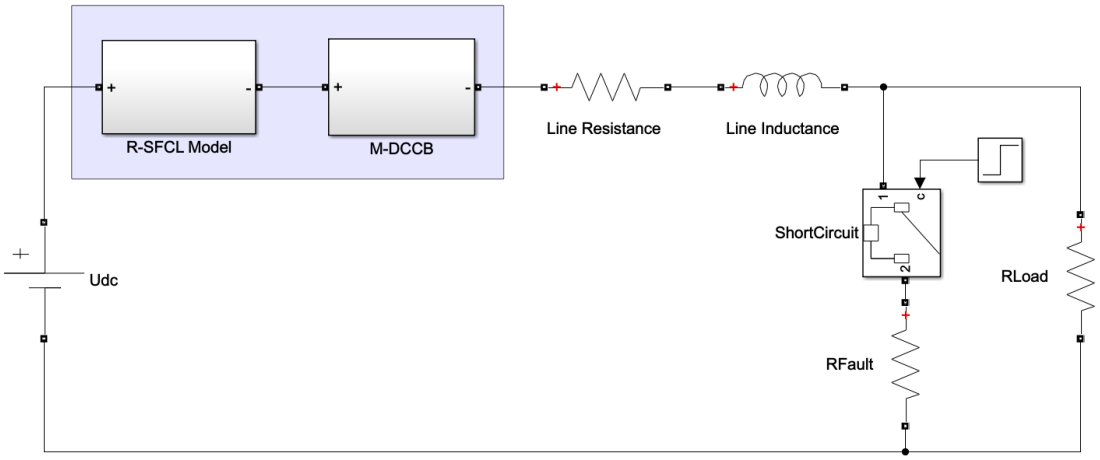

Figure 70 Basic TestBed

The model parameters are shown in Table 13:

Variable	Unit	Value
U_{dc}	$[kV]$	100
L_{line}	$[mH]$	50
R_{line}	$[\Omega]$	5
R_{load}	$[\Omega]$	250
R_{fault}	$[\Omega]$	5
t_{fault}	$[s]$	0.05
$I_{prospective}$	$[kA]$	10

Table 13 Variable values of TestBed

Figure 71 shows in detail the circuit breaker implemented for this testbed. It consists of an active current injection M-DCCB, notice that a CRL has been added to the device.

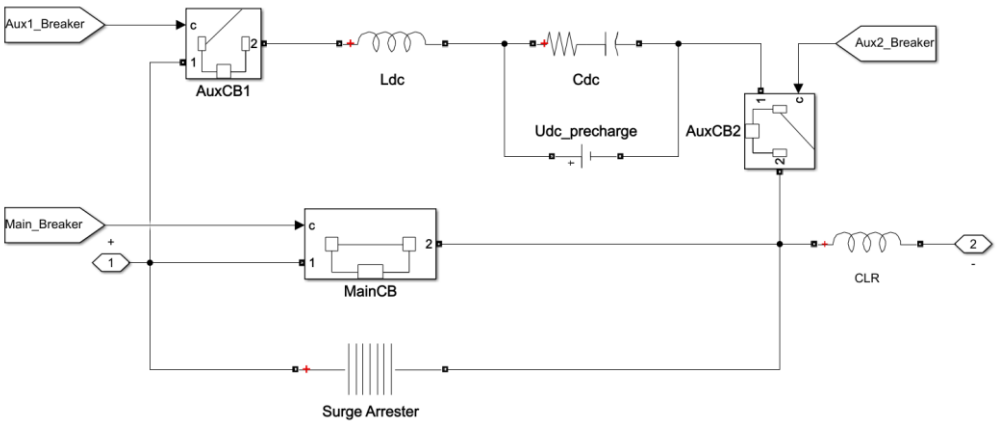

Figure 71 M-DCCB with active injection

M-DCCB parameters values are shown in Table 14.

Variable	Unit	Value
L_{dc}	$[uH]$	290
C_{dc}	$[uF]$	17.7
L_{CLR}	$[mH]$	1
$V_{SurgeArrester}$	pu	1.5
I_{crit}	$[kA]$	4
$BRK_{OP\,Delay}$	$[ms]$	17

Table 14 Parameters of the M-DCCB

4.1 Model analysis

In this first part of the model analysis, model's settings are going to be modified under the same system conditions. In this way, it can be understood the relevance of each variable and the way the model interacts with the system. Some models have much more setting that the simplest ones, as the step model, for instance. Emphasis is going to be given to critical current and fault resistance dependence on quenching dynamic.

As an example, Figure 72 shows the implementation of the step model, where the developed resistance is multiplied by the current and transformed to voltage so the systems behaves electrically as it should. All the models have the same mechanism to interact with the system.

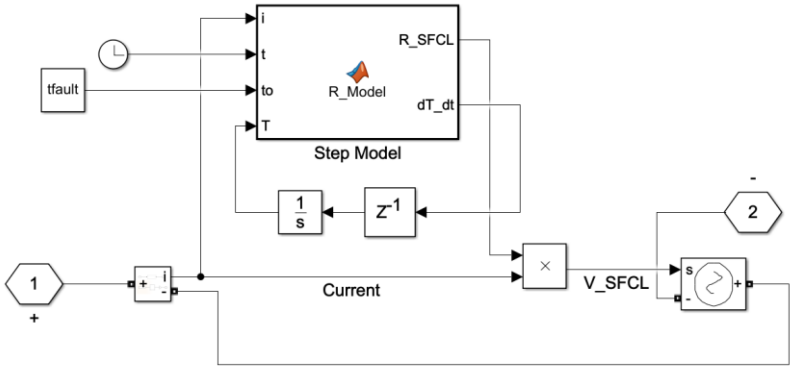

Figure 72 Step model implementation

4.1.1 Step model

Step model is going to be simulated for different device resistances and for different fault resistances and critical currents. Model settings are shown in Table 15.

Model Settings		
Variable	**Unit**	**Value**
R_{sfcl}	$[\Omega]$	15 - 30
I_c	[A]	600 - 1200

Table 15 Step model settings

Figure 73 show the behaviour of the model for different resistances, where fault current, Rsfcl variation, and voltage across current limiter and circuit breaker is depicted.

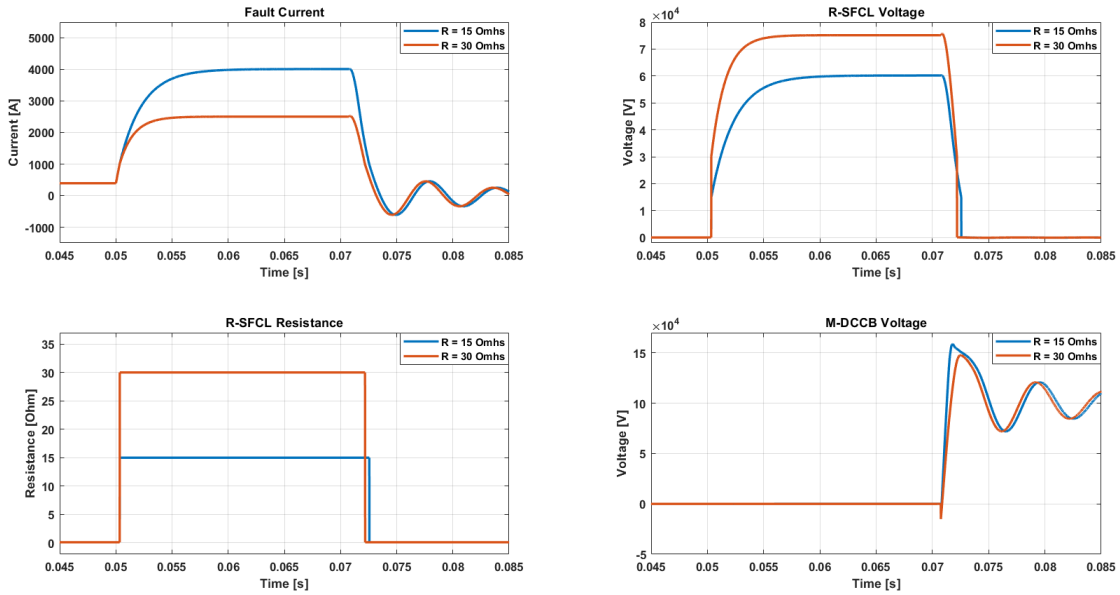

Figure 73 Step model analysis for different resistive values

Firstly, it is concluded that this model cannot be employed to evaluate the peak fault current of the study case system as the resistance is developed instantaneously, so the fault current goes from load value to final limited value directly.

Secondly and obviously, the bigger the resistance, the smaller the final fault current. This is traduced in a smaller overvoltage in circuit breaker as the total magnetic energy stored (E_L) in the system is smaller, as it is shown in Equation 44.

$$E_L = \frac{1}{2} L_{system} I_{Fault}$$

Equation 44

Next, by modifying critical current and modifying fault resistance, exactly same behaviour is obtained. This makes sense as this model quenches instantaneously once critical current is surpassed, and fault resistance and critical current value modifies very little the instant this surpass happens.

4.1.2 Exponential Model

Exponential model analysis is bases on the same philosophy. Different transition times are going to be evaluated for different fault resistances and critical currents. Model settings are shown in Table 16.

Model Settings		
Variable	**Unit**	**Value**
R_{sfcl}	$[\Omega]$	30
I_c	[A]	600 - 1200
τ	[ms]	1 – 2 – 3

Table 16 Exponential model settings

Figure 74 shows fault current and Rsfcl resistive variation for different time constant values and critical current values.

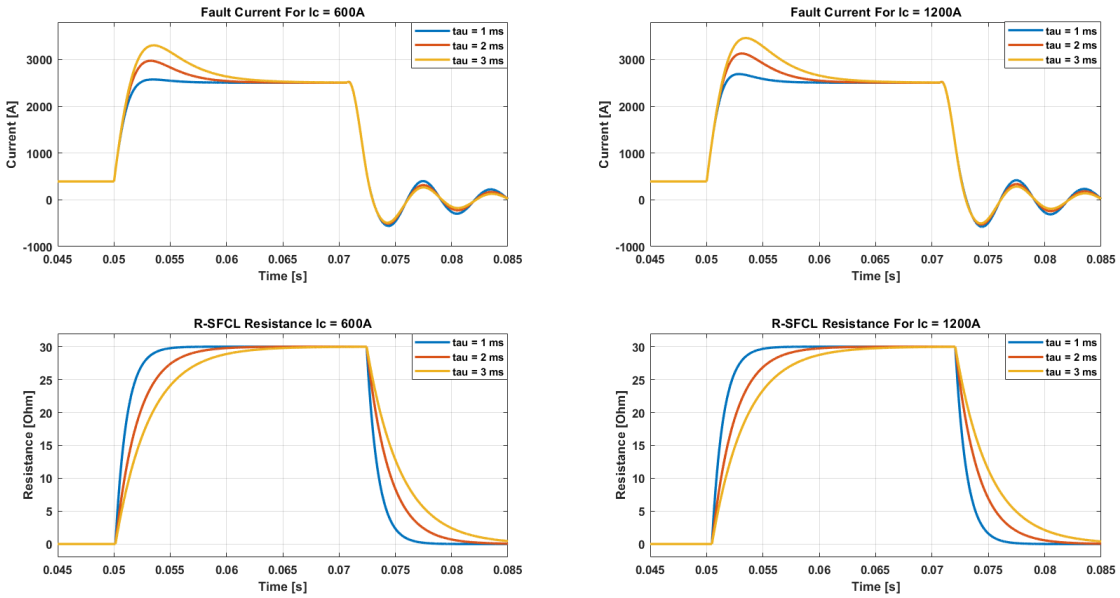

Figure 74 Exponential model analysis for different time constants and critical currents

The smaller the time constant is, the more approximated is the model to a step model, thus, the current peak is reduced.

The model is almost insensitive to critical current variation. The transition time of this model is fixed by time constant, thus, it is insensitive to different fault resistances.

Exponential model is a well-recognized model as it emulates transition time allowing peak current analyses and more realistic response of the system. However, it is still fully current dependant and transition time is fixed to all kind of scenarios, as varying fault resistance, or critical current variation.

Step model and exponential models are simplified models that may be interesting for steady state analysis.

4.1.3 R-Q model

Due to the differences of this model comparing with others, the simplified model diagram shown in Figure 65 is implemented in Figure 75, where the look up table (LUT) contains the R-Q relation shown in Figure 64. Saturation to 30 ohms has been implemented.

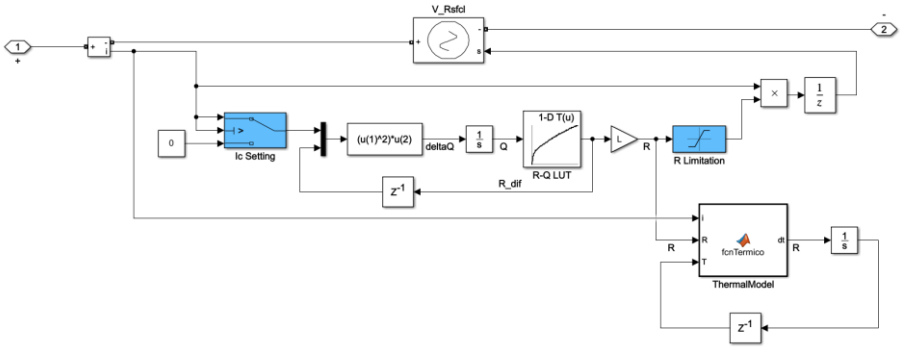

Figure 75 R-Q Model implementation

Model settings are shown in Table 17.

Model Settings		
Variable	**Unit**	**Value**
R_{sfcl}	[Ω]	30
I_c	[A]	600 - 1200
L	[km]	0.4 – 0.6 – 0.8

Table 17 RQ model settings

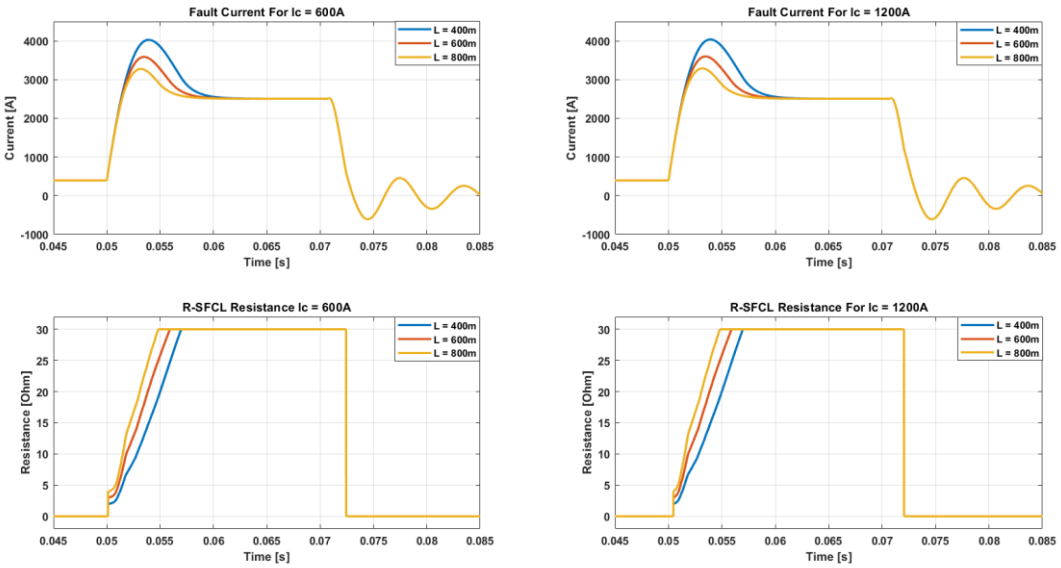

Figure 76 RQ model analysis for different length and critical current

Figure 76 shows fault current and Rsfcl variation for for different lengths and critical currents. It can be concluded that the higher the length, the faster it quenches and the smaller is the peak current value. Other side, this model is insensible to critical current variations.

However, an interesting feature of this model is that quenching transition time is fault resistance dependant, as shown in Figure 77. The higher the fault resistance value, the smaller the prospective fault current, and, thus, the model transition is slower, this behaviour is more realistic than the previous two models.

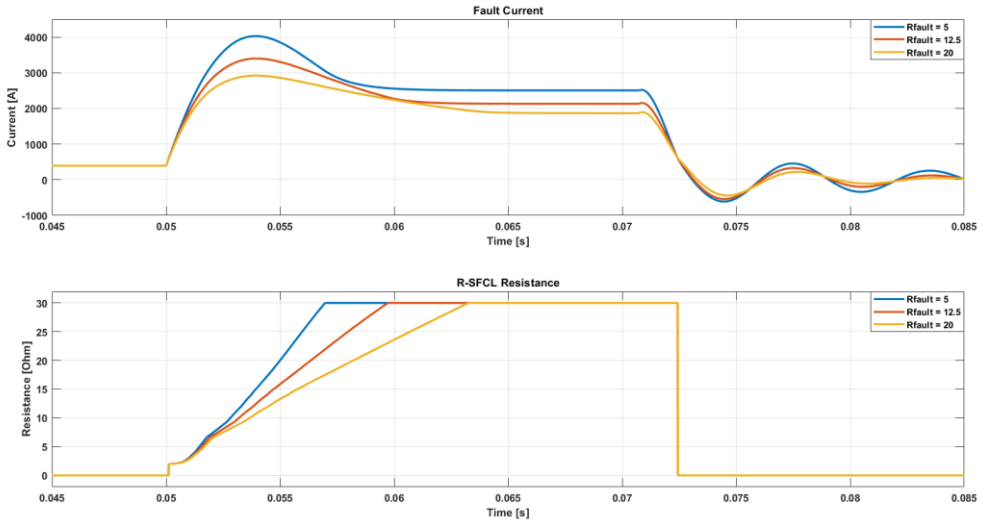

Figure 77 Fault resistance swept

Furthermore, shunt resistance analysis has been done with this model. Figure 78 shows the current, resistive value, voltage and temperature of the current limiter. Thermal model shown in 3.2.2.5 has been implemented to determine temperature. As stated in [39], when shunt resistance is added, overvoltage and maximum temperature is decreased, but the peak current increases as the equivalent resistance drops.

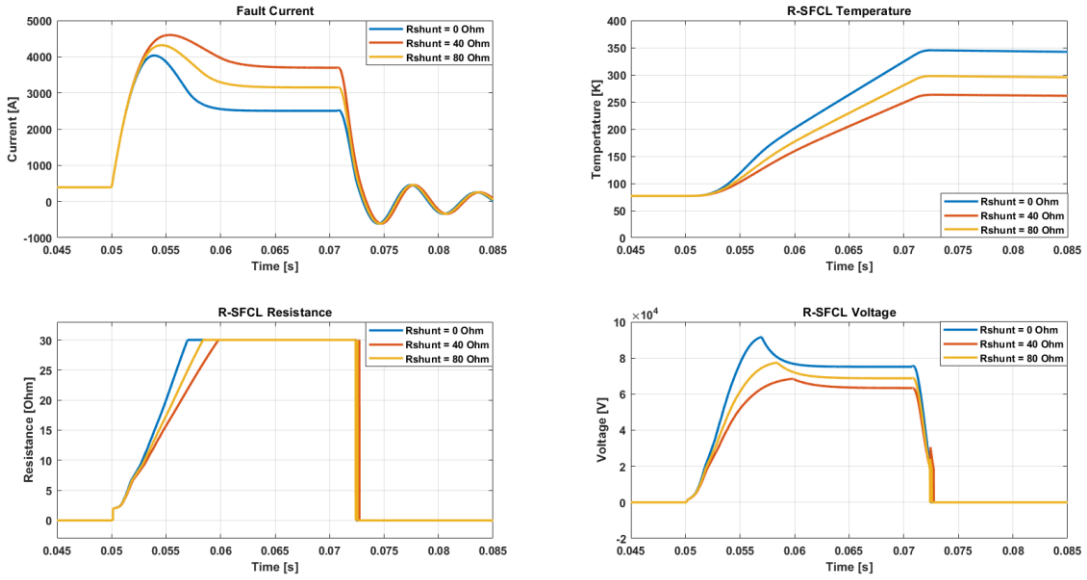

Figure 78 Shunt resistance analysis

4.1.3 Magneto thermal model

The magneto-thermal model is based on the model shown in chapter 3.2.2.3.3. Saturation to 30 ohms has been implemented, as in RQ model.

Magneto thermal model have a lot of settings, but only length and critical current is going to be assess, as well as fault resistance swept. Modified model settings are shown in Table 18.

Model Settings		
Variable	**Unit**	**Value**
R_{sfcl}	$[\Omega]$	30
I_c	[A]	300 - 600 - 1200
L	[km]	3 – 4 – 5

Table 18 Magneto Thermal model settings

Figure 79 shows the behaviour of the current limiter for different lengths and critical currents.

On the one hand, it is very remarkable that the quenching phenomena, for these model settings and DC system, is very slow. Peak current is around 5,5-6kA for all superconducting lengths when critical current is 600A, this differs considerably comparing with the previous three models.

For a critical current of 1200 A, the limiter does not even quench, and the breaking current capability is surpassed so the breaker does not open.

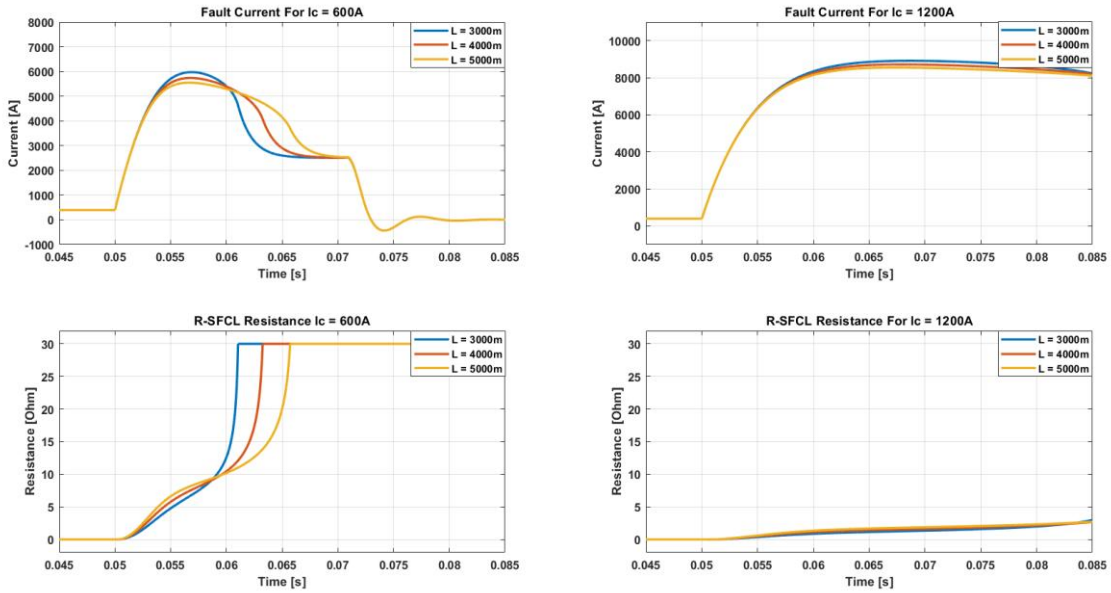

Figure 79 Magneto Thermal model analysis for different lengths and critical currents

Thus, it can be concluded that critical current has a huge impact on the quenching phenomena.

Next, fault resistance swept is implemented for a critical current of 300A. Figure 80 shows the quenching for different fault resistances, it can be concluded that fault resistance has big impact in transition time.

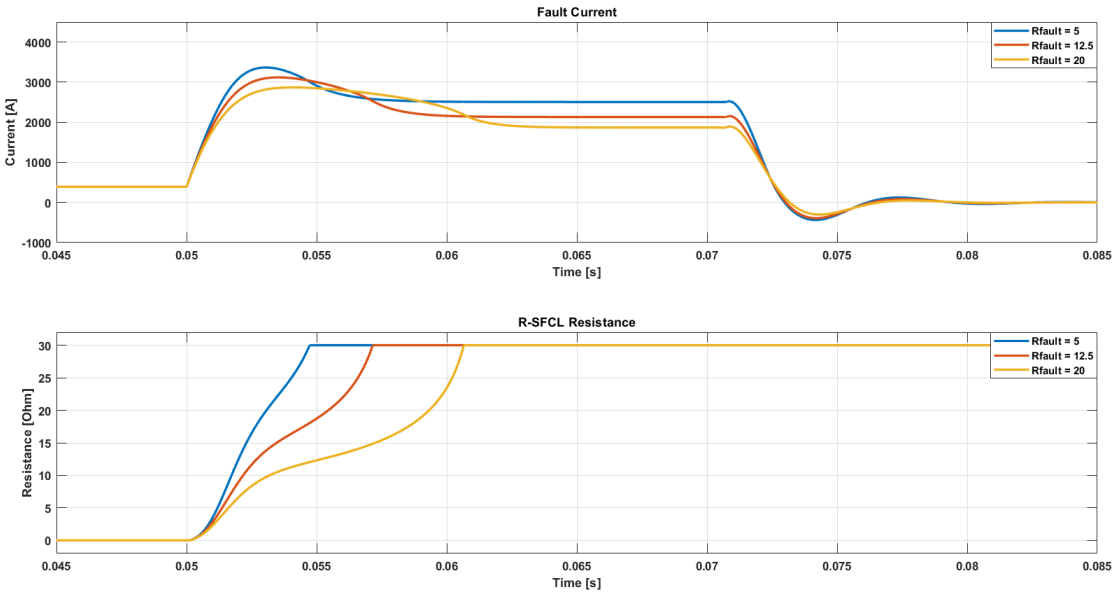

Figure 80 Fault resistance swept for Ic = 300A

4.2 Model comparison

This chapter compares the behaviour of each model. Figure 81 compares current and resistance of the four models with the settings shown in Table 19, note that critical current is the same for all the models.

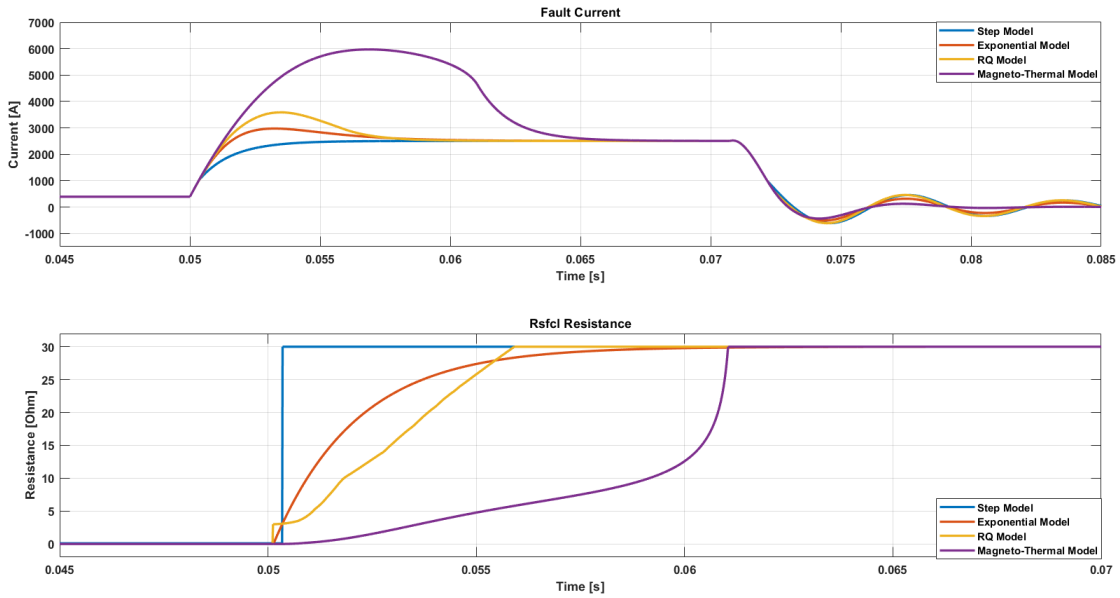

Figure 81 Superconducting fault current limiter model comparison

On the one hand, it is concluded that the behaviour of each model is very model setting dependant. The behaviour of two different models can be equalized for the same system conditions by adjusting model settings.

Model Settings		
Step Model		
Variable	**Unit**	**Value**
R_{sfcl}	[Ω]	30
I_c	[A]	600
Exponential Model		
R_{sfcl}	[Ω]	30
I_c	[A]	600
τ	$[ms]$	2
RQ Model		
R_{sfcl}	[Ω]	30
I_c	[A]	600
L	[km]	0.6
Magneto Thermal		
R_{sfcl}	[Ω]	30
I_c	[A]	600
L	[km]	3

Table 19 Model settings for comparison

On the other hand, it has been appreciated that exponential and step models are insensitive to system variations, as fault resistance, whilst RQ and magneto thermal are sensible to this variable. Figure 82 shows the current and resistance evolution for different fault resistances for exponential, RQ and magneto thermal model.

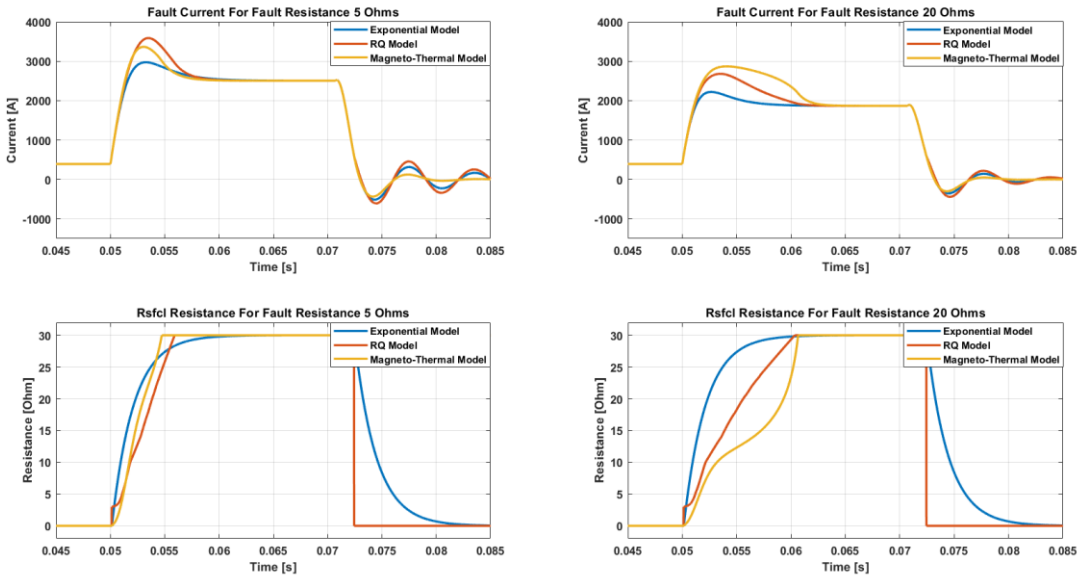

Figure 82 Model comparison for different fault resistances (Ic@MagnetoThermal = 300A)

It is appreciated how the quenching phenomena differs for different fault resistances.

Limiting factor is defines as in Equation 45, which is going to be used to evaluate the current reduction in the simulations from now on.

$$LF = \frac{I_{prospective}}{I_{limited}} 100$$

Equation 45

Figure 83 shows peak currents and limiting factors for different fault resistance values and for exponential, RQ and magneto thermal model. It can be concluded that peak and limiting factor evolve different depending on the model.

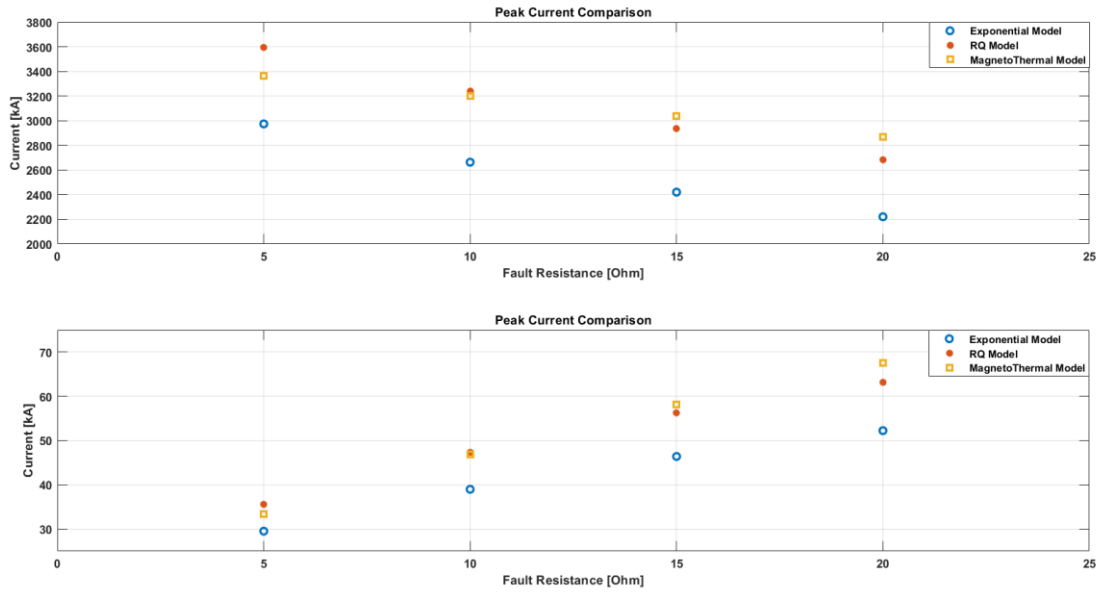

Figure 83 Peak current and limiting factor for different fault resistances

5. MULTITERMINAL HVDC SYSTEM SIMULATION

The main objective of this project is to evaluate the multiterminal HVDC system response once the R-SFCL device is integrated.

The system utilized is the one depicted in Figure 84. It consists of two converter (converter 1 and converter 2) connected to offshore AC wind farms, that feeds two onshore converters (converter 3 and converter 4) connected to the mainland AC grid. The system configuration is a symmetric monopolar with a ± 320Kv DC voltage. All the converters are MMC.

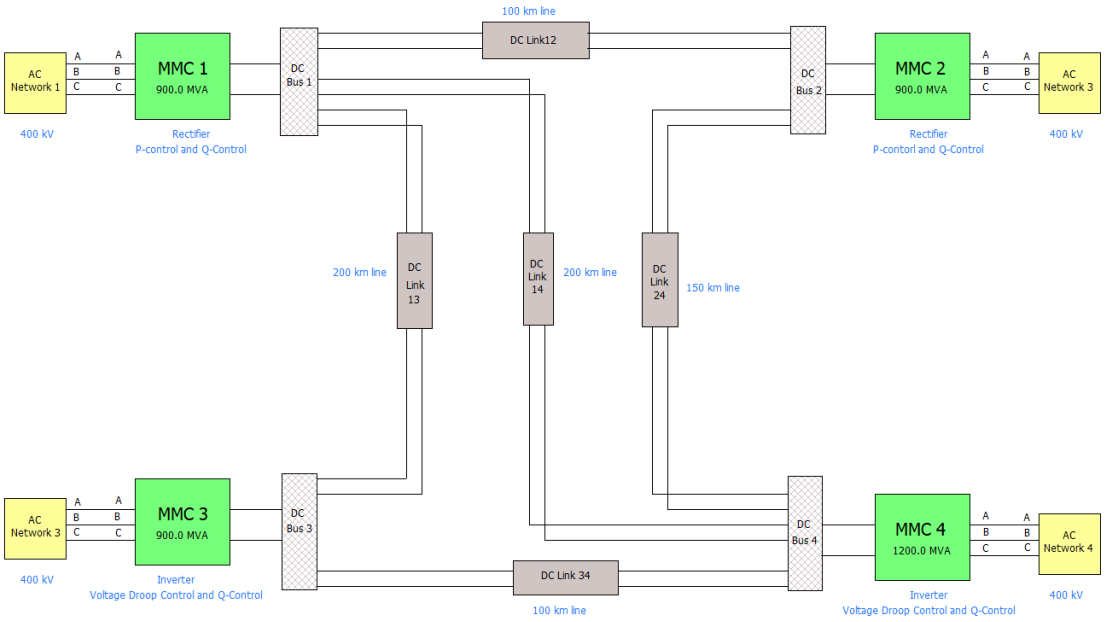

Figure 84 MTDC test system

The main parameters of the test system are shown in Table 20.

	Converter 1,2,3	Converter 4	Unit
Rated Power	900	1200	[MVA]
Rated DC voltage	± 320	± 320	[kV]
Rated DC Current	1.406	1.875	[kA]
IGBT Blocking Current	2.1 (1.5pu)	2.1 (1.12pu)	[kA]
AC Grid Voltage	400	400	[kV]
AC Converter Voltage	380	380	[kV]
Transformer Zpu	0.15	0.15	[pu]
AC Grid Reactance X_{ac}	17.7	13.4	[Ω]
AC Grid Reactance R_{ac}	1.77	1.34	[Ω]
Arm Capacitance C_{arm}	29.3	39	$[\mu F]$
Arm Reactor L_{arm}	84.8	63.6	$[mH]$
Arm Resistance L_{arm}	0.885	0.67	[Ω]
Bus Filter Reactor	10	10	$[mH]$

Table 20 MTDC system parameters

Converter control consists of inner current loops based on dq transformation which control active and reactive power, respectively. Negative current loops are set to zero to avoid unbalanced conditions. Converters 1 and 2 control active power to maintain wind power system stability and converters 3 and 4 control direct voltage level.

A simulation is carried out to evaluate the system behaviour without fault conditions and the power flow. On the one hand, Table 21 shows the variables of each converter.

CONVERTER [Nº]	BUS VOLTAGE [kV]	BUS TOTAL CURRENT [kA]	TOTAL POWER [MW]
1	642.45	1.085	695.3
2	643.667	1.079	694.03
3	638.71	-1.201	-767.38
4	640.2	-0.928	-593.62

Table 21 MTDC converter's variables

On the other hand, Table 22 shows the variables of each line.

LINE	POSITIVE CURRENT DIRECTION	OUTPUT CURRENT AMPLITUDE [kA]	POWER IN LINE ENDS [MW]	POWER LOSSES [kW]
12	From 2 to 1	-0.2239	$P_{out2} = 144.11\ MW$ $P_{in1} = 143.84\ MW$	270
13	From 1 to 3	0.7701	$P_{out1} = 494.75\ MW$ $P_{in3} = 491.87\ MW$	2880
14	From 1 to 4	0.534	$P_{out1} = 343.06\ MW$ $P_{in4} = 341.86\ MW$	1200
24	From 2 to 4	-0.8521	$P_{out2} = 548.46\ MW$ $P_{in4} = 545.51\ MW$	2950
34	From 4 to 3	0.4468	$P_{out4} = 286.04\ MW$ $P_{in3} = 285.37\ MW$	670

Table 22 MTDC line's variables

Figure 85 depicts the power- current flow, and voltage level on each converter. It can be observed that the system is not operating at maximum power level.

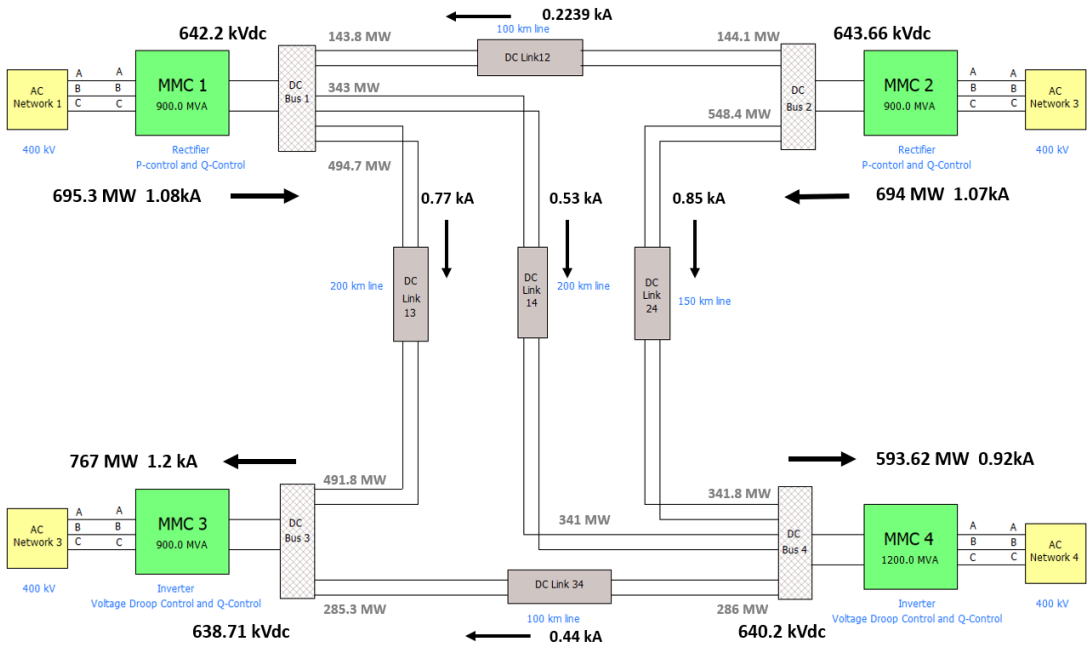

Figure 85 System variable illustration

5.1 MTDC Fault Phenomena

To understand and quantify the benefits of implementing R-SFCL in MTDC, in this section pole to pole and pole to ground permanent faults are going to be simulated and prospective currents for different fault resistances are going to be measured.

Pole to pole and pole to ground fault are going to be simulated in the positive pole of the link 12, next to bus 1 (km = 0).

5.1.1 Pole to pole permanent fault

Figure 86 shows DC bus 1 positive pole currents and voltages in the fault condition stated in 5.1. When pole to pole fault occurs, current through faulted line rise drastically and very fast. Voltage of faulted line poles drops instantaneously to 0 and so does the other voltages next.

Figure 87 shows the behaviour of the system from a converter level point of view. All the converters feed the fault and all the bus voltages drops nearly to 0, as the simulated fault has 0 resistance.

Power flow of all the system stops and all the converters and lines withstand huge current levels.

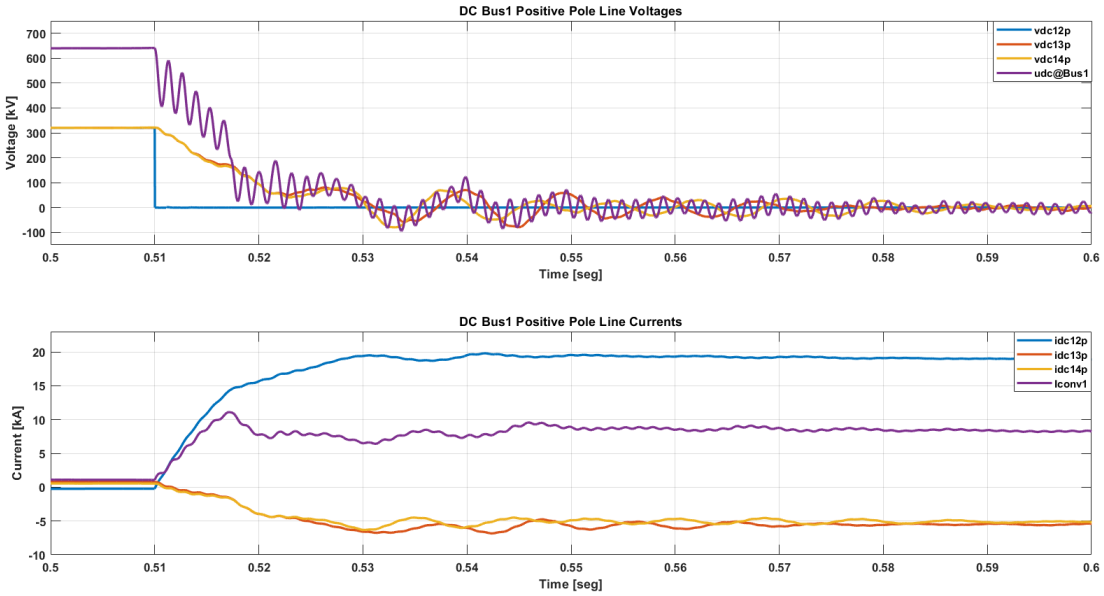

Figure 86 DC Bus 1 Positive pole currents and voltages when permanent pole to pole occurs

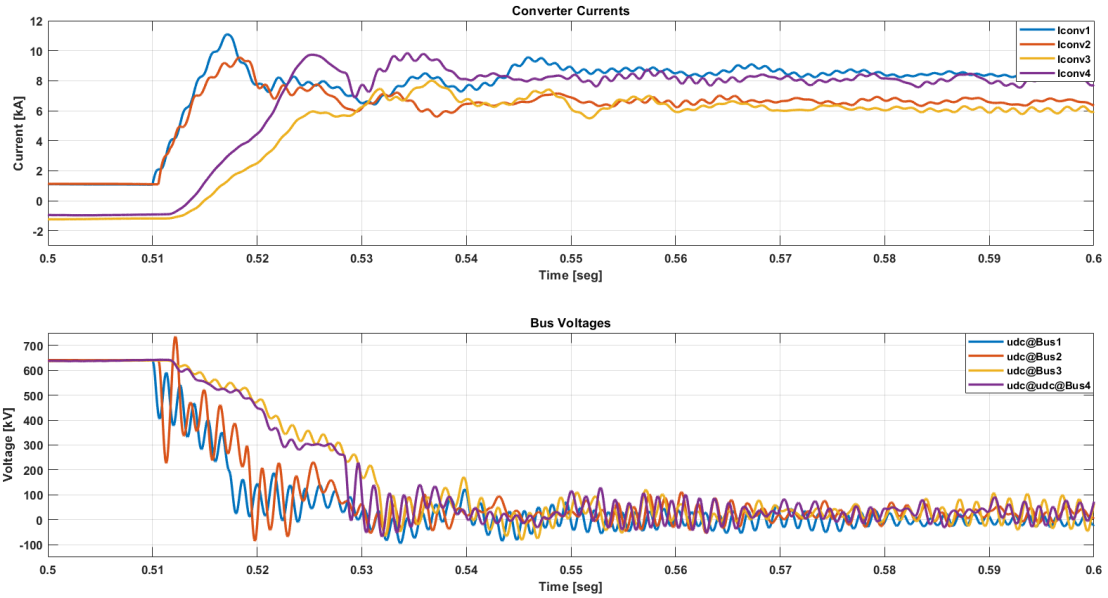

Figure 87 Converter currents and BUS voltages when permanent pole to pole occurs

5.1.2 Pole to ground permanent fault

The behaviour of this fault type differs radically from pole to pole one, since there is no permanent fault current and pole to pole voltages stay at nominal value.

Figure 88 shows DC bus 1 positive pole currents and voltages when permanent pole to ground fault occurs in the conditions stated in 5.1. It can be appreciated how when fault occurs, there is a transient current, but after a while previous current flow recovers.

According to voltages, faulted pole drops to 0 but ground voltage equals faulted pole voltage level, so pole to ground voltage of sane pole equals previous pole to pole level. Thus, pole to pole voltages stays at its nominal value.

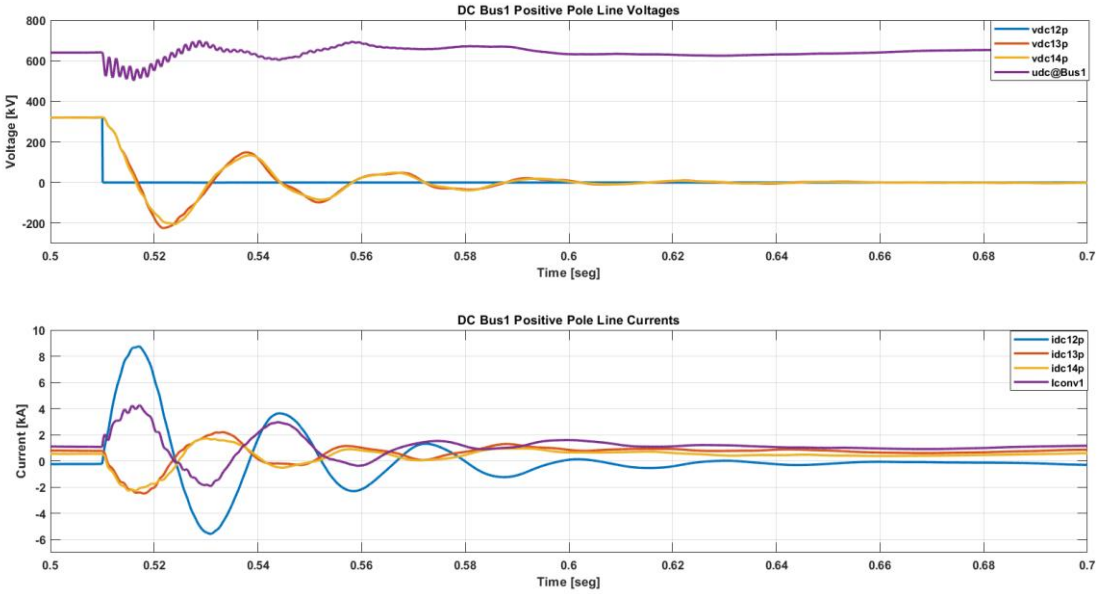

Figure 88 DC Bus 1 Positive pole currents and voltages when permanent pole to ground occurs

From a converter level point of view, Figure 89 shows all converter currents and bus voltage levels. All converters suffer from high transient peak currents, but at the steady state the current flow recovers. All bus voltages suffer from transitory oscillations, but steady state voltage is the nominal.

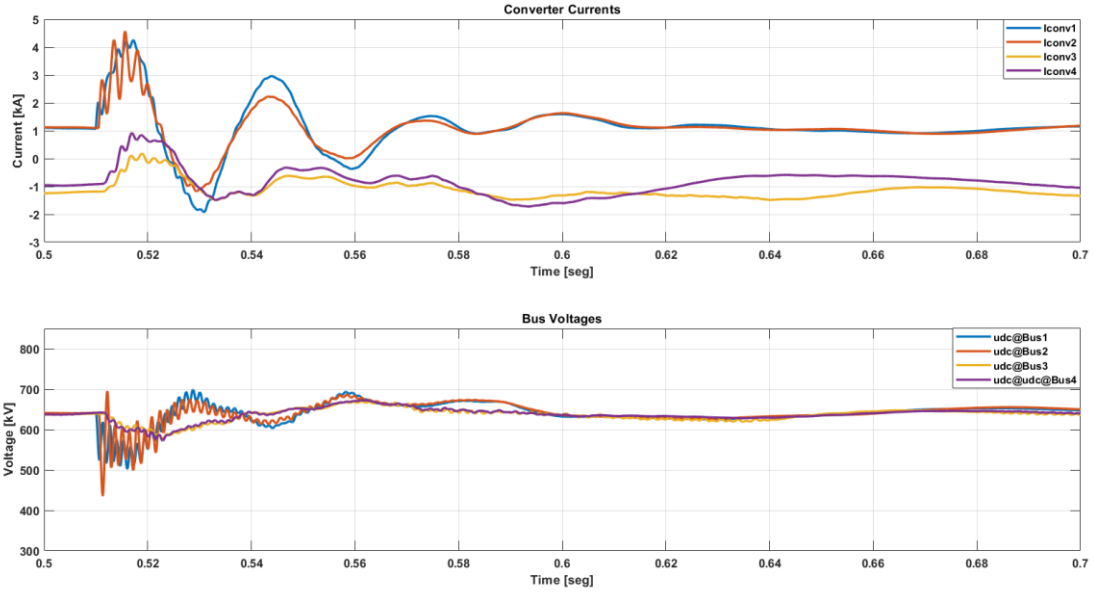

Figure 89 Converter currents and BUS voltages when permanent pole to ground occurs

5.2 MTDC System Response With R-SFCL

For evaluating the advantages of implementing superconducting current limiter, RQ model has been implemented in PSCAD. Model settings are shown in Table 23.

Model Settings		
Variable	**Unit**	**Value**
R_{sfcl}	[Ω]	80
I_c	[kA]	2

L	[km]	4

Table 23 RQ model settings for PSCAD

5.2.1 Pole to pole fault with R-SFCL

Figure 90 and Figure 91 show the improvement of system response when pole to pole fault occur.

In Figure 90 it can be appreciated how few milliseconds after the fault occurrence, the resistance of the R-SFCL develops and current gets limited all the lines connected to that bus. After the breaker tripping, only faulted line is isolated and all the currents through DC Bus 1 positive pole (and negative pole) converges to a similar value to the previous one. All system variables show an oscillatory behaviour after thre tripping of the CB towards the steady state.

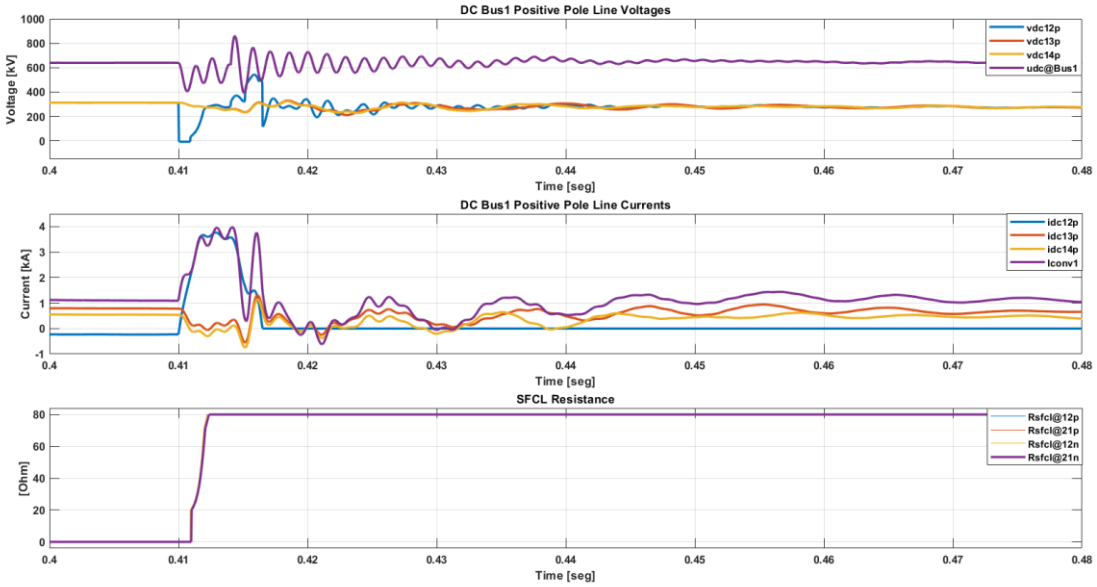

Figure 90 Positive pole currents and voltages with R-SFCL for pole to pole fault

All converter currents get limited comparing with the no R-SFCL scenario, especially converter 1 and converter 2. All the buses suffer transitory oscillations but after a while the nominal value is maintained, as depicted in Figure 91.

Figure 92 shows peak current and limiting factor for converter 1 and 2 for a fault resistance swept between 0 and 50 ohms. It can be concluded that fault current is limited for all fault resistance scenarios as the resistive current limiter develops resistance fast enough.

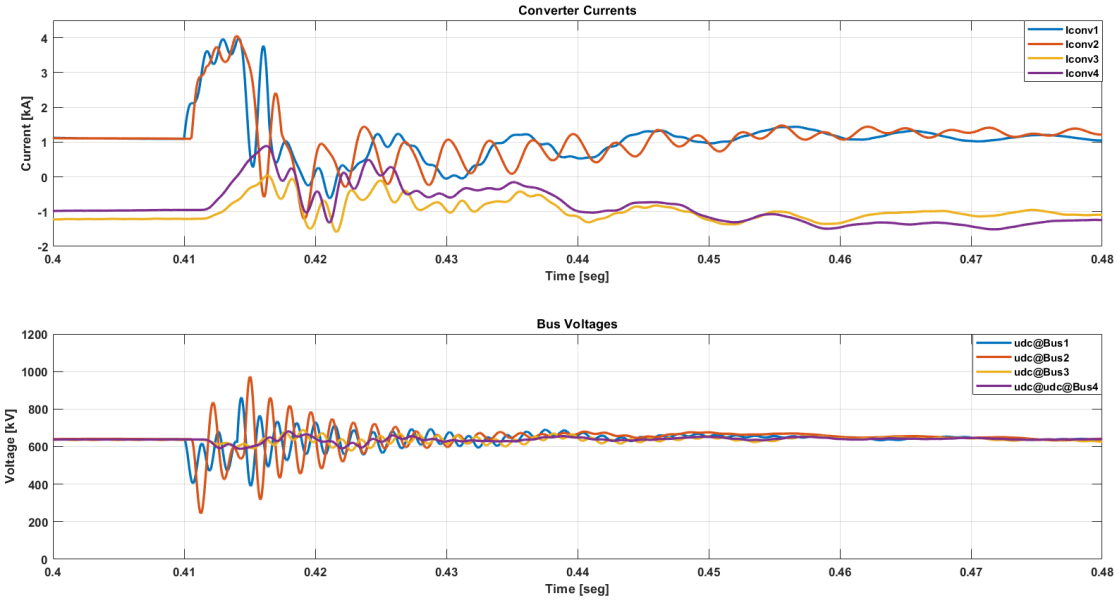

Figure 91 Converter currents and BUS voltages with R-SFCL for pole to pole fault

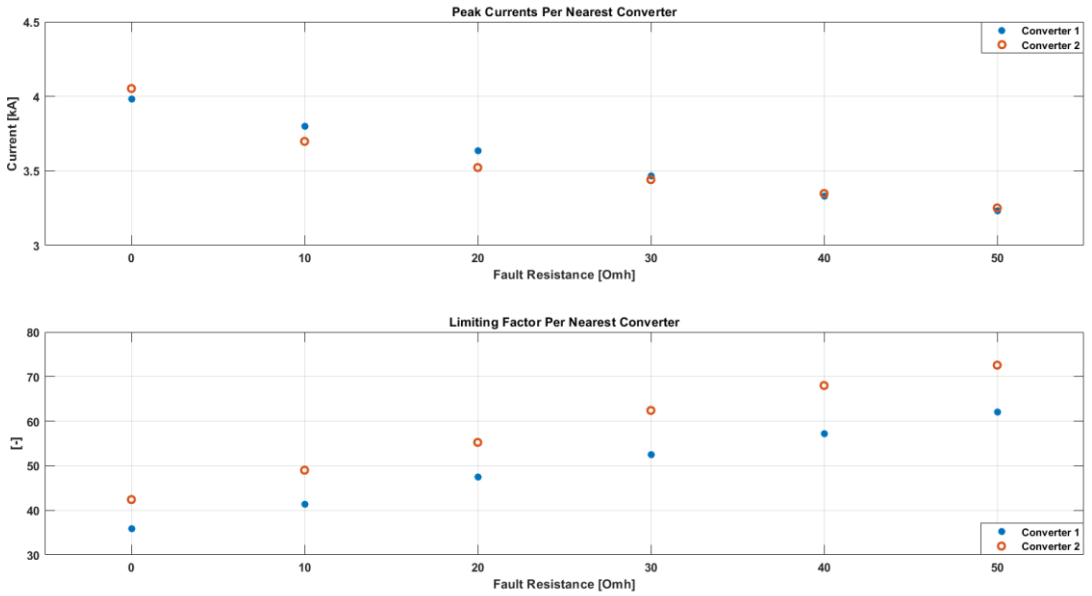

Figure 92 Peak current reduction per converter for pole to pole fault

Figure 93 shows three different scenarios: prospective current, current interruption without current limiter and current interruption with current limiter. The integration of the Rsfcl into the system reduces the breaking requirement for the CB from 9.23kA to 3.56kA.

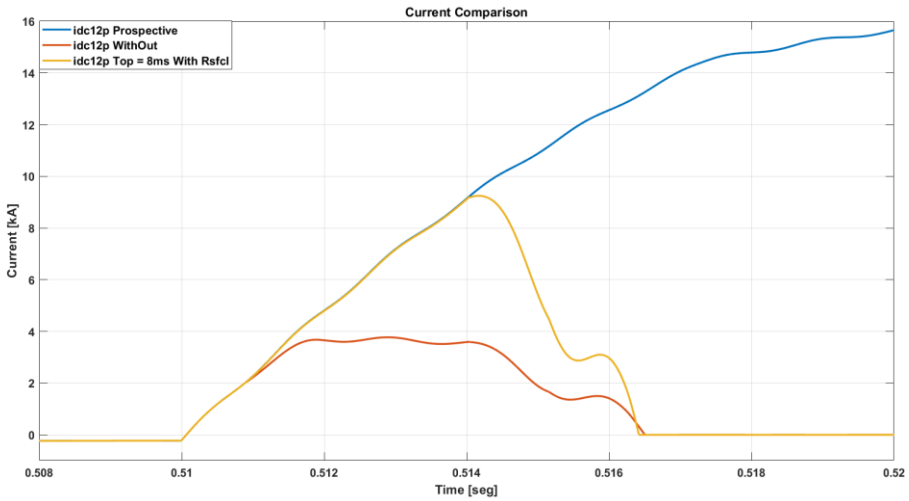

Figure 93 Current comparison for pole to pole fault

5.2.2 Pole to ground fault with R-SFCL

Figure 94 shows DC Bus 1 positive pole voltages and currents when pole to ground fault occurs. Current through line 12 is limited considerably. After the fault clearing, it is noticed that pole to ground voltages get permanently unbalanced. An advanced control should be implemented to correct this unbalance.

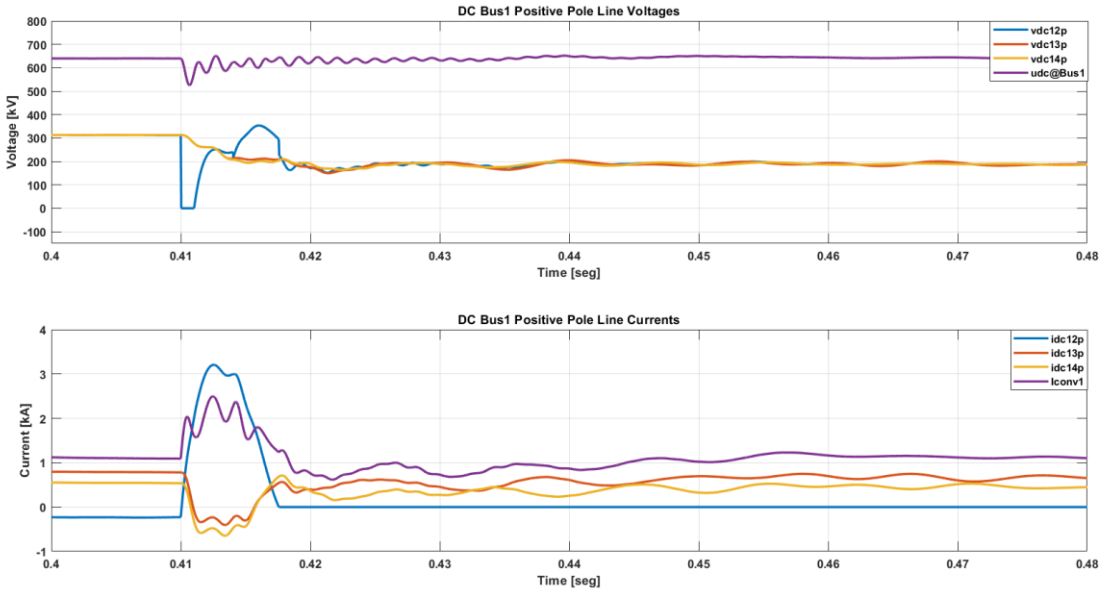

Figure 94 DC Bus 1 Positive pole currents and voltages with R-SFCL for pole to ground fault

According to converter level, Figure 95 depicts the current reduction provided by each converter. After fault clearance, current values converge to a similar value to the previous one.

Table 24 shows peak current with and without current limiter and limiting factor.

	Converter 1	Converter 2
Peak current without R-SFCL [kA]	4.25	4.57
Peak current with R-SFCL [kA]	2.49	2.94
Limiting Factor [%]	58	57

Table 24 Current peak reduction and limiting factor

Regarding bus voltages, DC bus 2 shows a permanent overvoltage.

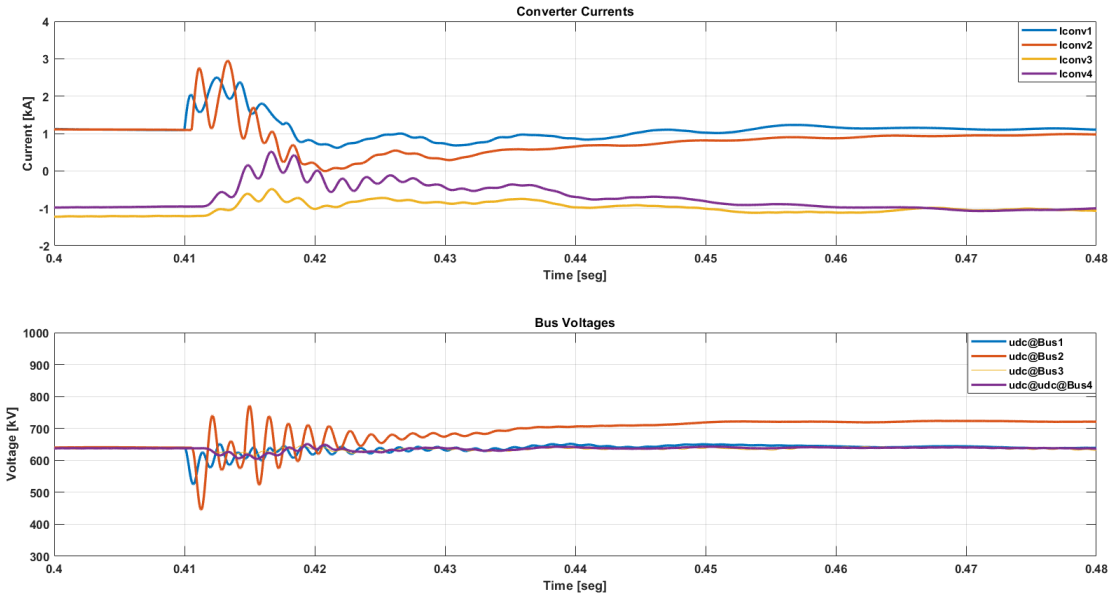

Figure 95 Converter currents and BUS voltages with R-SFCL for pole to ground fault

Figure 96 compares the same three scenarios as in pole to pole fault. The breaking requirement of the breaker for pole to ground fault is reduced from 7 .34kA to 2.99kA.

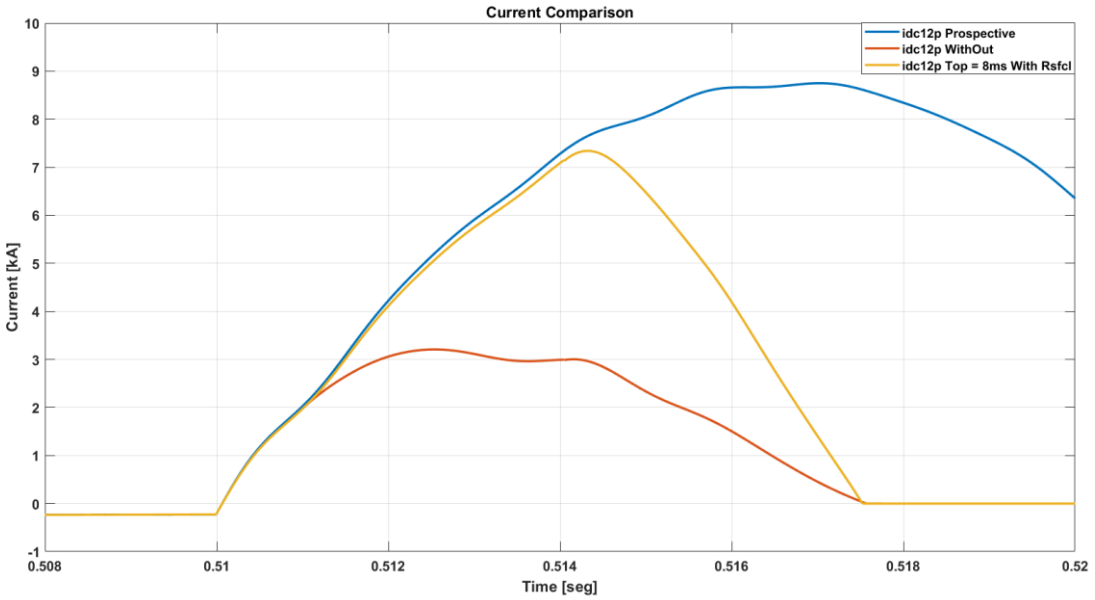

Figure 96 Current comparison for pole to ground fault

It can be concluded that the addition of R-SFCL reduced the stress of the converters, fault currents through system lines and reduces the breaking capability requirement of the DC breakers.

6. CONCLUSIONS

During the realization of this project several ideas and conclusions have been extracted.

On the one hand, HVDC lines and grids are considered as very appropriate for long distance transmission and underground and underwater transmission applications, especially for integrating offshore wind power generation. VSC converters are seen as a more appropriate technology for implementing HVDC grids. The implementation of HVDC grids, for instance interconnecting the existing HVDC point to point lines, have several benefits but it is still limited due troublesome of the fault current.

On the other hand, current limiters, especially superconducting resistive type, are considered as promising devices to conditionate the system response to the CB breaking capability. Four different Rsfcl have been evaluated. It has been concluded that step and exponential model are insensitive to fault resistance variations, whilst RQ and magneto thermal quenching time depends on this system variable. Magneto thermal model is the more accurate model since its response depends on many real design parameters.

According PSCAD simulations of MTDC with RQ model, it has been concluded that integration of a Rsfcl brings several advantages. Fault currents through converters and lines are reduced and reduces substantially the breaking capability and opening time of the DCCB. It is extremely important to make a good design of the Rsfcl, so it quenches fast enough and develops the appropriate resistive value. The appropriate setting of transition time and final resistance depends on the system parameters.

7. FUTURE WORKS

Some further developments have been detected.

According to the magneto thermal model, it would be interesting to make a real design and parameter setting following the design criteria developed in this project and evaluate the system response in a basic DC testbed. In this way, the design could be optimized to have the desired Rsfcl response.

According to thermal model, hotspot analysis could be carried out to evaluate the influence of the asymmetries of the critical current through the Rsfcl.

With the use of RQ look up table, assuming a reverse behaviour of the quenching, a more accurate recovery could be modelled. This model could be used to evaluate if the resistance of the device is low enough for making the reclose of the CB safely.

Regarding PSCAD simulations, other types of faults could be simulated to quantify the current reduction for all type of scenarios.

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