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Mitigation of Common Mode Voltage Issues in Electric Vehicle Drive Systems by Means of an Alternative AC-Decoupling Power Converter Topology

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Abstract: Electric vehicles (EV) are gaining popularity due to current environmental concerns. The electric drive, which is constituted by a power converter and an electric machine, is one of the main elements of the EV. Such machines suffer from common mode voltage (CMV) effects. The CMV introduces leakage currents through the bearings, leading to premature failures and reducing the propulsion system life cycles. As future EV power converters will rely on wide bandgap semiconductors with high switching frequency operation, CMV problems will become more prevalent, making the research on CMV mitigation strategies more relevant. A variety of CMV reduction methods can be found in the scientific literature, such as the inclusion of dedicated filters and the implementation of specific modulation techniques. However, alternative power converter topologies can also be introduced for CMV mitigation. The majority of such power converters for CMV mitigation are single-phase topologies intended for photovoltaic applications; thus, solutions in the form of three-phase topologies that could be applied to EVs are very limited. Considering all these, this paper proposes alternative three-phase topologies that could be exploited in EV applications. Their performance is compared with other existing proposals, providing a clear picture of the available alternatives, emphasizing their merits and drawbacks. From this comprehensive study, the benefits of a novel AC-decoupling topology is demonstrated. Moreover, an adequate modulation technique is also investigated in order to exploit the benefits of this topology while considering a trade-off between CMV mitigation, efficiency, and total harmonic distortion (THD). In order to extend the results of the study close to the real application, the performance of the proposed AC-decoupling topology is simulated using a complete and accurate EV model (including vehicle dynamics and a detailed propulsion system model) by means of state-of-the-art digital real-time simulation.

Keywords: EV; power conversion topologies; CMV; THD; efficiency; modulation

1. Introduction

In order to reduce pollution in urban areas, mitigate the consequences of climate change, and overcome current fuel scarcity, significant efforts are being carried out by the scientific community to contribute to the development of a more sustainable transportation [1–3]. In this context, the electric vehicle (EV) is considered as a key technology, where the battery pack, power converter, and electric machine are its most relevant elements [3–5].

The reliability of EV propulsion system components is a topic of interest for the industry and academia, as it is directly related to the vehicle maintenance costs and lifespan. In this context, one of the main problems in current electric drives is the common mode voltage (CMV). In particular,

the commutations of the power converter devices generate significant high-frequency CMV variations (Figure 1a). As a result, these voltage variations can produce not only high electromagnetic interferences (EMI) [6–8], but also shaft voltages (Figure 1b) in the electric machine [9–11], producing new capacitive paths [10]. These paths result in high-frequency leakage currents (Figure 1c) circulating through the motor bearings [12–14]. The most relevant capacitive paths are depicted in Figure 2, where the most significant bearing currents produced by CMV are the capacitive currents, electrostatic discharge currents, circulating currents, and rotor ground currents [9,13]. As bearings are critical components for the electric machine [10], a number of industrial companies are currently analyzing the degradation problems generated by such bearing currents [15–17].

Regarding this issue, it is important to remark that although the majority of current industrial solutions rely on silicon-based semiconductor technologies [18], the progressive introduction of new wide bandgap (WBG) semiconductor devices in automotive power converters is expected [19]. This will allow significantly increasing the operating switching frequencies when compared to conventional insulated gate bipolar transistor (IGBT) based Si technologies. As a consequence, CMV-derived issues will become more prevalent, as the faster switching will introduce faster CMV variations over time (dv/dt) [9–11,20].

Considering all the previous, mitigation of CMV in electric drives has become a relevant research topic for the scientific community and the industry [6,7,21–23]. In this context, the inclusion of dedicated filters (passive or active) [21,23,24] and the implementation of specific modulation techniques [21,24–26] are widespread CMV reduction solutions.

Alternatively, it is possible to use specific power conversion topologies (derivatives from the conventional two-level three-phase inverter topology) to achieve the same goals. For example, multilevel converters offer a high number of switching states (or degrees of freedom) that can be used to reduce or eliminate CMV [7,27–29]. However, multilevel technology has virtually no penetration in the EV market, as current battery pack voltage levels [30] are not high enough to justify their usage. The increase of voltage levels poses drawbacks in terms of device count, complexity in implementation, and additional costs [31]. Thus, the automotive industry continues relying on two-level solutions.
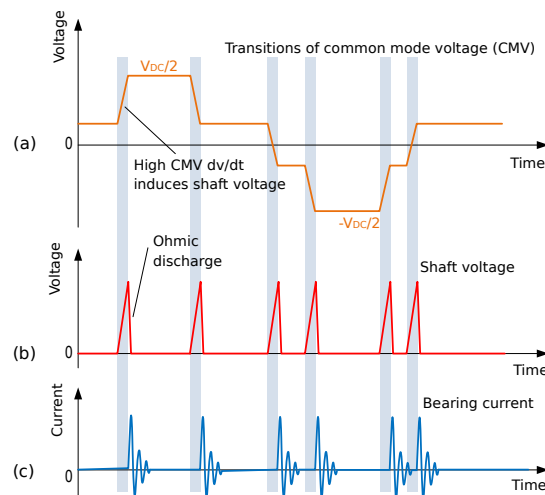

Figure 1. Common mode voltage (**a**), voltage accumulation on the electric machine shaft (**b**) and leakage current through the bearing (**c**).

The introduction of novel converter topologies is a common approach in non-isolated photovoltaic systems, and a number of single-phase (Table 1) and three-phase topologies have been proposed for CMV reduction in such applications [32–37]. As two-level three-phase technologies are dominant in EV propulsion systems [38], single-phase photovoltaic topologies cannot be directly used for vehicle propulsion systems. However, their underlying concepts can be used to propose equivalent two-level three-phase alternatives.

Table 1. Non-isolated single-phase topologies for photovoltaic applications.

Item	Topology					
	Full-Bridge (unipolar modulation)	Full-Bridge (bipolar modulation)	H5	H6D2	HBZVR-D	HERIC
Switches	4	4	5	6	5	6
Capacitors	1	1	1	2	2	1
Diodes	0	0	0	2	6	2
Efficiency	✓	✗	✓	✓	✓	✓✓
CMV	✗	✓✓	✗	✓✓	✓✓	✓
Leakage current	✗✗	✓	✓✓	✓✓	✓✓	✓✓
Advantages	High efficiency	Constant CMV, low leakage current	Low current ripple	Constant CMV, low leakage current	Very low leakage current, high efficiency	Without losses during freewheeling, high efficiency
Disadvantages	High leakage current	Very high current ripple, impaired signal quality, 2 voltage levels, low efficiency	Losses during freewheeling, high switching losses, variable CMV	High conduction losses	Bipolar output voltage due to dead time between driving and freewheeling mode	Injection of reactive power to the grid, floating CMV
References	[32–34]	[32,33]	[32,33,35,36]	[32,35,36]	[32,34,36]	[32–35]
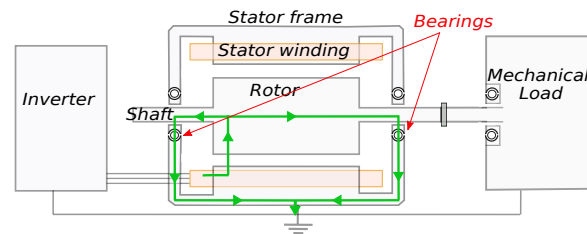
(**a**) Electric discharge machining (EDM) bearing current paths.
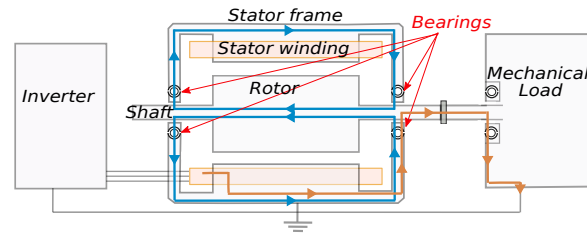
(**b**) Current paths derived from the common mode current.

Figure 2. Possible paths where bearing currents can flow through the electric machine.

Taking all the latter into account, this work will initially review conventional and CMV mitigation modulation techniques applied to two-level three-phase voltage source inverters (VSI) (as such modulation techniques and their derivatives will be used in this work for the control of the proposed topologies). After that, the state-of-the-art of alternative two-level three-phase converter topologies for CMV mitigation will be reviewed. Additionally, a series of novel topologies that adapt single-phase photovoltaic concepts into the three-phase context for their application in the EV will be proposed. Their performance (in terms of CMV, power losses, total harmonic distortion (THD), DC-link current ripple, etc.) will be quantitatively compared with other existing solutions by means of simulation. From this detailed analysis, the benefits of one of the proposals will be demonstrated, and the influence of various modulation techniques will be studied for this particular topology, resulting in effective hybrid modulation techniques. Finally, the performance of such a topology during realistic driving conditions will be simulated using a complete EV model (including vehicle dynamics and a detailed propulsion system model) by means of state-of-the-art digital real-time simulation, obtaining a clear picture of its integration in a real EV and shortening the gap between simulation and experimentation.

2. Conventional and CMV Mitigation Modulation Techniques for Two-Level Three-Phase Inverters

In power systems feeding a star-connected load, the CMV is defined as the voltage difference between the three-phase load neutral and the ground (Figure 3) [21,39].

This voltage is proportional to the DC-link voltage and has a frequency related to the carrier frequency of the inverter [9,10]:

$$v_{CM}(t) = \frac{1}{3}[v_{A0}(t) + v_{B0}(t) + v_{C0}(t)], \tag{1}$$

where $v_{CM}(t)$ is the instantaneous CMV and $v_{A0}(t)$, $v_{B0}(t)$, and $v_{C0}(t)$ are the per-phase phase-ground instantaneous voltages (Figure 3). Thus, the impact of the employed modulation technique on the CMV is significant [21,24,39,40].
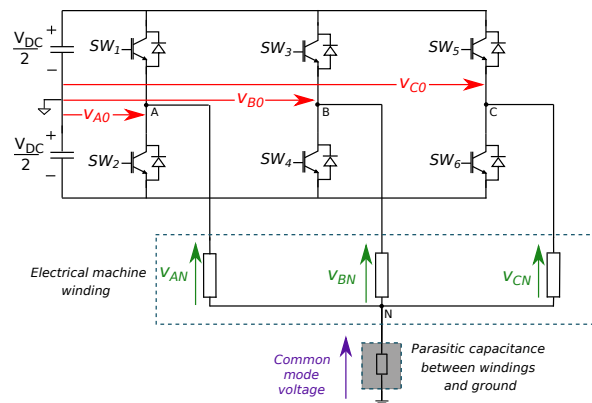

Figure 3. Two-level three-phase voltage source inverter (VSI) with star-connected load, including common mode impedance.

In order to minimize the CMV, a family of modulation techniques named reduced common mode voltage pulse width modulation (RCMV-PWM), which includes techniques such as the active zero-state (AZS-PWM), near-state (NS-PWM), and remote-state (RS-PWM), has been proposed in the literature [25,37]. The objective of such modulation techniques is to avoid the application of zero vectors, which are responsible for generating the highest CMV variations. However, when using such modulation techniques, the overall performance of the converter is degraded in terms of voltage linearity, DC-link current ripple, and THD [24,26,41].

Other modulation techniques such as the constant CMV PWM (CCMV-PWM) can be highlighted, which can provide a constant CMV [21]. On the other hand, discontinuous PWM modulation

techniques are also used in order to partially mitigate efficiency loss (a consequence of CMV mitigation), even at high switching frequencies. Within this group are the discontinuous (D-PWM) and modified discontinuous (MD-PWM) PWM techniques [25].

Table 2 summarizes vector sequences for all these conventional and CMV reduction modulation techniques depending on the $\alpha\beta$ plane sector S_1–S_6. It must be pointed out that each CMV mitigation method has a specific linear region (Figure 4) [24]. For techniques that allow the usage of the entire vector space (Figure 4a), the maximum output voltage to avoid overmodulation is 0.58 V_{DC} [24,26,37], and the modulation index (M) ranges from 0–1. Other modulation techniques such as RS-PWM or CCMV-PWM (Figure 4b) only use even (V_2, V_4, V_6) or odd vectors (V_1, V_3, V_5) to synthesize the reference vector [21,24,37], which limits the maximum output voltage to 0.33 V_{DC}, without overmodulation, resulting in a maximum modulation index of $M = 0.57$. Alternatively, the linear region for the NS modulation technique (Figure 4c) implies a modulation index ranging from $M = 0.67$–1 [24,37].

Table 2. Vector sequence examples for various modulation techniques depending on the specific $\alpha\beta$ plane sector.

PWM Method	References	Sequence (Depending on the $\alpha\beta$ Plane Sector)					
		S_1	S_2	S_3	S_4	S_5	S_6
SV-PWM	[21]	0127210	0327230	0347430	0547450	0567650	0167610
AZS-PWM	[25,37]	6123216	4321234	2345432	6543456	4561654	2165612
RS-PWM	[24,25]	31513	31513	31513	31513	31513	31513
NS-PWM	[24,25,37]	21612	32123	43234	54345	65456	16561
CCMV-PWM	[21]	10301	30103	30503	50305	50105	10501
D-PWM	[25,26,37]	72127	23032	74347	45054	76567	61016
MD-PWM	[25,26,37]	72127	23732	74347	45754	76567	61716
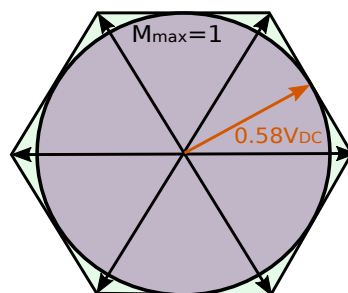
(**a**) SV-PWM, AZS-PWM, D-PWM, and MD-PWM.
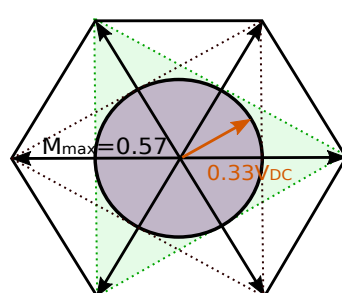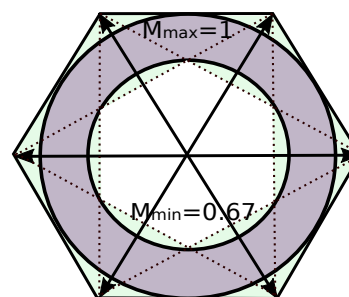
(**b**) RS-PWM and CCMV-PWM.

(**c**) NS-PWM.

Figure 4. Voltage linear regions for various PWM techniques: (**a**) SV-PWM, AZS-PWM, D-PWM, and MD-PWM; (**b**) RS-PWM and CCMV-PWM; (**c**) NS-PWM.

Although these modulation techniques have been originally proposed for their usage in two-phase three-level inverters, they can be adapted to be applied for the alternative topologies that will be analyzed in the following (It should be highlighted that some of the topologies presented in the next section have two operating modes:

(a) They can work applying the vectors dictated to the corresponding modulation technique without any modification.

(b) They require a modification of the modulation strategy to further improve the CMV. This modification consists of opening all the inverter devices and closing additional devices during the application time of zero vectors, instead of using the normal zero vectors V_0 and V_7. Throughout the document, when this modulation technique modification is used, it will be represented by the symbol "ⓜ".).

3. Topologies for CMV Reduction

Among the several three-phase alternatives that can effectively reduce the CMV, DC-decoupling and AC-decoupling topologies can be highlighted due to their features [37]. In the following, the current state-of-the-art of three-phase decoupling alternatives are reviewed (Section 3.1), and novel solutions (Sections 3.2 and 3.3) are proposed and presented.

3.1. State-of-the-Art of Three-Phase Decoupling Topologies

Topologies belonging to the DC-decoupling family rely on disconnecting the DC voltage source from the load when the modulation algorithm must apply zero vectors [25,37], consequently reducing CMV variations. The following existing topologies (Figure 5) can be highlighted:
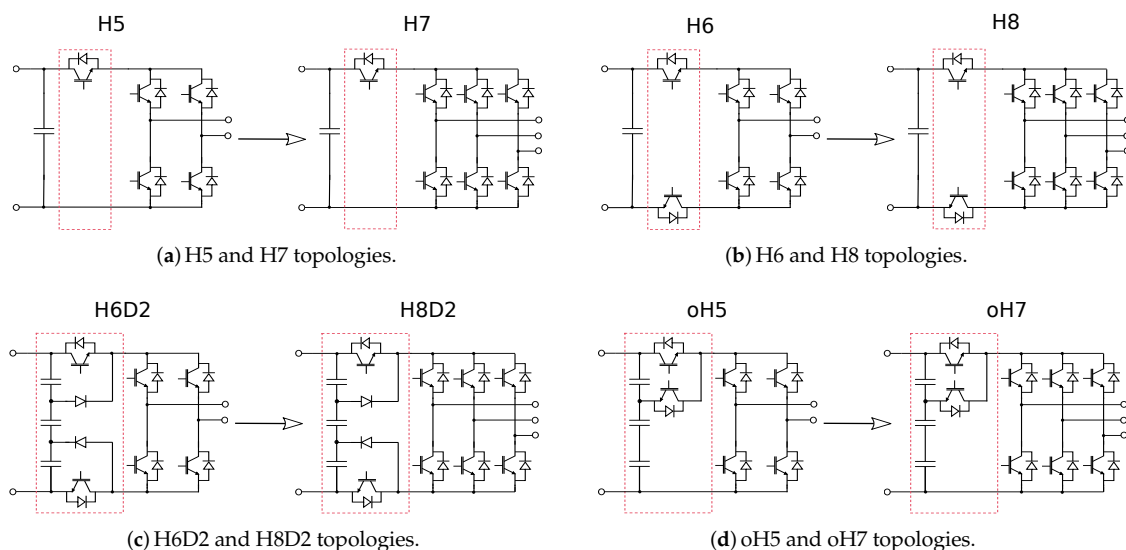

(**a**) H5 and H7 topologies.

(**b**) H6 and H8 topologies.

(**c**) H6D2 and H8D2 topologies.

(**d**) oH5 and oH7 topologies.

Figure 5. Three-phase DC-decoupling topologies and their corresponding single-phase topology from which they have been derived: (**a**) H5 and H7 topologies; (**b**) H6 and H8 topologies; (**c**) H6D2 and H8D2 topologies; (**d**) oH5 and oH7 topologies. The differences, regarding the VSI, are highlighted in red.

(a) **H7**: This topology is a derivative of the H5 architecture. The single-phase H5 topology was originally developed for non-isolated photovoltaic applications, and it has been a subject of study in the recent scientific literature. From this topology, various authors have proposed a three-phase extension (Figure 5a), known as H7 [25,37]. As in the H5, this architecture tries to reduce the CMV by including an additional switch. The disadvantage of this topology is that it does not use a clamping diode to control the CMV level.

(b) **H8**: The H8 topology (Figure 5b) has its origin in the single-phase H6 topology. The difference from the traditional VSI is that incorporates two active DC-decoupling switches that are activated when the zero voltage vectors are applied [25,26,41,42]. This topology reduces the CMV to a greater extent than H7, but as it uses more devices, the power losses increase.

(c) **H8D2**: This is a variant of the H8 topology (Figure 5c). This is constituted by a voltage divider, constituted by three balanced capacitors and two clamping diodes, placed between the two intermediate points of the voltage divider. This allows establishing the desired CMV during the zero voltage states [21,42,43]. However, as the H8, the greater number of devices increases the losses.

(d) **oH7**: This topology (Figure 5d) is not as wide-spread as the others. It has one more clamping device than the H7 topology, and it is a modification of the single-phase oH5 topology [42]. However, the additional complexity of oH7 does not justify the benefits of this topology, as the utilization of only one controllable device is sufficient in the voltage divider to provide the desired CMV level.

On the other hand, the aim of the topologies belonging to the AC-decoupling family is to disconnect the inverter from the AC load when the modulation algorithm applies a zero vector. Among them, the following three-phase structures (Figure 6) can be highlighted:

(a) **3P-HERIC**: The best-known AC-decoupling single-phase topology is the high efficient and reliable inverter concept (HERIC) converter [32–35]. However, the three-phase conversion derivative of this topology, named 3P-HERIC (Figure 6a), is not found in the literature, because it can be considered as complex due to the excessive number of additional active devices required for its implementation.

(b) **VSIZVR**: In [44], a new topology based on the extension of the H-bridge zero-voltage state rectifier (HBZVR) configuration was presented (Figure 6b). This topology, named the VSI zero-voltage state rectifier (VSIZVR), incorporates one rectifier circuit to reduce the CMV. However, as the H7 alternative, this topology is not very attractive, because it does not use the clamping method to control the voltage.

(c) **VSIZVR-D**: Similar to the previous topology, another variant of the HBZVR-D converter was presented in [45] (Figure 6c). This topology, named the VSI zero-voltage state rectifier with clamping diodes (VSIZVR-D), incorporates two rectifier circuits connected to the DC bus by means of two clamping diodes. The drawback of this topology is that the B-rectifier clamping voltage level cannot be controlled.
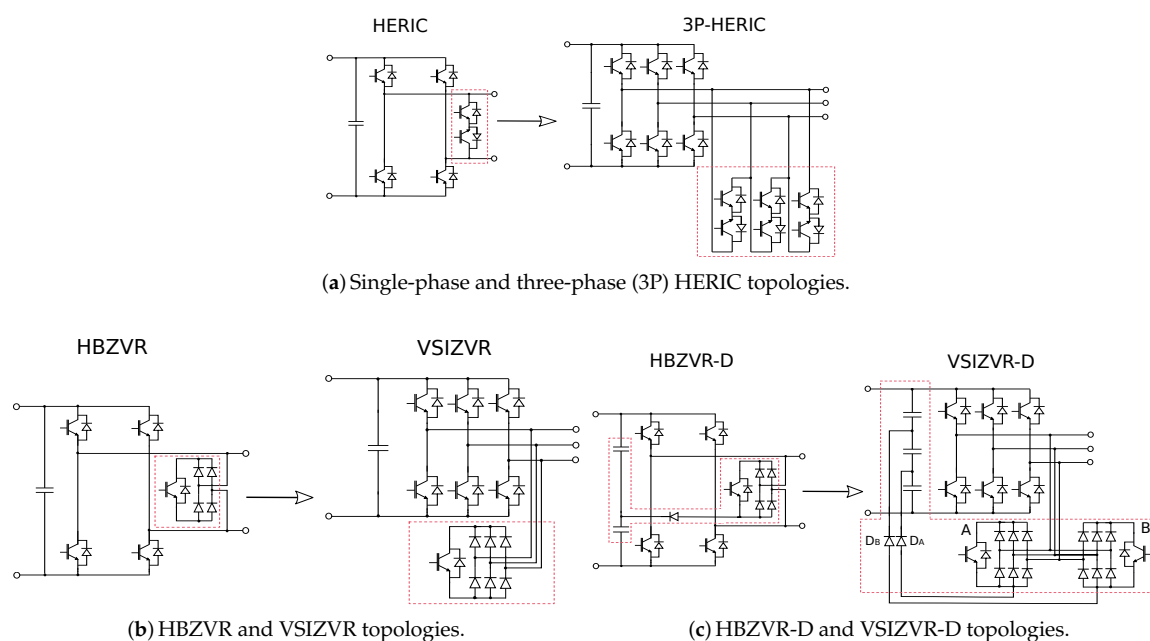

(**a**) Single-phase and three-phase (3P) HERIC topologies.

(**b**) HBZVR and VSIZVR topologies.   (**c**) HBZVR-D and VSIZVR-D topologies.

Figure 6. Three-phase AC-decoupling topologies and the corresponding single-phase topology: (**a**) HERIC topologies; (**b**) HBZVR and VSIZVR topologies; (**c**) HBZVR-D and VSIZVR-D topologies. The differences, regarding the VSI, are highlighted in red.

3.2. Other Three-Phase DC and AC-Decoupling Topologies

From the topologies presented in Section 3.1, this section proposes and discusses other derivatives that have not been previously discussed in the scientific literature (Figure 7). Such derivatives are summarized as follows:

(a) **H7D1**: A proposed alternative to the H7 topology, named H7D1, is shown in Figure 7a. Unlike the oH7 topology, it uses a clamping diode to set the CMV to controllable values (portion of the DC bus voltage), which can be considered as a significant advantage.

(b) **H9D1**: This alternative (Figure 7a) is the only one that has not been derived from a single-phase configuration. The objective of this topology is to improve CMV without incorporating additional AC-decoupling diodes and using only the VSI diodes. In order to achieve this goal, all the devices are opened during the application of zero vectors. For that reason, it is mandatory to incorporate a DC-decoupling mechanism as in the H8 configuration. However, the simultaneous use of DC-decoupling and AC-decoupling will significantly increase the losses of the converter. That is the reason why this alternative is not attractive for EV applications.

(c) **VSIZVR-D1**: The VSIZVR topology (Figure 6b) has the limitation of not being able to control the CMV during the application of zero vectors. An improved topology that includes a clamping diode to provide the desired voltage level, named the VSI zero-voltage state rectifier with one clamping diode (VSIZVR-D1), can be seen in Figure 7b. Unlike the H9D1 variant, this topology achieves the same CMV without using the DC-decoupling solution, but adding a diode rectifier bridge. In addition, it is not necessary to use the rectifier bridge switch anti-parallel diode, because the current does not flow through it.

(d) **VSIZVR-D2**: As stated before, the topology shown in Figure 6c has a significant drawback, as the B-rectifier clamping voltage level cannot be controlled, achieving the same result as in the VSIZVR-D1 topology (Figure 7b). Another alternative (Figure 7b), named VSIZVR-D2, incorporates two rectifier circuits properly connected to the DC bus by means of two clamping diodes. Due to the advantages offered by this topology, its operation principles will be thoroughly explained in Section 3.3.
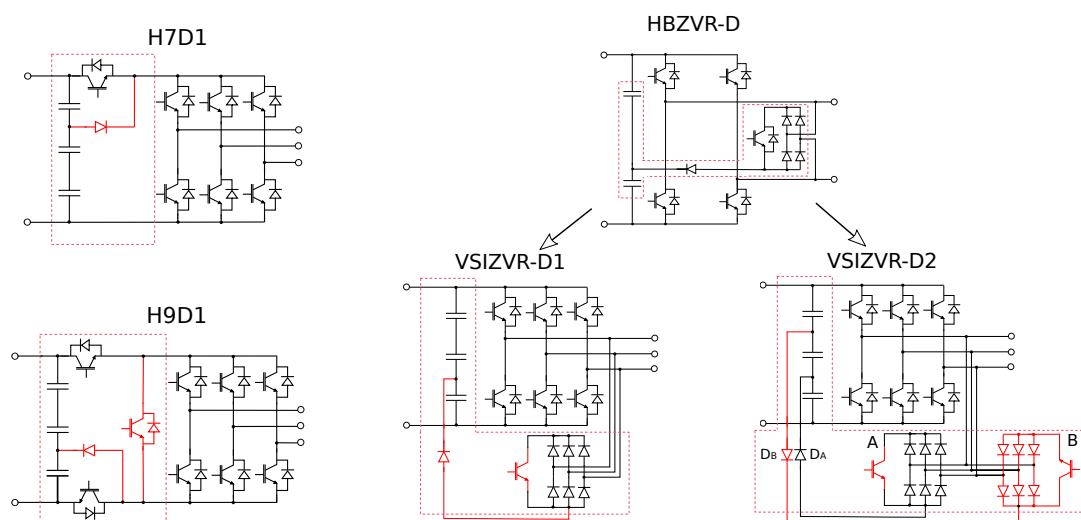
(**a**) Topology variants with DC-decoupling. (**b**) Improved three-phase solutions derived from the HBZVR-D topology.

Figure 7. Other proposed three-phase DC and AC-decoupling topology variants: (**a**) variants with DC-decoupling; (**b**) improved solutions derived from HBZVR-D.

All these solutions allow reducing the CMV in amplitude (v_{CM}) or in the number of CMV variations over each modulation period ($N_{v_{CM}}$) when compared to the VSI, trying not to reduce significantly the other relevant features such as efficiency or THD. Table 3 summarizes the CMV

produced by some of these topologies when applying a given active (V_1-V_6) or zero (V_0, V_7) vector (as AC-decoupling topologies allow to work in two operating modes, VSIZVR-D1 and VSIZVR-D2 topologies allow improving the CMV or operating as a conventional VSI, which may be of interest in terms of maximizing the efficiency in EV applications depending on the driving conditions and battery state of charge level).

Table 3. Switching states and common mode voltage (CMV) for various inverter topologies.

Voltage	Switching	CMV Depending on Each Topology							
Vectors	States	VSI	H7	H7D1	H8	H8D2	H9D1 [m]	VSIZVR-D1 [m]	VSIZVR-D2 [m]
V_0	000	$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/2$	$V_{DC}/4$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$
V_1	100	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$
V_2	110	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$
V_3	010	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$
V_4	011	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$
V_5	001	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$
V_6	101	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$
V_7	111	$V_{DC}/2$	$-V_{DC}/4$	$V_{DC}/6$	$-V_{DC}/4$	$V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$V_{DC}/6$
SV-PWM CMV waveforms									
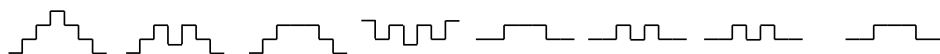
Note: [m] Operation Mode 2 of the AC-decoupling topologies.

3.3. Operation Principles of the VSIZVR-D2 Topology

AC-decoupling solutions combined with clamping methods are generally more advantageous than DC-decoupling solutions (this will be demonstrated in Section 4.1). In this context, VSIZVR-D2 has been selected due to its advantages, and this paper analyzes in detail the operation principles of this topology (Figure 8).
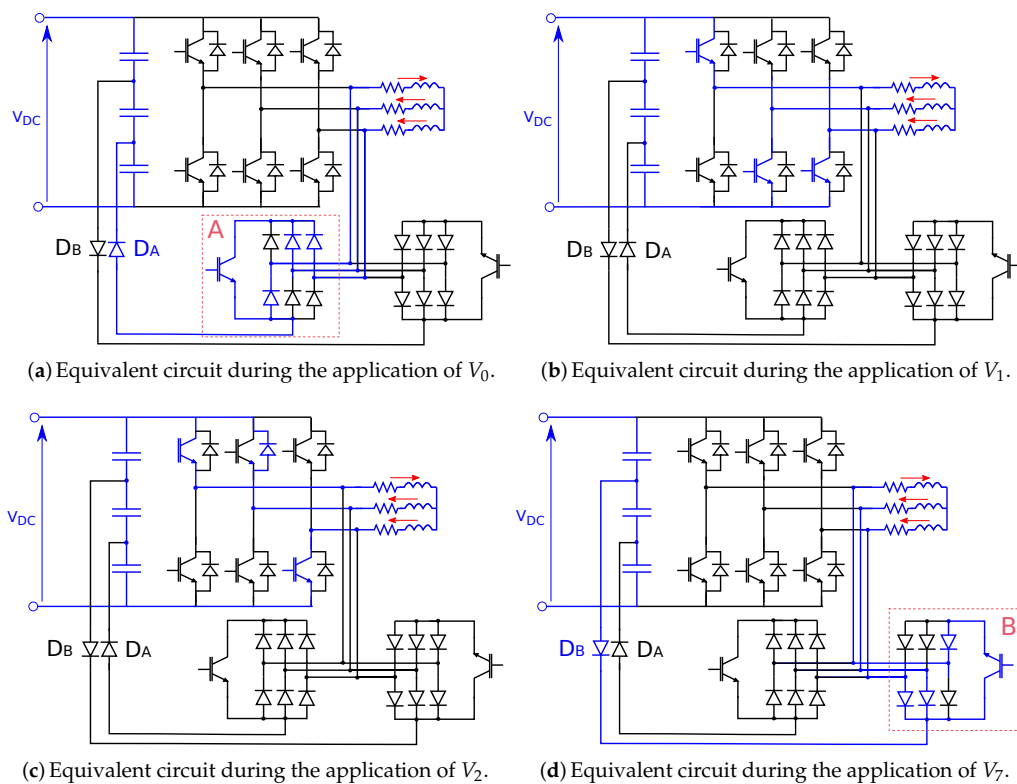

(**a**) Equivalent circuit during the application of V_0.　　(**b**) Equivalent circuit during the application of V_1.

(**c**) Equivalent circuit during the application of V_2.　　(**d**) Equivalent circuit during the application of V_7.

Figure 8. Current paths and switching sequences in the VSIZVR-D2 applying the vector sequence "0127210".

In this topology, a capacitive divider is placed in the DC side of the inverter, producing CMV voltages equal to $-V_{DC}/6$ and $V_{DC}/6$ during the application times corresponding to zero vectors

(Table 3). In fact, the AC-decoupling devices and clamping diodes (D_A and D_B) allow obtaining the same CMV values during the application times of both active and zero vectors.

This topology operates as follows. The A-rectifier (Figure 8a) is activated during the zero vector V_0, before and after applying odd active vectors (V_1, V_3, V_5). On the other hand, the B-rectifier (Figure 8d) is activated during the zero vector V_7 before and after applying even active vectors (V_2, V_4, V_6). For example, during the application of the "0127210" SV-PWM vector sequence in Sector 1, VSIZVR-D2 devices switch following the sequence depicted in Figure 8.

In practice, it is necessary to add parallel resistances in order to ensure an equal partition of the voltage across the capacitors. In addition, it is mandatory to add a dead time during the transition between the active vectors and the zero vectors to avoid short circuits in the capacitors of the DC-link. Nevertheless, diodes D_A and D_B are included in order to prevent this type of short circuit (Figure 8).

4. Analysis of the CMV Reduction Topologies

Once the most relevant CMV mitigation topologies have been presented, they will be compared by means of simulation in order to study their suitability for EV applications, and the usage of various modulation techniques will also be analyzed. The MATLAB/Simulink platform was used for this purpose.

4.1. Comparison of the Studied Topologies

In order to compare the performance of each topology independent of the modulation technique, the traditional SV-PWM technique was applied for all of them, controlling the additional power switches in order to reduce the CMV. The converters were controlled in open loop, connected to a 320-V DC source at the input and a passive three-phase load (R = 1 Ω and L = 1 mH) at the output. The switching frequency f_{sw} was set to 10 kHz, as DC bus voltages and switching frequencies of such magnitude orders are common in current industrial automotive inverters [46].

Figure 9 shows the CMV variations and their harmonic spectrum over one switching period when using the studied DC-decoupling and AC-decoupling topologies. The topologies that achieved a greater reduction in CMV variations were the VSIZVR-D2 (using the ⓜ operation mode) and the H8D2. Both improved the Δv_{CM} and $N_{v_{CM}}$ up to 66.6% when compared to the traditional VSI. Followed by these were the H9D1 and VSIZVR-D1 topologies, improving Δv_{CM} up to 66.6%, but only improving $N_{v_{CM}}$ up to 33.3% due to the greater number of vector transitions. Without using the clamping method, the H8 topology improved Δv_{CM} up to 50% (but with the same $N_{v_{CM}}$ as the VSI). Finally, the H7 and H7D1 topologies improved Δv_{CM} up to 33.3% and $N_{v_{CM}}$ up to 33.3%.

As SV-PWM was used to modulate all the topologies, the THD remained equal for all cases. However, and due to the additional switches that incorporate such topologies, significant differences can be observed regarding efficiency (the power loss model used in this study was detailed in [47]). In this sense, Figure 10 illustrates the relationship between efficiency and switching frequency for a modulation index of $M = 0.6$ (although only mode ⓜ is represented for the AC-decoupling topologies, the efficiency would correspond to the VSI curve in the case of VSIZVR-D1 and VSIZVR-D2 when using traditional modulations without modifications). On the other hand, the distribution between conduction and switching losses varies according to the topology. For example, the DC-decoupling topologies increased the conduction losses, but reduced the switching losses (Figure 11).

As a summary, Figure 12 shows the results obtained for all the studied topologies under a given operation condition, where vertical blue bars represent the maximum CMV variation, the dashed red line represents $N_{v_{CM}}$, and the table below the figure provides additional data of interest. As a trade-off, it was concluded that the VSIZVR-D2 can be considered the best topology for CMV reduction, while it kept the efficiency between reasonable values, i.e., by redistributing the losses between its additional devices (Table 4). This last can be an additional advantage of this topology, as this redistribution of the power losses could reduce the cost and size of the required heat sink. Thus, in the following, the analysis will focus on the VSIZVR-D2 topology.
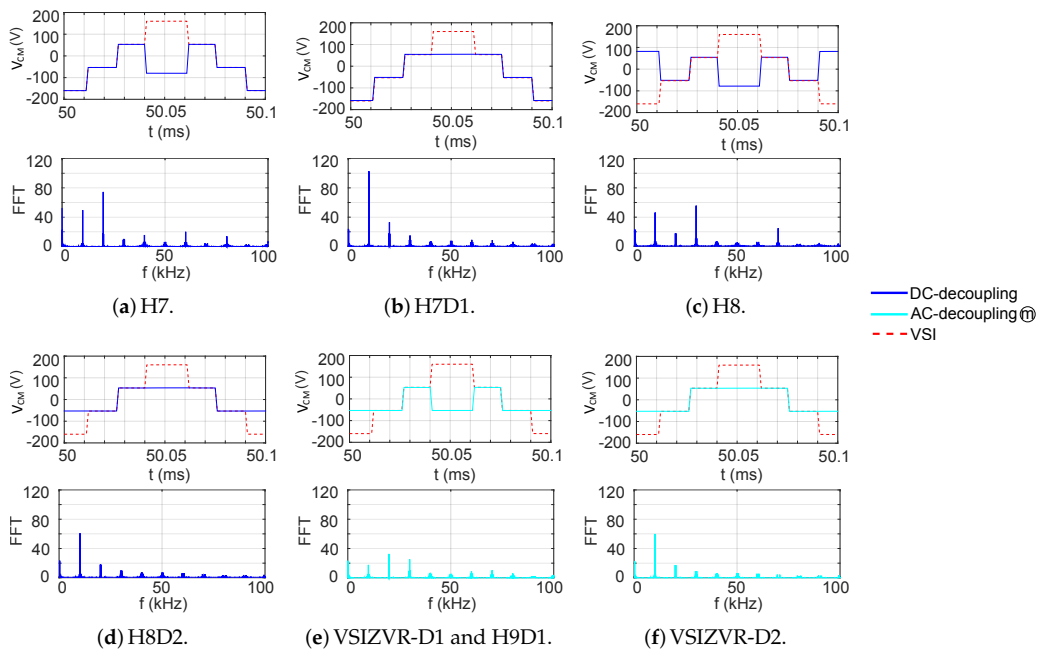
Figure 9. CMV and spectrum of DC-decoupling and AC-decoupling topologies for *M* = 0.6: (**a**) H7 topology; (**b**) H7D1 topology; (**c**) H8 topology; (**d**) H8D2 topology; (**e**) VSIZVR-D1 and H9D1 topologies; (**f**) VSIZVR-D2 topology.
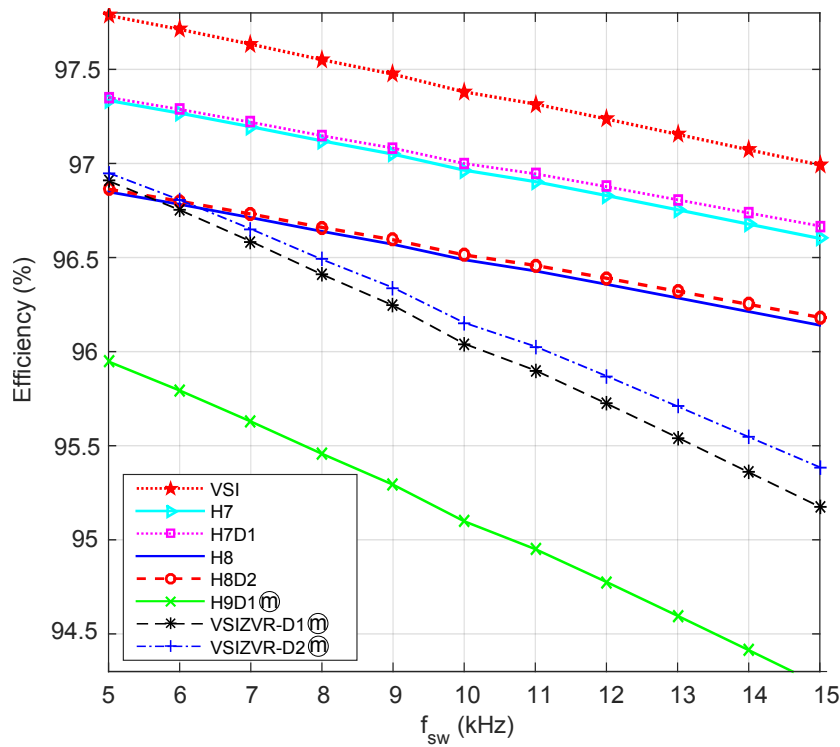

Figure 10. Efficiency versus f_{sw} for *M* = 0.6.

	VSI	H7	H7D1	H8	H8D2	H9D1	VSIZVR-D1	VSIZVR-D2
P_{tot} (W)	430.2	498.3	493.4	576.2	572.9	804.2	649.8	631.6
ΔP_{tot}	—	15.8%	14.7%	34.0%	33.2%	87.0%	51.1%	46.8%
ΔP_{cond}	—	26.5%	26.5%	52.9%	52.9%	78.4%	25.6%	25.7%
ΔP_{sw}	—	-9.2%	-13.1%	-10.6%	-13.3%	107.2%	111.2%	96.7%

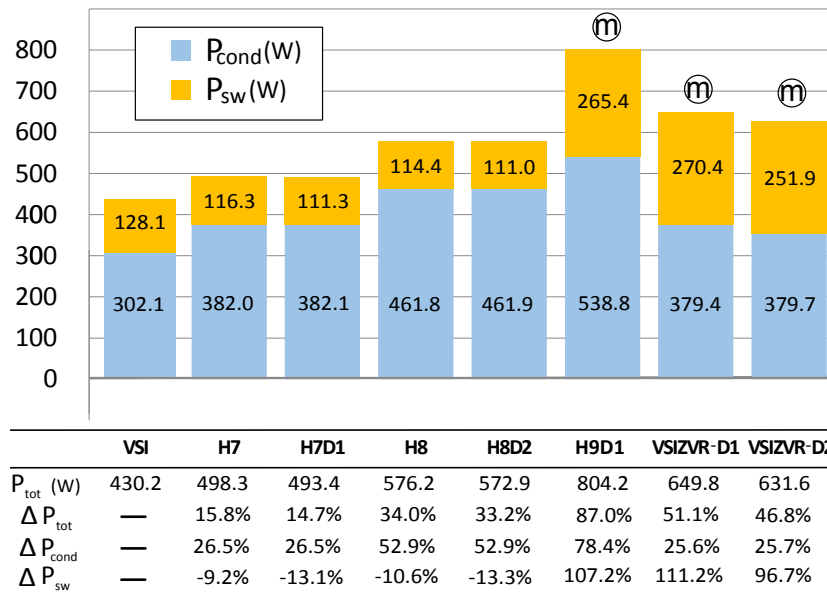**Figure 11.** Variation of the total losses for all the studied topologies with respect to the conventional VSI for *M* = 0.6.

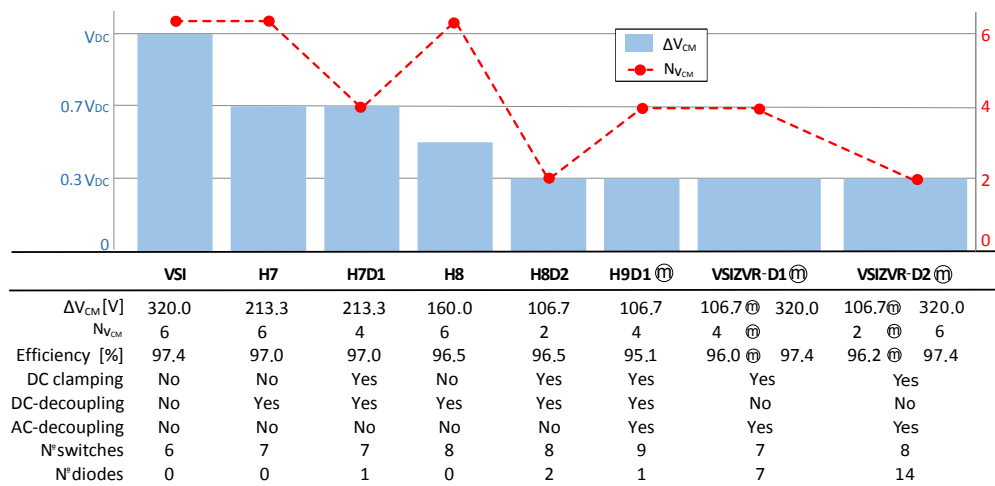|	VSI	H7	H7D1	H8	H8D2	H9D1 ⓜ	VSIZVR-D1 ⓜ		VSIZVR-D2 ⓜ	
ΔV_{CM} [V]	320.0	213.3	213.3	160.0	106.7	106.7	106.7ⓜ	320.0	106.7ⓜ	320.0
$N_{V_{CM}}$	6	6	4	6	2	4	4	ⓜ	2 ⓜ	6
Efficiency [%]	97.4	97.0	97.0	96.5	96.5	95.1	96.0 ⓜ	97.4	96.2 ⓜ	97.4
DC clamping	No	No	Yes	No	Yes	Yes	Yes		Yes	
DC-decoupling	No	Yes	Yes	Yes	Yes	Yes	No		No	
AC-decoupling	No	No	No	No	No	Yes	Yes		Yes	
Nº switches	6	7	7	8	8	9	7		8	
Nº diodes	0	0	1	0	2	1	7		14	

Figure 12. Comparative summary of three-phase topologies applicable to EVs for *M* = 0.6.

Table 4. Loss distribution per device in VSI and VSIZVR-D2 applying SV-PWM, for *M* = 0.6.

Devices		**Losses**			
Topology		P_{cond_Q} (W)	P_{cond_D} (W)	P_{sw_Q} (W)	P_{sw_D} (W)
VSI	$SW_1 - SW_6$	37.2	13.1	19.2	2.6
	$SW_7 - SW_8$	-	-	-	-
	$D_{A_1} - D_{A_6}$	-	-	-	-
	$D_{B_1} - D_{B_6}$	-	-	-	-
VSIZVR-D2	$SW_1 - SW_6$	26.8	1.1	16.9	0.7
	$SW_7 - SW_8$	34.5	-	61.1	-
	$D_{A_1} - D_{A_6}$	-	11.9	-	2.1
	$D_{B_1} - D_{B_6}$	-	11.9	-	2.1

4.2. Analysis of the Influence of the Modulation Technique on the VSIZVR-D2 Topology

In this section, the performances of the modulation techniques described in Section 2 are compared for the VSIZVR-D2 topology in order to determine which provides the best possible performance. Again, the simulation conditions of the previous section were set.

Figure 13 shows that, regardless of the modulation technique, this topology improved the CMV over the traditional VSI. Another relevant conclusion was that RCMV-PWM modulation techniques did not use zero vectors, so they did not fully exploit the benefits of the VSIZVR-D2 topology, obtaining the same results that would be obtained in a traditional VSI. Furthermore, the discontinuous modulation techniques and the CCMV-PWM improved the CMV over the traditional VSI without making use of the benefits of the VSIZVR-D2 topology. However, when all the inverter's devices were open (modulation modification ⓜ) and the rectifiers were activated, the CMV was completely eliminated.

As a summary, Table 5 shows the main differences obtained when applying each modulation technique. An improvement of DC bus current ripple ($\Delta I_{C_{DC}}$) was observed for most of these. However, depending on the employed modulation, it can be seen that the THD at the load side was significantly increased (Figure 14). Finally, the efficiency differences between the different modulation techniques did not exceed 0.54% with respect to the VSI. In this sense, Figure 15 shows, in detail, the evolution of the efficiency for different modulation index values. It can be seen that, when CMV was improved by using the rectifiers of the VSIZVR-D2 (ⓜ), the efficiency was also reduced. Otherwise, without using them, the efficiencies were higher than in the VSI with SV-PWM.
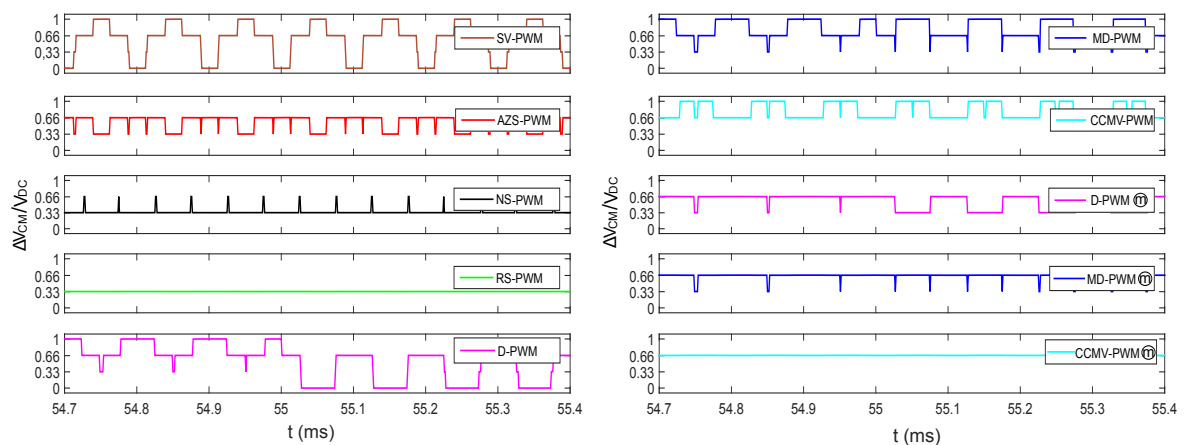

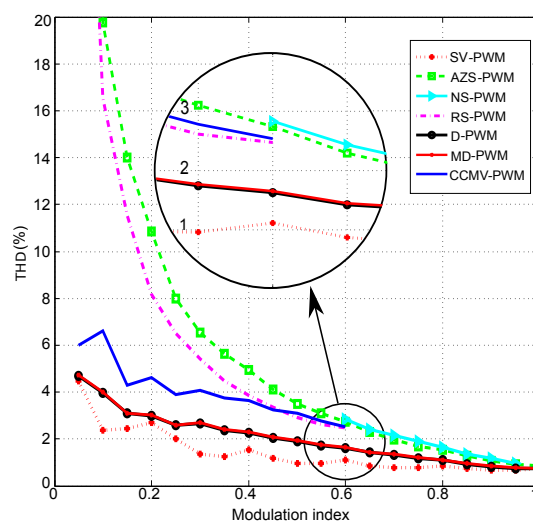**Figure 13.** CMV of VSIZVR-D2 with various modulation techniques for *M* = 0.6.

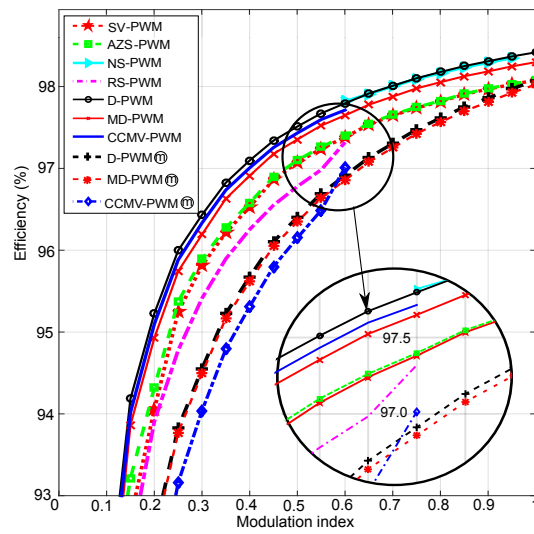**Figure 14.** THD vs. the modulation index.

Figure 15. Efficiency vs. the modulation index.

From all these results, it was concluded that the best modulation techniques among those studied were D-PWM and CCMV-PWM, as these allowed the maximum performance of the VSI-ZVR-D2 in general terms.

In the following and in order to further explore the applicability of the proposed VSIZVR-D2 topology in a real EV, its performance under realistic driving conditions will be carried out, focusing on power losses and efficiency.

Table 5. Performance comparisons for various PWM techniques for $M = 0.6$.

Modulation	Voltage Linearity	Phase Current	Current THD	CMV Amplitude		Num. CMV Variations	CMV Levels	DC-link Current Ripple		Output Current Ripple		Efficiency
		$[A_p]$	(%)		dev. (%) [3]	dev. (%) [3]		$[A_{rms}]$	dev. (%) [3]	$[A_p]$	dev. (%) [3]	(%)
SV-PWM	0–1	104.5	1.1	320.0	-	6	-	4	32.4	-	2.2	-	97.4
AZS-PWM	0–1	104.5	2.7	106.7	−66.7	6	0	2	34.3	5.6	3.3	49.5	97.4
NS-PWM [1]	0.67–1	107.4	2.8	106.7	−66.7	2	−66.7	2	19.6	−39.5	2.2	0.0	97.8
RS-PWM [2]	0–0.57	104.6	2.5	0.0	−100.0	0	−100.0	1	32.5	0.3	3.6	60.4	97.3
D-PWM	0–1	105.1	1.6	320.0	0	4	−33.3	4	22.9	−29.5	2.5	12.2	97.8
MD-PWM	0–1	105.1	1.6	213.3	−33.3	4	−33.3	3	22.9	−29.5	2.5	12.2	97.7
CCMV-PWM [2]	0–0.57	104.9	2.5	213.3	−33.3	3	−50.0	2	23.1	−28.8	1.2	−48.2	97.7
D-PWM ⓜ	0–1	105.1	1.6	106.7	−66.7	2	−66.7	2	22.9	−29.5	2.5	12.2	96.9
MD-PWM ⓜ	0–1	105.1	1.6	106.7	−66.7	3	−50.0	2	22.9	−29.5	2.5	12.2	96.9
CCMV-PWM ⓜ [2]	0–0.57	104.9	2.5	0.0	−100.0	0	−100.0	1	23.1	−28.8	1.1	−48.7	97.0

Notes: [1] The system enters slightly into overmodulation. The modulation index of 0.6 is less than 0.67. [2] The system enters slightly into overmodulation. The modulation index of 0.6 is greater than 0.57. [3] Deviation from SV-PWM. Negative deviations represent an improvement over the studied feature, while positive ones represent a worsening.

5. VSIZVR-D2 Topology Performance during Realistic Driving Conditions

A complete light-duty EV drive model including power electronics, a battery, a synchronous electric machine, a control board, vehicle dynamics, and power loss and thermal calculation blocks was developed in the Simulink environment (Figure 16) to study the VSIZVR-D2 topology under real driving conditions. The power conversion topology was described with the SimPowerSystems toolbox together with the power loss and thermal model described in Appendix A. The stator and torque equations of the electric machine were implemented in the synchronous *dq* reference frame, where calculated stator currents were introduced to the converter model by means of variable current sources. The well-known field-oriented control (FOC) approach was followed in the simulated controller for torque regulation, and a flowchart-based voltage-constraint-tracking field weakening algorithm was also included to operate beyond the machine base speed [48]. This model had the capability of simulating standardized driving cycles (more information regarding other EV driving cycles can be obtained in [49]) with a long duration and with real torque and speed conditions, while it kept the simulation step low (in the order of 1 μs) to avoid *jitter* and to obtain accurate results. Details regarding the vehicular model can be found in a previous work of the authors presented in [50].
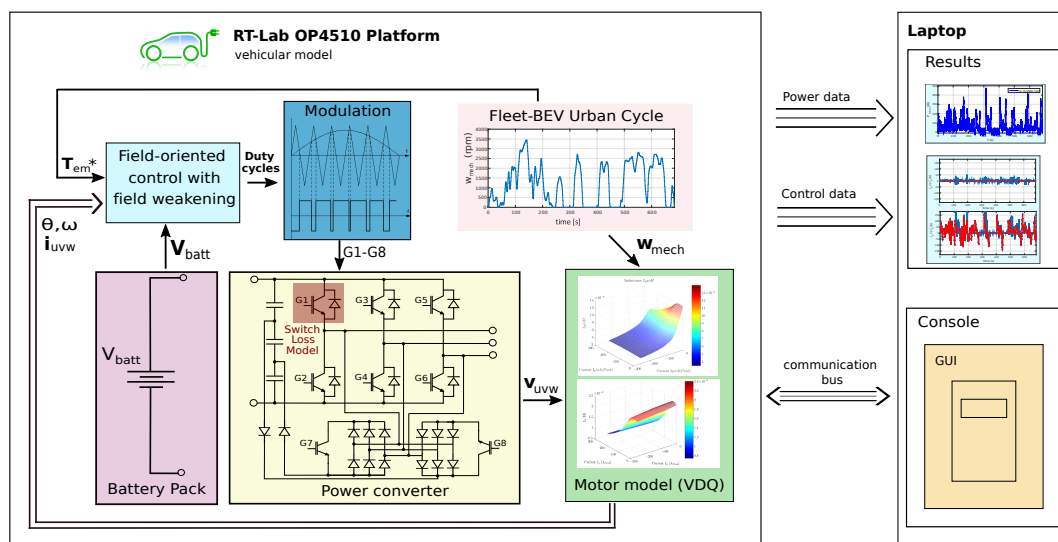

Figure 16. Diagram of the simulation platform of the electric vehicle propulsion system.

The electric machine used was a 65-kW axial flux SM-PMSM (EVO AF-130). The DC-link incorporated a C_{DC} of 700 μF, and the battery pack had a rated voltage of 320 V. Each inverter switch was formed by four parallelized automotive-grade discrete IR AUIR-GPS4067D1 devices (TO-247 package), as such devices constitute a representative example of the power device technologies used in current EVs [18]. Once again, the switching frequency was set at 10 kHz for the same reason justified in Section 4.1.

Regarding the driving cycles selected for this analysis, the Fleet-BEVdriving cycles (defined in [51]) were used, which represent real EV driving conditions that consider the driver's range anxiety, giving a better representation of a real EV driving. The Fleet-BEV cycles consist of three differentiated cycles, i.e., urban, rural (extra-urban), and mixed versions. In order to study the power conversion stage performance separately under urban and extra-urban conditions, the Fleet-BEV-Urban-Cycle and the Fleet-BEV-Rural-Cycle were selected.

As the computational burden for simulating such long driving cycles was high, the developed model was implemented for a single computational node of a high-performance OPAL-RT RT-Lab OP4510 digital platform (Figure 16), which consisted of four computational nodes (Intel Xeon E3, 3.2 GHz). In this way, it was possible to simulate more than one test condition simultaneously by using parallel computing, greatly accelerating the required tests.

In order to compare the VSIZVRD-2 with the operation of a conventional VSI, the SV-PWM and D-PWM techniques were selected. Additionally, two hybrid modulation techniques were proposed in order to achieve a better trade off between CMV reduction and efficiency. The first one, named Hybrid 1, combined the D-PWM (when $M > 0.57$) and the CCMV-PWM $\widehat{m}$ (when $M < 0.57$). The other one, named Hybrid 2, combined the D-PWM $\widehat{m}$ (when $M > 0.57$) and the CCMV-PWM (when $M < 0.57$).

5.1. Results of the VSIZVR-D2 Topology under the Fleet-BEV-Urban-Cycle

Figure 17 shows how the EV propulsion system control algorithm performed a satisfactory machine torque control (T_{em}) throughout the entire urban driving cycle. When comparing the performance of the studied modulation techniques under this driving cycle (Table 6), it can be observed how the $\widehat{m}$ modified techniques had a lower converter efficiency, but were able to reduce CMV to a greater extent. In addition, when using hybrid modulations, a similar efficiency to the VSI topology with SV-PWM could be achieved, at the cost of losing some CMV reduction capability. In this sense, Figure 18 compares the VSI topology (using the SV-PWM modulation technique) and the VSIZVR-D2 using the hybrid modulations Hybrid 1 and Hybrid 2. It can be seen that the average values of the power losses were close in both curves. In addition, Figure 19 shows (for the studied modulation techniques) how the power converter losses were distributed between the traditional inverter devices and the rectifier bridges in the new VSIZVR-D2 inverter topology.
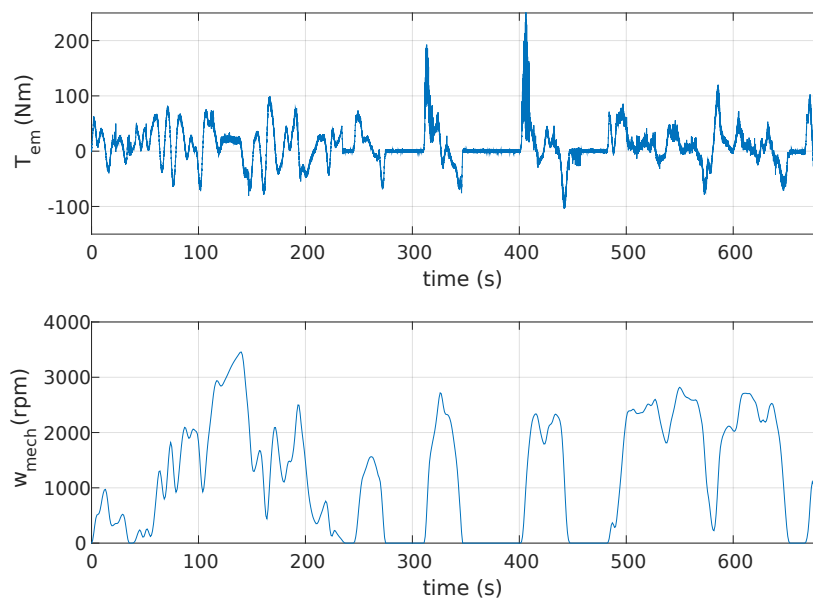

Figure 17. Torque and speed profiles obtained throughout the urban driving cycle for Hybrid 2 modulation.

Table 6. Results' summary obtained using various modulation techniques in the VSIZVR-D2 during a Fleet-BEV-Urban-Cycle.

Modulation Technique	CCMV-PWM Utilization (%)	D-PWM Utilization (%)	SV-PWM Utilization (%)	Efficiency (%)	$N_{v_{CM}}$ Reduction (%) [1]	Δv_{CM} Reduction (%) [1]	Average Power Dissipated (W)	Dev. Average Power Dissipated (%) [1]
SV-PWM	0	0	100	97.3	-	-	84.8	-
SV-PWM ⓜ	0	0	100	96.0	−66.7	−66.7	129.0	52.1
D-PWM	0	100	0	97.7	−33.3	0	71.9	−15.2
D-PWM ⓜ	0	100	0	96.6	−66.7	−66.7	106.9	26.1
Hybrid 1	90.2	9.8	0	97.3	−51.6	−36.6	84.3	−0.6
Hybrid 2	90.5	9.5	0	96.1	−93.7	−90.5	122.5	44.5

Notes: [1] Deviation from SV-PWM. Negative deviations represent an improvement over the studied feature, while positive ones represent a worsening.
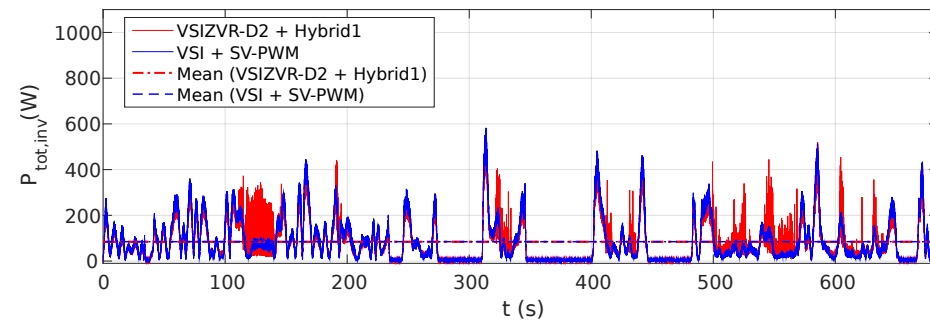
(**a**) Hybrid 1: CCMV-PWM and D-PWM ⓜ.
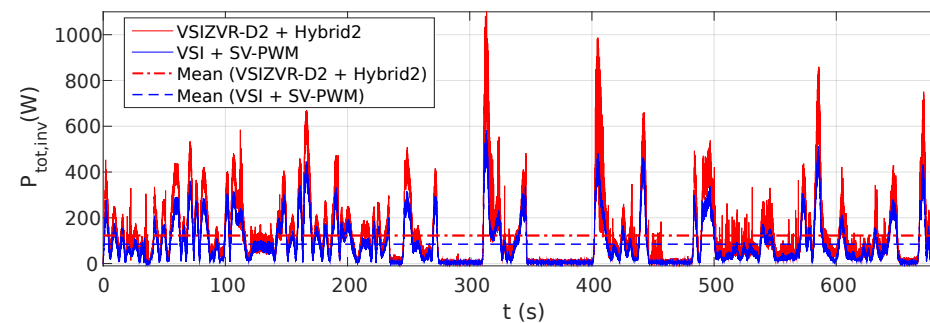
(**b**) Hybrid 2: CCMV-PWM ⓜ and D-PWM.

Figure 18. Total converter losses during the Fleet-BEV-Urban-Cycle: VSI topology using SV-PWM vs. VSIZVR-D2 using hybrid PWMs: (**a**) Hybrid 1; (**b**) Hybrid 2.

(**a**) SV-PWM ⓜ.

(**b**) D-PWM ⓜ.

(**c**) Hybrid 1: CCMV-PWM and D-PWM ⓜ.
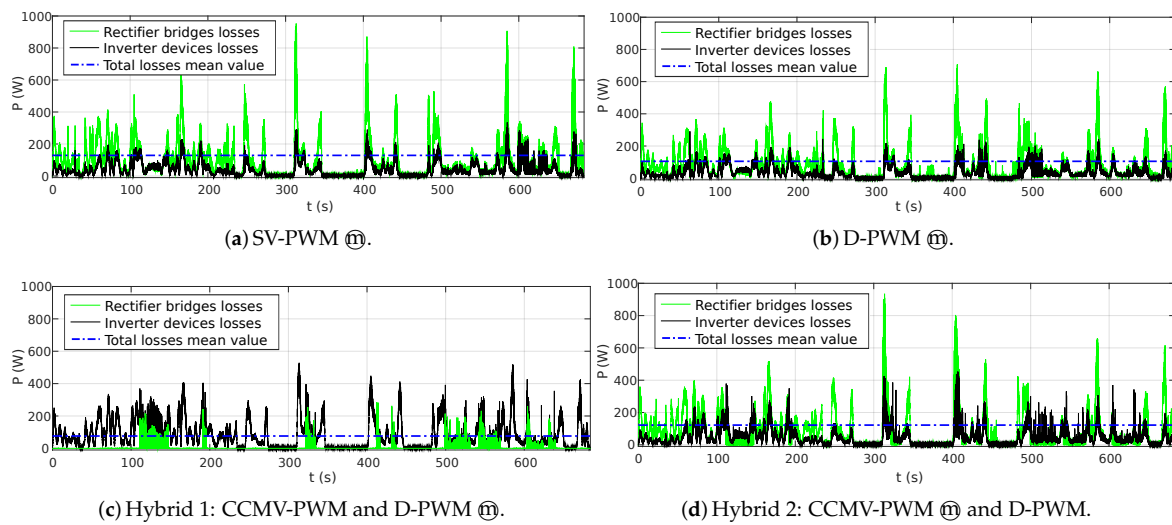
(**d**) Hybrid 2: CCMV-PWM ⓜ and D-PWM.

Figure 19. VSIZVR-D2 losses' distribution between the traditional inverter and the additional devices under the urban cycle: (**a**) SV-PWM ⓜ; (**b**) D-PWM ⓜ; (**c**) Hybrid 1; (**d**) Hybrid 2.

5.2. Results of the VSIZVR-D2 Topology under the Fleet-BEV-Rural-Cycle

As for the urban cycle, Figure 20 shows how torque control (T_{em}) was satisfactorily performed throughout the entire rural driving cycle. Table 7 shows, quantitatively, the differences when applying the studied modulation techniques for the VSIZVR-D2 topology under the rural driving cycle. Figure 21 compares again the VSI topology (using the SV-PWM modulation technique) and the VSIZVR-D2 using the hybrid modulations Hybrid 1 and Hybrid 2. It can be seen again that the average values of the power losses were close in both curves. Figure 22 shows the loss distribution between the inverter side devices and the additional devices.
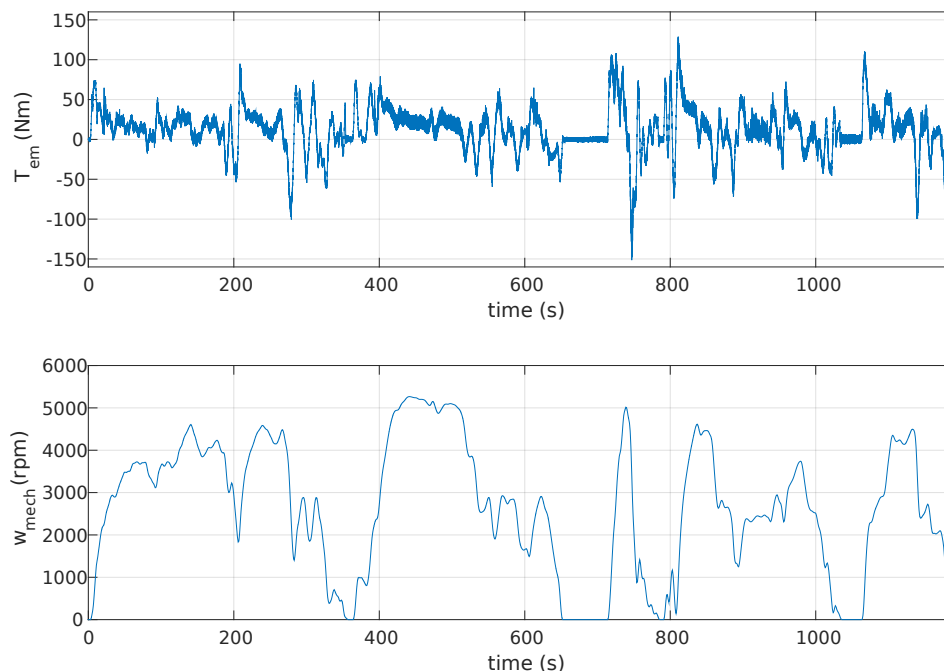

Figure 20. Torque and speed profiles obtained throughout the rural driving cycle for Hybrid 2 modulation.

Table 7. Results' summary obtained using various modulation techniques in the VSIZVR-D2 during a Fleet-BEV-Rural-Cycle.

Modulation Technique	CCMV-PWM Utilization (%)	D-PWM Utilization (%)	SV-PWM Utilization (%)	Efficiency (%)	$N_{v_{CM}}$ Reduction (%) [1]	Δv_{CM} Reduction (%) [1]	Average Power Dissipated (W)	Dev. Average Power Dissipated (%) [1]
SV-PWM	0	0	100	98.3	-	-	112.6	-
SV-PWM ⓜ	0	0	100	97.7	−66.7	−66.7	148.7	32.1
D-PWM	0	100	0	98.4	−33.3	0	101.8	−9.6
D-PWM ⓜ	0	100	0	97.9	−66.7	−66.7	131.2	16.5
Hybrid 1	51.3	48.7	0	95.5	−58.1	−49.6	177.6	57.7
Hybrid 2	51.4	48.6	0	98.0	−67.6	−51.4	129.3	14.8

Notes: [1] Deviation from SV-PWM. Negative deviations represent an improvement over the studied feature, while positive ones represent a worsening.
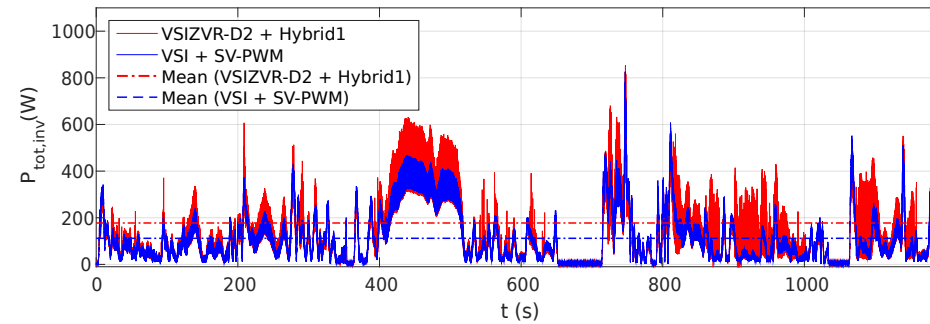
(**a**) Hybrid 1: CCMV-PWM and D-PWM ⓜ.
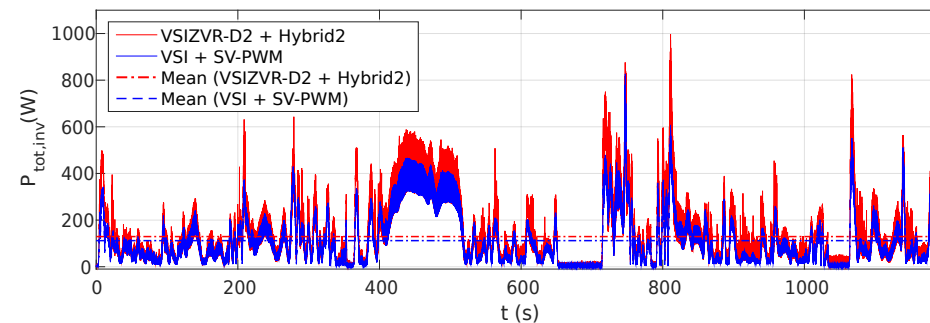
(**b**) Hybrid 2: CCMV-PWM ⓜ and D-PWM.

Figure 21. Total converter losses during the Fleet-BEV-Rural-Cycle: VSI topology using SV-PWM vs. VSIZVR-D2 using hybrid modulations: (**a**) Hybrid 1; (**b**) Hybrid 2.
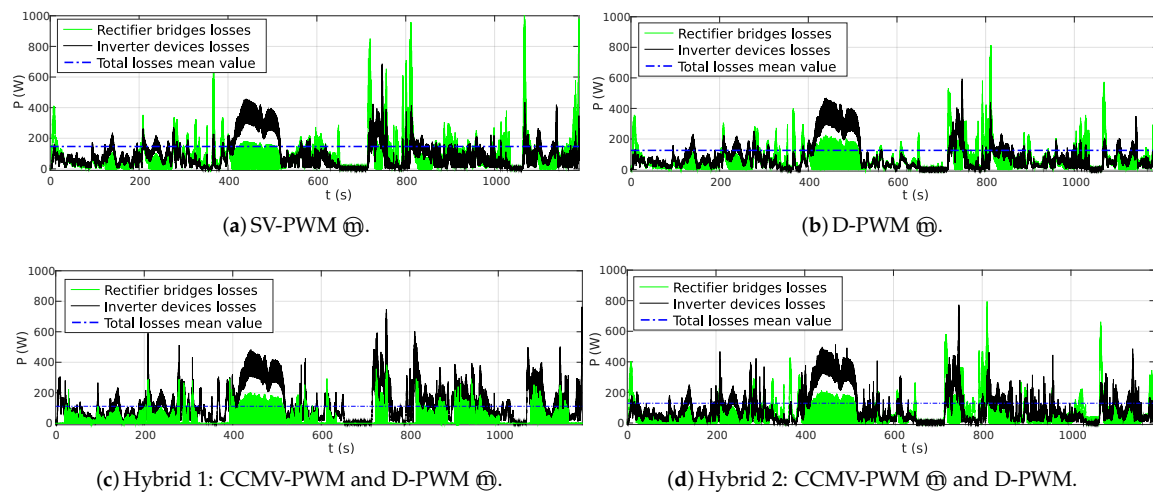
(**a**) SV-PWM ⓜ.

(**b**) D-PWM ⓜ.

(**c**) Hybrid 1: CCMV-PWM and D-PWM ⓜ.

(**d**) Hybrid 2: CCMV-PWM ⓜ and D-PWM.

Figure 22. VSIZVR-D2 loss distribution between the inverter switches and the additional devices under the rural cycle: (**a**) SV-PWM ⓜ; (**b**) D-PWM ⓜ; (**c**) Hybrid 1; (**d**) Hybrid 2.

6. Conclusions

A number of inverter topologies that can mitigate CMV issues were reviewed or proposed in this paper, and their performances were compared. The best results were obtained when using AC-decoupling topologies as, in general, the usage of such decoupling topologies provided a higher efficiency with respect to the DC-decoupling ones. Furthermore, it was shown that the voltage-clamping solution ensured the desired CMV during the application times of zero vectors. This allowed the usage of devices with a reduced breakdown voltage, reducing the additional losses introduced by these devices.

From the previous analysis, it was concluded that the VSIZVR-D2 was the best topology when considering the CMV, THD, DC bus current ripple, output current ripple, and efficiency. This work proposed VSIZVR-D2, which allowed mitigating the CMV issue with the lowest losses possible. In addition, the VSIZVR-D2 allowed operating in two different operating modes. When the efficiency was more important than the CMV, the converter could work like the traditional VSI, obtaining the same efficiency. When CMV was more important, the converter could open all the VSI devices during zero vectors, reducing CMV variations, but making the converter less efficient. Thus, this degree of freedom can be effectively used in an EV application.

Finally, simulations of the complete EV propulsion system under realistic driving conditions showed that the efficiency reduction of the proposed VSIZVR-D2 topology under hybrid modulation techniques was assumable considering the benefits on CMV reduction. Specifically and due to the urban and extra-urban nature of the cycles, the Hybrid 1 technique was more efficient for the urban driving cycle, and the Hybrid 2 technique was more efficient for the rural driving cycle.

Author Contributions: E.R. concept for the article, state of the art, writting, simulation platform development, simulations and analysis, M.F. simulation platform development, support on simulations and analysis, E.I. simulation platform development, review and suppervision, J.A. review and suppervision, I.K. review and conceptual support.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating current
AZS-PWM	Active zero-state pulse width modulation
CCMV-PWM	Constant common mode voltage pulse width modulation
CMV	Common mode voltage
DC	Direct current
D-PWM	Discontinuous pulse width modulation
EDM	Electric discharge machining
EMI	Electromagnetic interferences
EV	Electric vehicle
Fleet-BEV	Fleet battery electric vehicle
FOC	Field-oriented control
HBZVR	H-Bridge zero-voltage rectifier
HERIC	High efficient and reliable inverter concept
IGBT	Insulated gate bipolar transistor
MD-PWM	Modified discontinuous pulse width modulation
NS-PWM	Near-state pulse width modulation
PWM	Pulse width modulation
RCMV-PWM	Reduced common mode voltage pulse width modulation
RS-PWM	Remote-state pulse width modulation
RT	Real time
SM-PMSM	Surface mounted permanent magnet synchronous machine
SV-PWM	Space vector pulse width modulation
THD	Total harmonic distortion
VSI	Voltage source inverter
VSIZVR	Voltage source inverter zero-voltage rectifier
WBG	Wide bandgap

Appendix A. Description of the Power Loss and Thermal Model

In this work, an accurate loss model of an automotive-grade IGBT/diode discrete device of International Rectifier (part number AUIRGPS4067D1) was carried out in order to compare the studied topologies and modulation techniques. Table A1 shows the most significant parameters of such a device.

In order to determine the power losses of the power converter, the calculation of the conduction and switching losses of each IGBT and diode was required [52]. The IGBT conduction losses can be expressed as:

$$P_{cond,Q} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_{CEsat}(t)\, i_C(t)\, dt, \tag{A1}$$

where T_{sw} is the switching period, i_C is the instantaneous current circulating through the semiconductor, and $v_{CEsat}(t)$ is the instantaneous driving voltage, where

$$v_{CEsat}(t) = f[i_C(t), T_j(t), V_{GE}], \tag{A2}$$

V_{GE} being the gate-emitter voltage and T_j the junction temperature of the device.

Similarly, the conduction losses of the anti-parallel diode during a switching period can be represented as:

$$P_{cond,D} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_F(t)\, i_F(t)\, dt, \tag{A3}$$

where v_F is the diode forward voltage and i_F is the instantaneous current circulating through the diode, being:

$$v_F(t) = f[i_F(t), T_j(t)], \tag{A4}$$

On the other hand, the switching losses are defined as the product of the switching frequency f_{sw} and the dissipated energy. Starting from the curve $E_{sw,Q} = f(i_C)$ provided by the manufacturer, and subsequently applying correction factors corresponding to the blocking voltage (V_{CE}), junction temperature (T_j), and gate resistance (R_G), accurate estimation of switching losses was obtained for IGBTs:

Table A1. Most significant parameters of the simulated power electronics system incorporating IRAUIRGPS4067D1 devices.

Parameter	Symbol	Value	Units
Nominal current per switch	$I_{C,nom}$	120	A
Maximum blocking voltage	$V_{CES,max}$	600	V
Typical collector-emitter voltage	$V_{CE,on}$	1.7	V
Typical turn-on switching loss	E_{ON}	8.2	mJ
Typical turn-off switching loss	E_{OFF}	2.9	mJ
Typical diode reverse recovery	E_{REC}	2.4	mJ
Allowable junction temperature	T_{vj}	-55 to $+175$	°C

$$E_{sw,Q} = K_{V_{CE}} K_{T_j,Q} K_{R_G,Q} E_{sw}(i_C), \tag{A5}$$

where:

$$K_{V_{CE}} = \left(\frac{V_{CE}}{V_{CE,ref}}\right)^{K_{v,Q}}, \tag{A6}$$

$$K_{T_j,Q} = [1 + TC_{Esw,Q}(T_j - T_{j_{ref}})], \tag{A7}$$

$$K_{R_G,Q} = \frac{E_{on+off}(R_G)}{E_{on+off}(R_{G,ref})} \tag{A8}$$

where $K_{v,Q} = 1.3$ and $TC_{Esw,Q} = 0.003$.

The diode E_{rr} was calculated in a similar way, using again the corresponding correction factors:

$$E_{sw,D} = K_{V_F} K_{T_j,D} E_{sw}(i_D, R_G), \tag{A9}$$

where

$$K_{V_F} = \left(\frac{V_D}{V_{D,ref}}\right)^{K_{v,D}}, \tag{A10}$$

$$K_{T_j,D} = [1 + TC_{Esw,D}(T_j - T_{j_{ref}})] \tag{A11}$$

where $K_{v,Q} = 0.6$ and $TC_{Esw,Q} = 0.0065$.

In this context, the determination of v_{CEsat}, v_F, $E_{sw,Q}$, and $E_{sw,D}$ was implemented via 1D and 2D look-up tables (LUT), while the corresponding correction factors were applied, when required, over the outputs of such LUTs.

The total instantaneous inverter losses can be expressed as:

$$P_{tot,inv} = \sum_{i=0}^{N}(P_{cond,Q_i} + P_{sw,Q_i}) + \sum_{j=0}^{M}(P_{cond,D_j} + P_{sw,D_j}), \tag{A12}$$

where N and M are the number of IGBTs and diodes that constitute the converter, respectively.

Finally, the thermal behavior of the power semiconductors was characterized using equivalent Cauer networks from data provided by the manufacturer. A single Cauer network (consisting of three nodes for IGBTs and four nodes for diodes) was used to model the vertical heat transfer of each semiconductor. These Cauer networks were connected in parallel to the heat sink thermal model (Figure A1). Table A2 shows the thermal resistance and capacitance values used for the simulations. The implementation of the thermal model was straightforward, as the SimPowerSystems toolbox was used for this purpose. Current sources at the input of each device equivalent thermal network represent the instantaneous power losses, while the input voltage represents their instantaneous virtual junction temperatures.
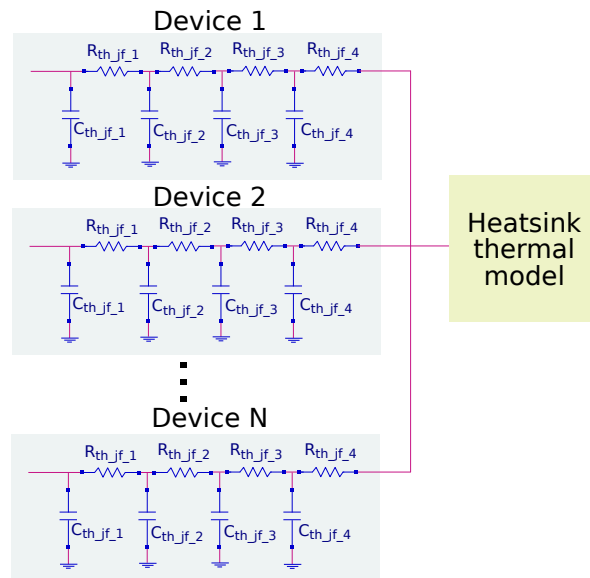

Figure A1. General diagram of the implemented thermal model.

Table A2. Thermal resistances and capacitances of the AUIRGPS4067D1 IGBTs and diodes for equivalent Cauer networks.

Parameter	Symbol	Value	Units
IGBT thermal resistances	$R_{th1,IGBT}$	0.0564	°C/W
	$R_{th2,IGBT}$	0.0888	
	$R_{th3,IGBT}$	0.0547	
IGBT thermal capacitances	$C_{th1,IGBT}$	0.0045	Ws/°C
	$C_{th2,IGBT}$	0.0355	
	$C_{th3,IGBT}$	0.2723	
IGBT thermal resistances	$R_{th1,IGBT}$	0.0060	°C/W
	$R_{th2,IGBT}$	0.1404	
	$R_{th3,IGBT}$	0.1912	
	$R_{th4,IGBT}$	0.1016	
Diode thermal capacitances	$C_{th1,IGBT}$	0.0027	Ws/°C
	$C_{th2,IGBT}$	0.0028	
	$C_{th3,IGBT}$	0.0214	
	$C_{th4,IGBT}$	0.2092	

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