Universidad del País Vasco Euskal Herriko Unibertsitatea

BILBOKO INGENIARITZA ESKOLA
ESCUELA DE INGENIERÍA DE BILBAO

INDUSTRIA ELEKTRONIKAREN ETA AUTOMATIKAREN INGENIARITZAKO GRADUA

GRADU AMAIERAKO LANA

TRESNA ELEKTRONIKOENTZAKO KARGAGAILU FOTOVOLTAIKO BATEN DISEINUA, SIMULAZIOA ETA PROTOTIPAKETA

I ERANSKINA – *EZAUGARRI ORRIAK*

Ikaslea: Jorge, Aristorena, Asier

Zuzendaria: Otaegi, Aizpeolea, Aloña

Ikasturtea: 2020-2021

Data: Bilbon, 2021eko ekainaren 25ean

Aurkibidea

ATMega 328P

Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 4/8/16/32K Bytes of In-System Self-Programmable Flash progam memory (ATmega48PA/88PA/168PA/328P)
  - 256/512/512/1K Bytes EEPROM (ATmega48PA/88PA/168PA/328P)
  - 512/1K/1K/2K Bytes Internal SRAM (ATmega48PA/88PA/168PA/328P)
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C(1)
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Six PWM Channels
  - 8-channel 10-bit ADC in TQFP and QFN/MLF package
    - Temperature Measurement
  - 6-channel 10-bit ADC in PDIP Package
    - Temperature Measurement
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Byte-oriented 2-wire Serial Interface (Philips I^2C compatible)
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-pin PDIP, 32-lead TQFP, 28-pad QFN/MLF and 32-pad QFN/MLF
- Operating Voltage:
  - 1.8 - 5.5V for ATmega48PA/88PA/168PA/328P
- Temperature Range:
  - -40°C to 85°C
- Speed Grade:
  - 0 - 20 MHz @ 1.8 - 5.5V
- Low Power Consumption at 1 MHz, 1.8V, 25°C for ATmega48PA/88PA/168PA/328P:
  - Active Mode: 0.2 mA
  - Power-down Mode: 0.1 µA
  - Power-save Mode: 0.75 µA (Including 32 kHz RTC)

8-bit AVR® Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash

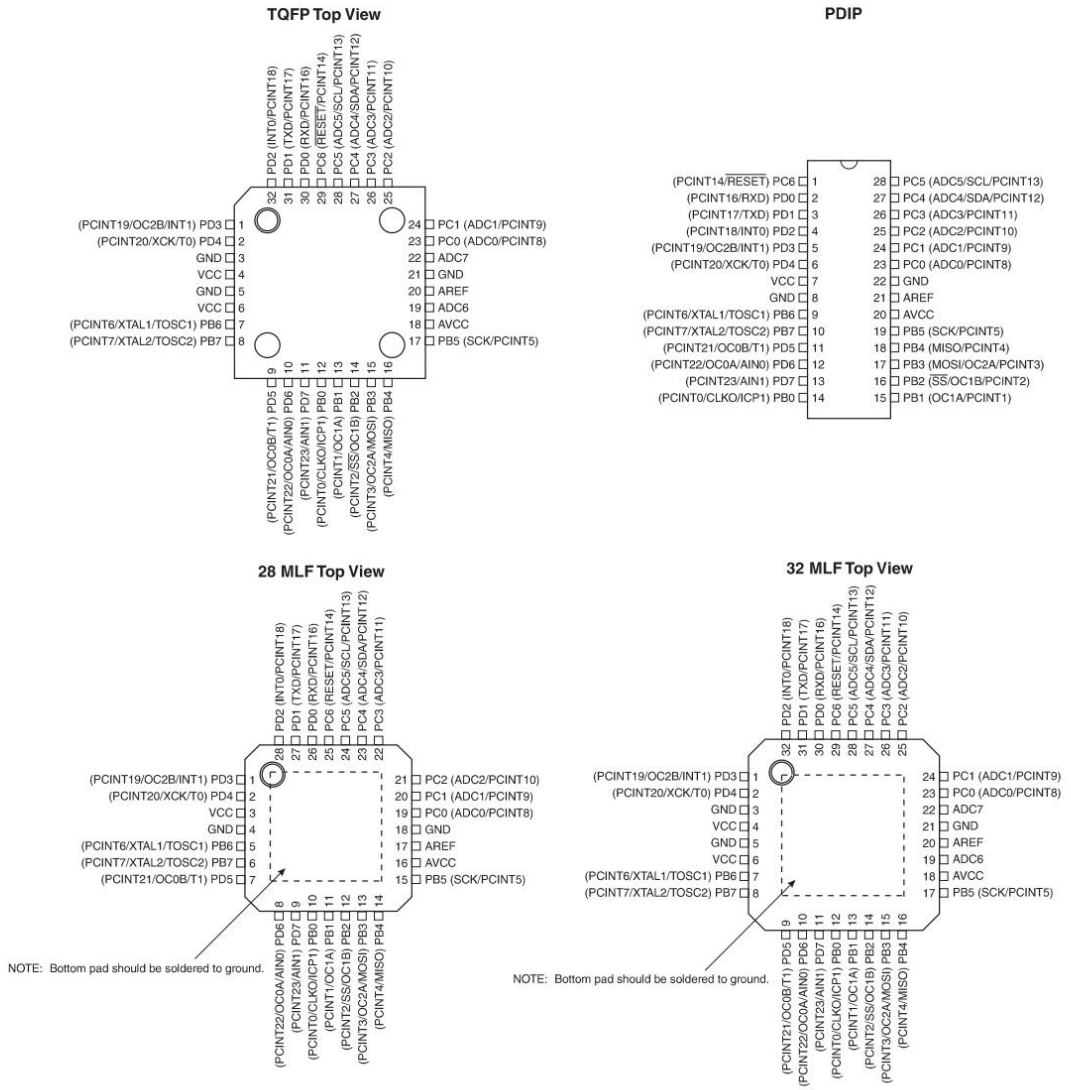
ATmega48PA
ATmega88PA
ATmega168PA
ATmega328P

Summary

Rev. 8161DS–AVR–10/09

1. Pin Configurations

Figure 1-1. Pinout ATmega48PA/88PA/168PA/328P



1.1 Pin Descriptions

1.1.1 VCC

Digital supply voltage.

1.1.2 GND

Ground.

1.1.3 Port B (PB7:0) XTAL1/XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of Port B are elaborated in "Alternate Functions of Port B" on page 76 and "System Clock and Clock Options" on page 26.

1.1.4 Port C (PC5:0)

Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PC5..0 output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

1.1.5 PC6/$\overline{\text{RESET}}$

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in Table 28-3 on page 308. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated in "Alternate Functions of Port C" on page 79.

1.1.6 Port D (PD7:0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

The various special features of Port D are elaborated in "Alternate Functions of Port D" on page 82.

1.1.7 AV_{CC}

AV_{CC} is the supply voltage pin for the A/D Converter, PC3:0, and ADC7:6. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that PC6..4 use digital supply voltage, V_{CC}.

1.1.8 AREF

AREF is the analog reference pin for the A/D Converter.

1.1.9 ADC7:6 (TQFP and QFN/MLF Package Only)

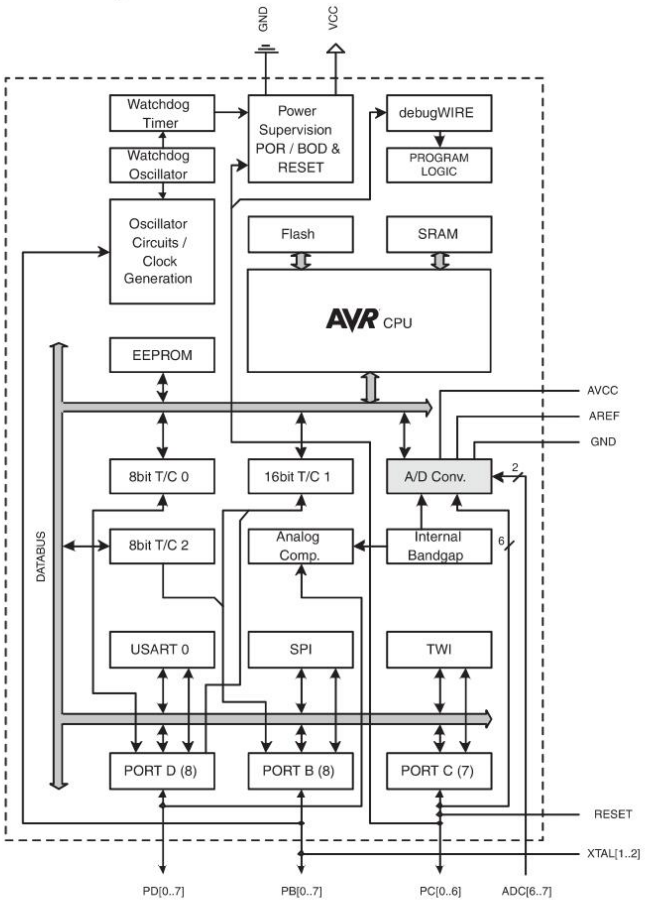
In the TQFP and QFN/MLF package, ADC7:6 serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

2. Overview

The ATmega48PA/88PA/168PA/328P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega48PA/88PA/168PA/328P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting

architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega48PA/88PA/168PA/328P provides the following features: 4/8/16/32K bytes of In-System Programmable Flash with Read-While-Write capabilities, 256/512/512/1K bytes EEPROM, 512/1K/1K/2K bytes SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte-oriented 2-wire Serial Interface, an SPI serial port, a 6-channel 10-bit ADC (8 channels in TQFP and QFN/MLF packages), a programmable Watchdog Timer with internal Oscillator, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire Serial Interface, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega48PA/88PA/168PA/328P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega48PA/88PA/168PA/328P AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2.2 Comparison Between ATmega48PA, ATmega88PA, ATmega168PA and ATmega328P

The ATmega48PA, ATmega88PA, ATmega168PA and ATmega328P differ only in memory sizes, boot loader support, and interrupt vector sizes. Table 2-1 summarizes the different memory and interrupt vector sizes for the three devices.

Table 2-1. Memory Size Summary

Device	Flash	EEPROM	RAM	Interrupt Vector Size
ATmega48PA	4K Bytes	256 Bytes	512 Bytes	1 instruction word/vector
ATmega88PA	8K Bytes	512 Bytes	1K Bytes	1 instruction word/vector
ATmega168PA	16K Bytes	512 Bytes	1K Bytes	2 instruction words/vector
ATmega328P	32K Bytes	1K Bytes	2K Bytes	2 instruction words/vector

ATmega88PA, ATmega168PA and ATmega328P support a real Read-While-Write Self-Programming mechanism. There is a separate Boot Loader Section, and the SPM instruction can only execute from there. In ATmega48PA, there is no Read-While-Write support and no separate Boot Loader Section. The SPM instruction can execute from the entire Flash.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

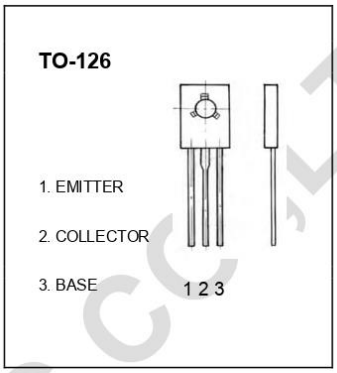
BD139

WEJ®

RoHS

BD135/137/139

BD135/BD137/BD139 TRANSISTOR (NPN)



FEATURES

Power dissipation

P_{CM}: 1.25 W (Tamb=25℃)

Collector current

I_{CM}: 1.5 A

Operating and storage junction temperature range

T_J, T_{stg}: -55℃ to +150℃

ELECTRICAL CHARACTERISTICS (Tamb=25℃ unless otherwise specified)

Parameter	Symbol	Test conditions		MIN	TYP	MAX	UNIT
Collector-base breakdown voltage	$V_{(BR)CBO}$	I_C=100μA, I_E=0	BD135	45			V
			BD137	60			
			BD139	80			
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	I_C=30mA, I_B=0	BD135	45			V
			BD137	60			
			BD139	80			
Emitter-base breakdown voltage	$V_{(BR)EBO}$	I_E=100μA, I_C=0		5			V
Collector cut-off current	I_{CBO}	V_{CB}=30V, I_E=0				0.1	μA
Emitter cut-off current	I_{EBO}	V_{EB}=5V, I_C=0				10	μA
DC current gain	$h_{FE(1)}$	V_{CE}=2V, I_C=5mA		25			
	$h_{FE(2)}$	V_{CE}=2V, I_C=150mA	BD135	40		250	
			BD137/BD139	40		160	
	$h_{FE(3)}$	V_{CE}=2V, I_C=500mA		25			
Collector-emitter saturation voltage	$V_{CE(sat)}$	I_C=500mA, I_B=50mA				0.5	V
Base-emitter voltage	V_{BE}	V_{CE}=2V, I_C=500mA				1	V

CLASSIFICATION OF $h_{FE(2)}$

Rank	6	10	16
Range	40-100	63-160	100-250

 Http:// www.wej.cn E-mail:wej@yongerjia.com

MBR3045CT

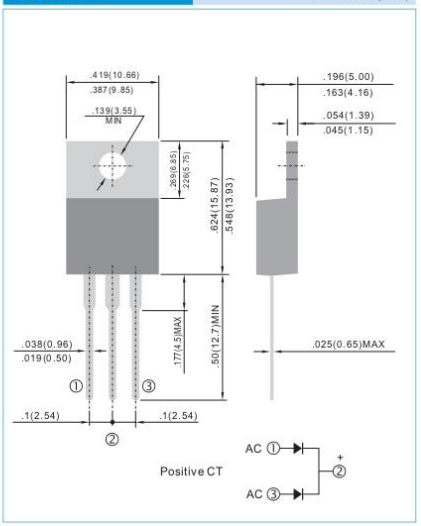
MBR3020CT~MBR30100CT

KERSEMI

SCHOTTKY BARRIER RECTIFIERS

VOLTAGE 20 to 100 Volts **CURRENT** 30.0 Amperes

TO-220AB Unit : inch (mm)



FEATURES

- Plastic package has Underwriters Laboratory Flammability Classification 94V-O. Flame Retardant Epoxy Molding Compound.
- Exceeds environmental standards of MIL-S-19500/228
- Low power loss, high efficiency.
- Low forwrd voltge, high current capability
- High surge capacity.
- For use in low voltage,high frequency inverters free wheeling , and polarlity protection applications.
- In compliance with EU RoHS 2002/95/EC directives

MECHANICAL DATA

- Case: TO-220AB Molded plastic
- Terminals: Solder plated, solderable per MIL-STD-750, Method 2026
- Polarity: As marked.
- Standard packaging: Any
- Weight: 0.083 ounces, 2.24grams.

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified. Single phase, half wave, 60 Hz, resistive or inductive load.

For capacitive load, derate current by 20%

PARAMETER	SYMBOL	MBR3020CT	MBR3030CT	MBR3035CT	MBR3040CT	MBR3045CT	MBR3045CT	MBR3050CT	MBR3060CT	MBR3080CT	MBR30100CT	UNITS
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	20	30	35	40	45	45	50	60	80	100	V
Maximum RMS Voltage	V_{RMS}	14	21	24.5	28	31.5	31.5	35	42	56	70	V
Maximum DC Blocking Voltage	V_{DC}	20	30	35	40	45	45	50	60	80	100	V
Maximum Average Forward Current lead length at T_C=90°C	$I_{F(AV)}$	30										A
Peak Forward Surge Current :8.3ms single half sine-wave superimposed on rated load(JEDEC method)	I_{FSM}	275										A
Maximum Forward Voltage at 15A, per leg	V_F	0.55						0.70		0.80		V
Maximum DC Reverse Current T_J=25 °C at Rated DC Blocking Voltage T_J=100°C	I_R	0.1 20										mA
Typical Thermal Resistance	$R_{\theta JC}$	1.5										°C / W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-50 TO + 150										°C

www.kersemi.com

MBR3020CT~MBR30100CT

KERSEMI

RATING AND CHARACTERISTIC CURVES

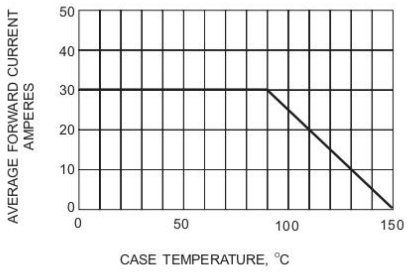


Fig.1- FORWARD CURRENT DERATING CURVE

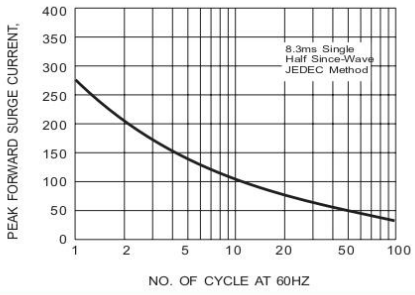


Fig.2- MAXIMUM NON - REPETITIVE SURGE CURRENT

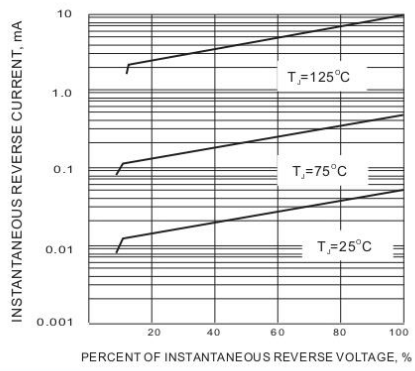


Fig.3- TYPICAL REVERSE CHARACTERISTICS

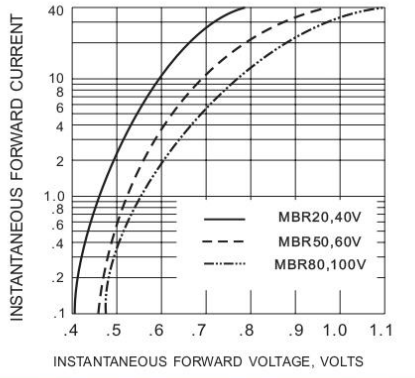


Fig.4- TYPICAL INSTANTANEOUS FORWARD CHARACTERISTICS

LEGAL STATEMENT

www.kersemi.com

MC34063A

Order this document by MC34063A/D

MOTOROLA

MC34063A
MC33063A

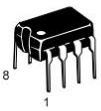
DC-to-DC Converter Control Circuits

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC–to–DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step–Down and Step–Up and Voltage–Inverting applications with a minimum number of external components. Refer to Application Notes AN920A/D and AN954/D for additional design information.

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

DC–to–DC CONVERTER CONTROL CIRCUITS

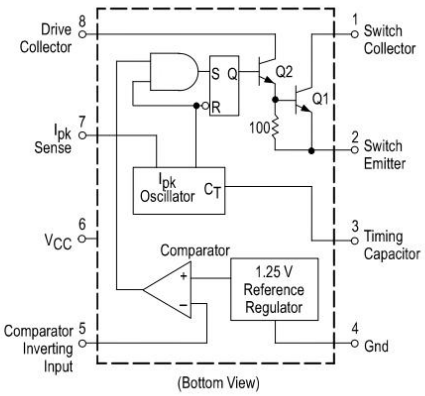
SEMICONDUCTOR TECHNICAL DATA



P, P1 SUFFIX
PLASTIC PACKAGE
CASE 626

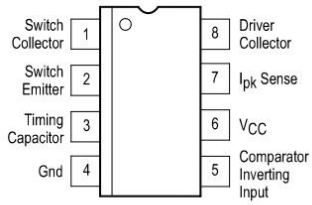
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Schematic Diagram



This device contains 51 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33063AD	T_A = – 40° to +85°C	SO–8
MC33063AP1		Plastic DIP
MC33063AVD	T_A = –40° to +125°C	SO–8
MC33063AVP		Plastic DIP
MC34063AD	T_A = 0° to +70°C	SO–8
MC34063AP1		Plastic DIP

 Rev 5

MC34063A MC33063A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	−0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{Pin\ 1}$ = 40 V)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	A
Power Dissipation and Thermal Characteristics Plastic Package, P, P1 Suffix T_A = 25°C Thermal Resistance SOIC Package, D Suffix T_A = 25°C Thermal Resistance	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 1.25 100 625 160	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range MC34063A MC33063AV MC33063A	T_A	 0 to +70 −40 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES: 1. Maximum package power dissipation limits must be observed.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency ($V_{Pin\ 5}$ = 0 V, C_T = 1.0 nF, T_A = 25°C)	f_{osc}	24	33	42	kHz
Charge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{chg}	24	35	42	µA
Discharge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{dischg}	140	220	260	µA
Discharge to Charge Current Ratio (Pin 7 to V_{CC}, T_A = 25°C)	I_{dischg}/I_{chg}	5.2	6.5	7.5	–
Current Limit Sense Voltage (I_{chg} = I_{dischg}, T_A = 25°C)	$V_{ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (Note 4)					
Saturation Voltage, Darlington Connection (Note 5) (I_{SW} = 1.0 A, Pins 1, 8 connected)	$V_{CE(sat)}$	–	1.0	1.3	V
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, $R_{Pin\ 8}$ = 82 Ω to V_{CC}, Forced β ≃ 20)	$V_{CE(sat)}$	–	0.45	0.7	V
DC Current Gain (I_{SW} = 1.0 A, V_{CE} = 5.0 V, T_A = 25°C)	h_{FE}	50	75	–	–
Collector Off–State Current (V_{CE} = 40 V)	$I_{C(off)}$	–	0.01	100	µA

NOTES: 3. T_{low} = 0°C for MC34063A, −40°C for MC33063A, AV T_{high} = +70°C for MC34063A, +85°C for MC33063A, +125°C for MC33063AV
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs for it to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended:

Forced β of output switch : $\frac{I_C \text{ output}}{I_C \text{ driver} - 7.0 \text{ mA}^*} \geq 10$

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage T_A = 25°C T_A = T_{low} to T_{high}	V_{th}	 1.225 1.21	 1.25 –	 1.275 1.29	V
Threshold Voltage Line Regulation (V_{CC} = 3.0 V to 40 V) MC33063A, MC34063A MC33363AV	Reg_{line}	 – –	 1.4 1.4	 5.0 6.0	mV
Input Bias Current (V_{in} = 0 V)	I_{IB}	–	–20	–400	nA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th}, Pin 2 = Gnd, remaining pins open)	I_{CC}	–	–	4.0	mA

NOTES: 3. T_{low} = 0°C for MC34063A, –40°C for MC33063A, AV T_{high} = +70°C for MC34063A, +85°C for MC33063A, +125°C for MC33063AV
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5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs for it to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended:

Forced β of output switch : $\frac{I_{C\ output}}{I_{C\ driver} - 7.0\ mA^*} \geq 10$

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor

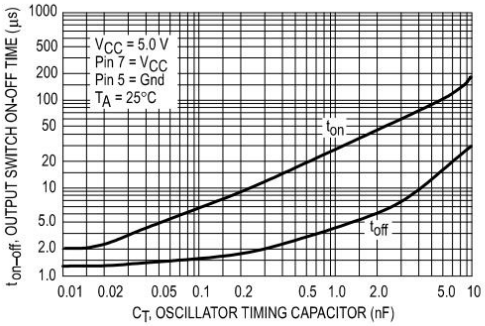


Figure 2. Timing Capacitor Waveform

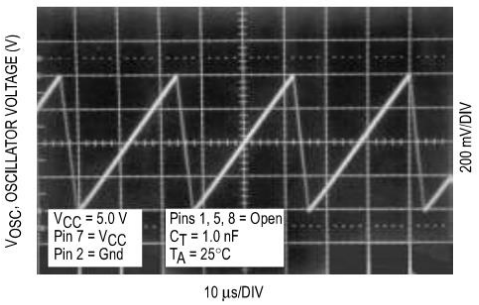


Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

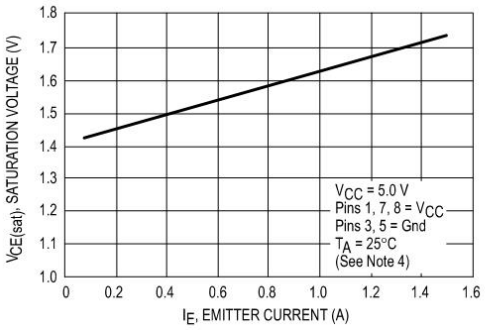


Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

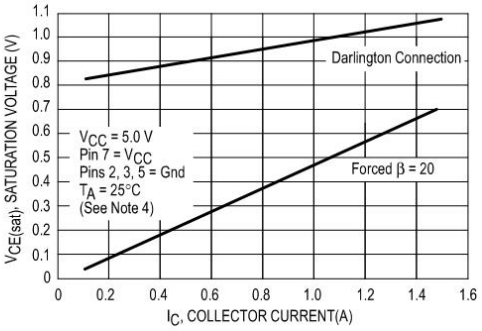


Figure 5. Current Limit Sense Voltage versus Temperature

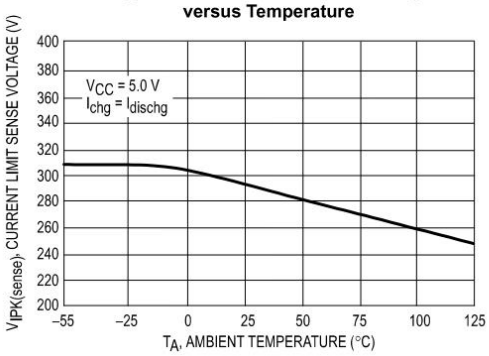
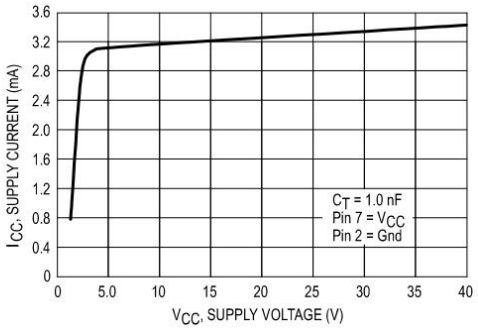
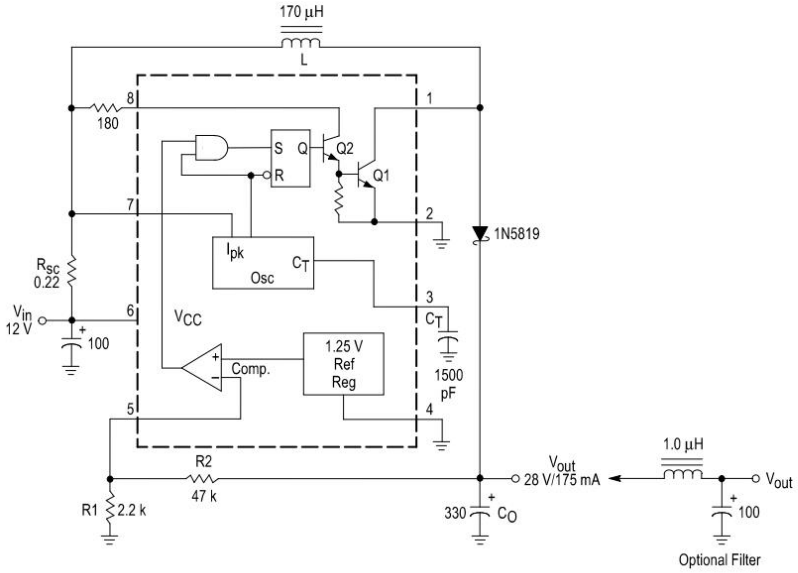


Figure 6. Standby Supply Current versus Supply Voltage



NOTE: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

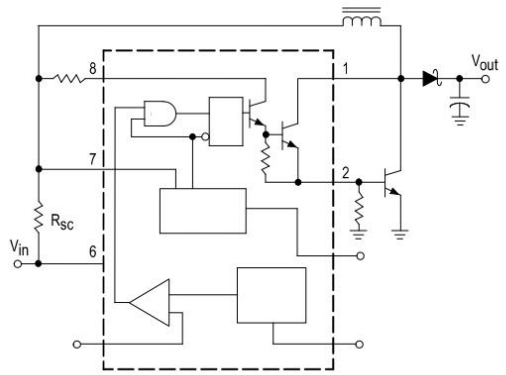
Figure 7. Step–Up Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 16 V, I_O = 175 mA	30 mV = ±0.05%
Load Regulation	V_{in} = 12 V, I_O = 75 mA to 175 mA	10 mV = ±0.017%
Output Ripple	V_{in} = 12 V, I_O = 175 mA	400 mVpp
Efficiency	V_{in} = 12 V, I_O = 175 mA	87.7%
Output Ripple With Optional Filter	V_{in} = 12 V, I_O = 175 mA	40 mVpp

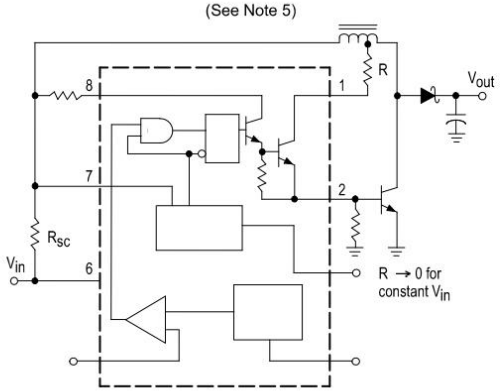
Figure 8. External Current Boost Connections for I_C Peak Greater than 1.5 A

8a. External NPN Switch



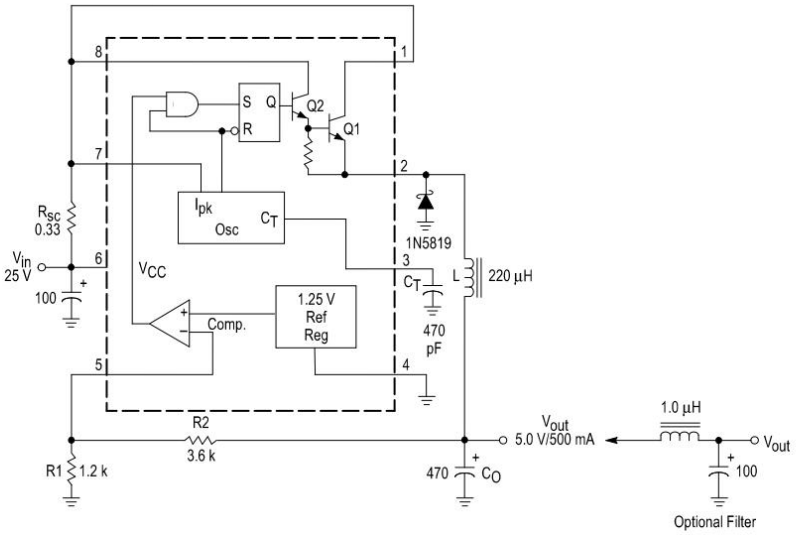
8b. External NPN Saturated Switch

(See Note 5)



NOTE: 5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended.

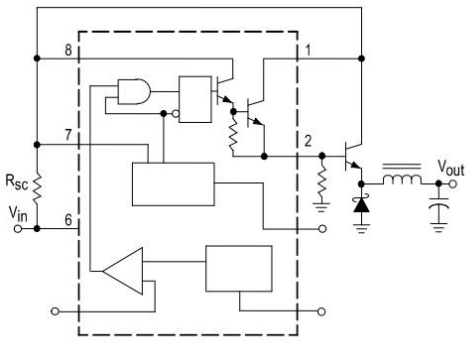
Figure 9. Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 15 V to 25 V, I_O = 500 mA	12 mV = ±0.12%
Load Regulation	V_{in} = 25 V, I_O = 50 mA to 500 mA	3.0 mV = ±0.03%
Output Ripple	V_{in} = 25 V, I_O = 500 mA	120 mVpp
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	1.1 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	83.7%
Output Ripple With Optional Filter	V_{in} = 25 V, I_O = 500 mA	40 mVpp

Figure 10. External Current Boost Connections for I_C Peak Greater than 1.5 A

10a. External NPN Switch



10b. External PNP Saturated Switch

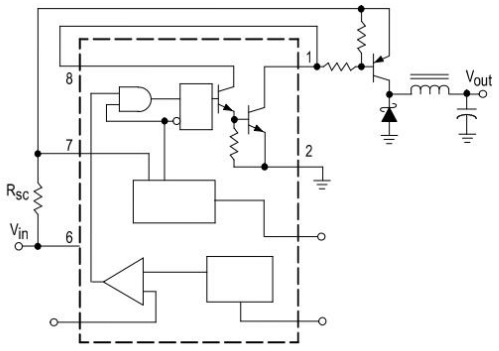
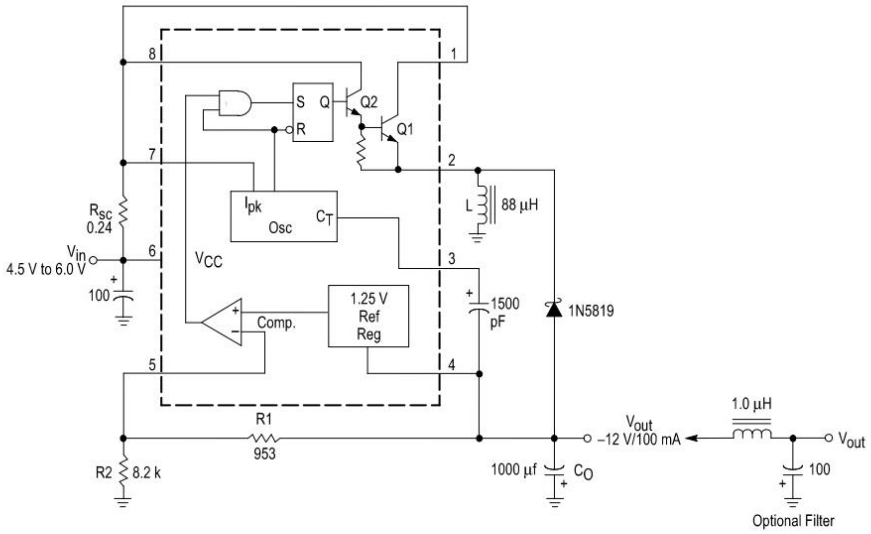


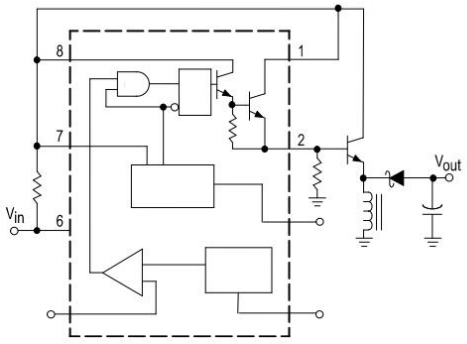
Figure 11. Voltage Inverting Converter



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 V to 6.0 V, I_O = 100 mA	3.0 mV = ±0.012%
Load Regulation	V_{in} = 5.0 V, I_O = 10 mA to 100 mA	0.022 V = ±0.09%
Output Ripple	V_{in} = 5.0 V, I_O = 100 mA	500 mVpp
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{in} = 5.0 V, I_O = 100 mA	62.2%
Output Ripple With Optional Filter	V_{in} = 5.0 V, I_O = 100 mA	70 mVpp

Figure 12. External Current Boost Connections for I_C Peak Greater than 1.5 A

12a. External NPN Switch



12b. External PNP Saturated Switch

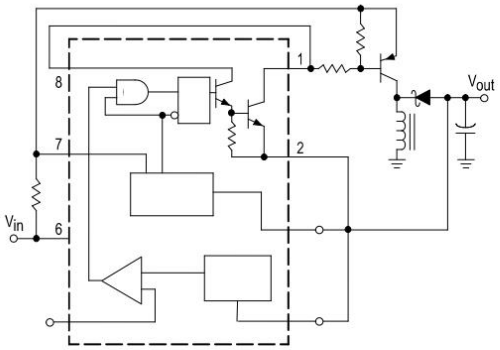
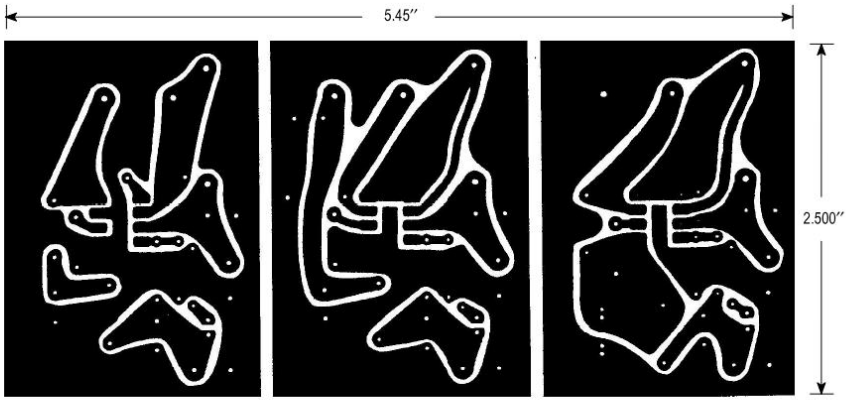
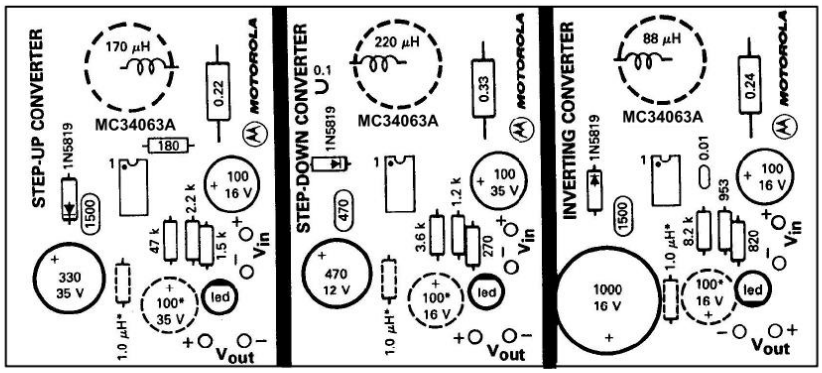


Figure 13. Printed Circuit Board and Component Layout
(Circuits of Figures 7, 9, 11)



(Top view, copper foil as seen through the board from the component side)



(Top View, Component Side) *Optional Filter.

INDUCTOR DATA

Converter	Inductance (µH)	Turns/Wire
Step–Up	170	38 Turns of #22 AWG
Step–Down	220	48 Turns of #22 AWG
Voltage–Inverting	88	28 Turns of #22 AWG

All inductors are wound on Magnetics Inc. 55117 toroidal core.

Figure 14. Design Formula Table

Calculation	Step–Up	Step–Down	Voltage–Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1\right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1\right)$
R_{sc}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$9\,\frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9\,\frac{I_{out} t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

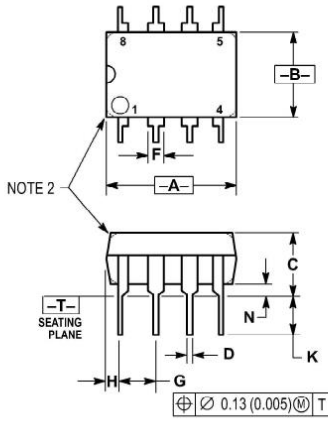
V_{in} – Nominal input voltage.
V_{out} – Desired output voltage, $\lvert V_{out}\rvert = 1.25 \left(1 + \frac{R2}{R1}\right)$
I_{out} – Desired output current.
f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_O.
$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

NOTE: For further information refer to Application Note AN920A/D and AN954/D.

MC34063A MC33063A

OUTLINE DIMENSIONS

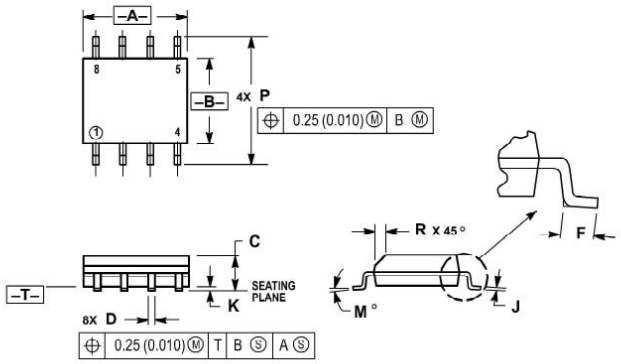
P, P1 SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE P



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TC1262

MICROCHIP

TC1262

500mA Fixed Output CMOS LDO

Features

- Very Low Dropout Voltage
- 500mA Output Current
- High Output Voltage Accuracy
- Standard or Custom Output Voltages
- Over Current and Over Temperature Protection

Applications

- Battery Operated Systems
- Portable Computers
- Medical Instruments
- Instrumentation
- Cellular/GSM/PHS Phones
- Linear Post-Regulators for SMPS
- Pagers

Device Selection Table

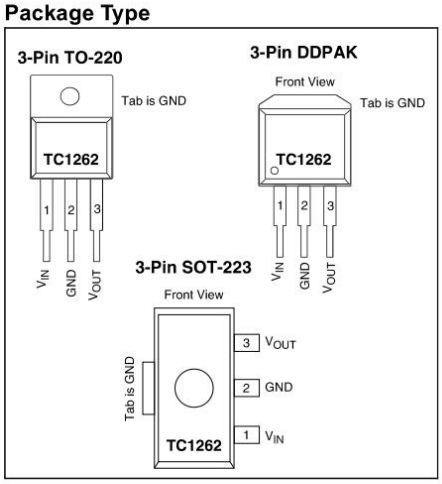
Part Number	Package	Junction Temp. Range
TC1262-xxVDB	3-Pin SOT-223	-40°C to +125°C
TC1262-xxVAB	3-Pin TO-220	-40°C to +125°C
TC1262-xxVEB	3-Pin DDPAK	-40°C to +125°C

NOTE: xx indicates output voltages.

Available Output Voltages: 2.5, 2.8, 3.0, 3.3, 5.0.

Other output voltages are available. Please contact Microchip Technology Inc. for details.

Package Type



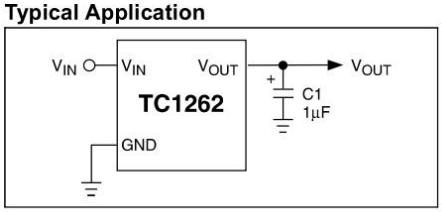
General Description

The TC1262 is a fixed output, high accuracy (typically ±0.5%) CMOS low dropout regulator. Designed specifically for battery-operated systems, the TC1262's CMOS construction eliminates wasted ground current, significantly extending battery life. Total supply current is typically 80μA at full load (20 to 60 times lower than in bipolar regulators).

TC1262 key features include ultra low noise operation, very low dropout voltage (typically 350mV at full load), and fast response to step changes in load.

The TC1262 incorporates both over temperature and over current protection. The TC1262 is stable with an output capacitor of only 1μF and has a maximum output current of 500mA. It is available in 3-Pin SOT-223, 3-Pin TO-220 and 3-Pin DDPAK packages.

Typical Application



TC1262

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Input Voltage 6.5V
Output Voltage..... (V_{SS} – 0.3V) to (V_{IN} + 0.3V)
Power Dissipation.....Internally Limited **(Note 6)**
Maximum Voltage on Any Pin ..... V_{IN} +0.3V to -0.3V
Operating Temperature Range..... -40°C < T_J < 125°C
Storage Temperature.....-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC1262 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: $V_{IN} = V_{OUT} + 1V$, $I_L = 100\mu A$, $C_L = 3.3\mu F$, $T_A = 25°C$, unless otherwise noted. **Boldface** type specifications apply for junction temperatures of -40°C to +125°C.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IN}	Input Operating Voltage	**2.7**	—	**6.0**	V	**Note 7**
I_{OUTMAX}	Maximum Output Current	**500**	—	—	mA	
V_{OUT}	Output Voltage	— **V_R – 2.5%**	V_R ±0.5% —	— **V_R + 2.5%**	V	**Note 1**
$\Delta V_{OUT}/\Delta T$	V_{OUT} Temperature Coefficient	—	40	—	ppm/°C	**Note 2**
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	—	.003	**0.35**	%/V	$(V_R + 1V) \le V_{IN} \le 6V$
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	—	0.002	**0.01**	%/mA	I_L = 0.1mA to I_{OUTMAX} **(Note 3)**
V_{IN}-V_{OUT}	Dropout Voltage	— — — 	20 60 200 350	**30** **130** **390** **650**	mV	I_L = 100µA I_L = 100mA I_L = 300mA I_L = 500mA **(Note 4)**
I_{DD}	Supply Current	—	80	**130**	µA	I_L = 0
PSRR	Power Supply Rejection Ratio	—	64	—	dB	$F_{RE} \le 1kHz$
I_{OUTSC}	Output Short Circuit Current	—	1200	—	mA	V_{OUT} = 0V
$\Delta V_{OUT}/\Delta P_D$	Thermal Regulation	—	0.04	—	V/W	**Note 5**
eN	Output Noise	—	260	—	nV/√Hz	$I_L = I_{OUTMAX}$, F_{RE} = 10kHz

Note 1: V_R is the regulator output voltage setting.

2: TC $V_{OUT} = \frac{(V_{OUTMAX} - V_{OUTMIN}) \times 10^6}{V_{OUT} \times \Delta T}$

3: Regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 0.1mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

4: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at a 1V differential.

5: Thermal Regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6V for T = 10 msec.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see Section 4.0 Thermal Considerations for more details.

7: The minimum V_{IN} has to justify the conditions: $V_{IN} \ge V_R + V_{DROPOUT}$ and $V_{IN} \ge$ 2.7V for I_L = 0.1mA to I_{OUTMAX}.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

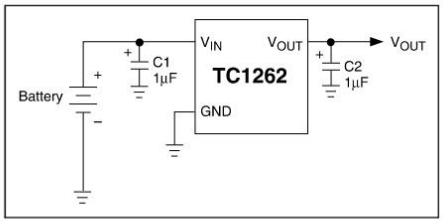
Pin No. (3-Pin SOT-223) (3-Pin TO-220) (3-Pin DDPAK)	Symbol	Description
1	V_{IN}	Unregulated supply input.
2	GND	Ground terminal.
3	V_{OUT}	Regulated voltage output.

3.0 DETAILED DESCRIPTION

The TC1262 is a precision, fixed output LDO. Unlike bipolar regulators, the TC1262's supply current does not increase with load current. In addition, V_{OUT} remains stable and within regulation over the entire 0mA to $I_{LOADMAX}$ load current range (an important consideration in RTC and CMOS RAM battery back-up applications).

Figure 3-1 shows a typical application circuit.

FIGURE 3-1: TYPICAL APPLICATION CIRCUIT



3.1 Output Capacitor

A 1µF (min) capacitor from V_{OUT} to ground is required. The output capacitor should have an effective series resistance greater than 0.1Ω and less than 5Ω, and a resonant frequency above 1MHz. A 1µF capacitor should be connected from V_{IN} to GND if there is more than 10 inches of wire between the regulator and the AC filter capacitor, or if a battery is used as the power source. Aluminum electrolytic or tantalum capacitor types can be used. (Since many aluminum electrolytic capacitors freeze at approximately -30°C, solid tantalums are recommended for applications operating below -25°C.) When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the value of the input and output capacitors and employing passive filtering techniques.

4.0 THERMAL CONSIDERATIONS

4.1 Thermal Shutdown

Integrated thermal protection circuitry shuts the regulator off when die temperature exceeds 160°C. The regulator remains off until the die temperature drops to approximately 150°C.

4.2 Power Dissipation

The amount of power the regulator dissipates is primarily a function of input and output voltage, and output current. The following equation is used to calculate worst case actual power dissipation:

EQUATION 4-1:

$$P_D \approx (V_{INMAX} - V_{OUTMIN})I_{LOADMAX}$$

Where:

P_D = Worst case actual power dissipation
V_{INMAX} = Maximum voltage on V_{IN}
V_{OUTMIN} = Minimum regulator output voltage
$I_{LOADMAX}$ = Maximum output (load) current

The maximum allowable power dissipation (Equation 4-2) is a function of the maximum ambient temperature (T_{AMAX}), the maximum allowable die temperature (TJ_{MAX}) and the thermal resistance from junction-to-air (θ_{JA}).

EQUATION 4-2:

$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$

Where all terms are previously defined.

Table 4-1 and Table 4-2 show various values of θ_{JA} for the TC1262 packages.

TABLE 4-1: THERMAL RESISTANCE GUIDELINES FOR TC1262 IN SOT-223 PACKAGE

Copper Area (Topside)*	Copper Area (Backside)	Board Area	Thermal Resistance (θ_{JA})
2500 sq mm	2500 sq mm	2500 sq mm	45°C/W
1000 sq mm	2500 sq mm	2500 sq mm	45°C/W
225 sq mm	2500 sq mm	2500 sq mm	53°C/W
100 sq mm	2500 sq mm	2500 sq mm	59°C/W
1000 sq mm	1000 sq mm	1000 sq mm	52°C/W
1000 sq mm	0 sq mm	1000 sq mm	55°C/W

*Tab of device attached to topside copper

TABLE 4-2: THERMAL RESISTANCE GUIDELINES FOR TC1262 IN 3-PIN DDPAK/TO-220 PACKAGE

Copper Area (Topside)*	Copper Area (Backside)	Board Area	Thermal Resistance (θ_{JA})
2500 sq mm	2500 sq mm	2500 sq mm	25°C/W
1000 sq mm	2500 sq mm	2500 sq mm	27°C/W
125 sq mm	2500 sq mm	2500 sq mm	35°C/W

*Tab of device attached to topside copper

Equation 4-1 can be used in conjunction with Equation 4-2 to ensure regulator thermal operation is within limits. For example:

Given:

V_{INMAX} = 3.3V ± 10%
V_{OUTMIN} = 2.7V ± 0.5%
$I_{LOADMAX}$ = 275mA
T_{JMAX} = 125°C
T_{AMAX} = 95°C
θ_{JA} = 59°C/W (SOT-223)

Find: 1. Actual power dissipation
2. Maximum allowable dissipation

Actual power dissipation:

$$P_D \approx (V_{INMAX} - V_{OUTMIN})I_{LOADMAX}$$
$$= [(3.3 \times 1.1) - (2.7 \times .995)]275 \times 10^{-3}$$
$$= 260mW$$

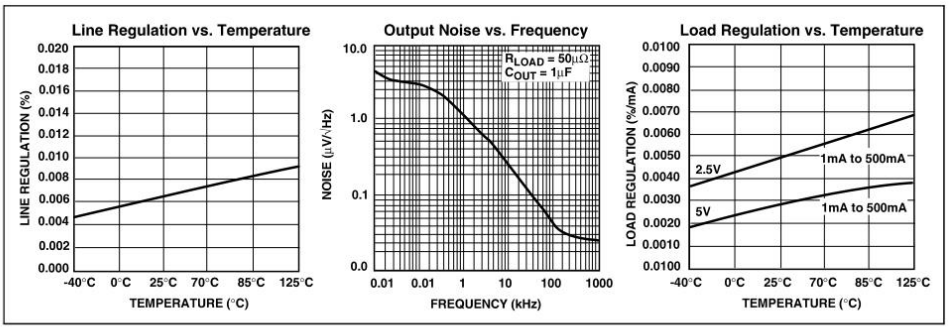
Maximum allowable power dissipation:

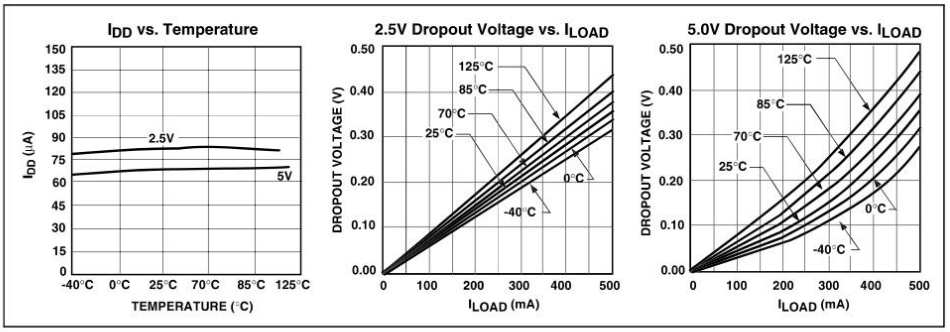
$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$
$$= \frac{(125 - 95)}{59}$$
$$= 508mW$$

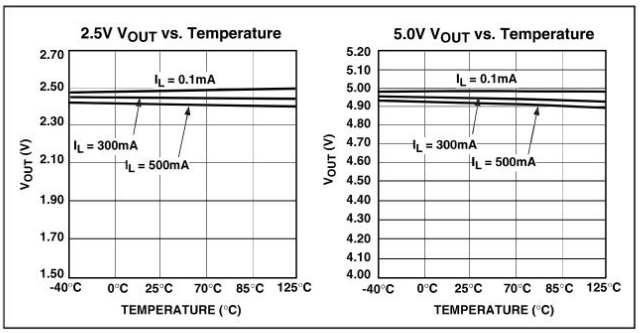
In this example, the TC1262 dissipates a maximum of 260mW; below the allowable limit of 508mW. In a similar manner, Equation 4-1 and Equation 4-2 can be used to calculate maximum current and/or input voltage limits. For example, the maximum allowable V_{IN}, is found by sustituting the maximum allowable power dissipation of 508mW into Equation 4-1, from which V_{INMAX} = 4.6V.

5.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.







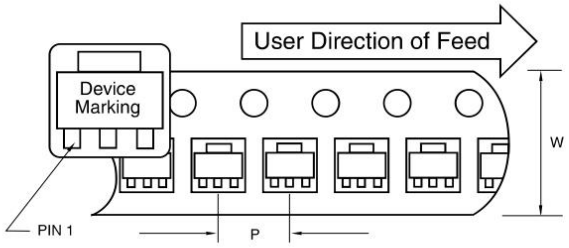
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

Package marking data not available at this time.

6.2 Taping Form

Component Taping Orientation for 3-Pin SOT-223 Devices

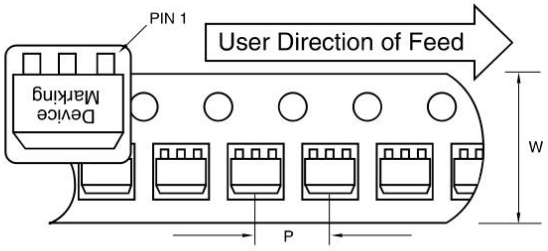


Standard Reel Component Orientation
for TR Suffix Device
(Mark Right Side Up)

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
3-Pin SOT-223	12 mm	8 mm	4000	13 in

Component Taping Orientation for 3-Pin DDPAK Devices



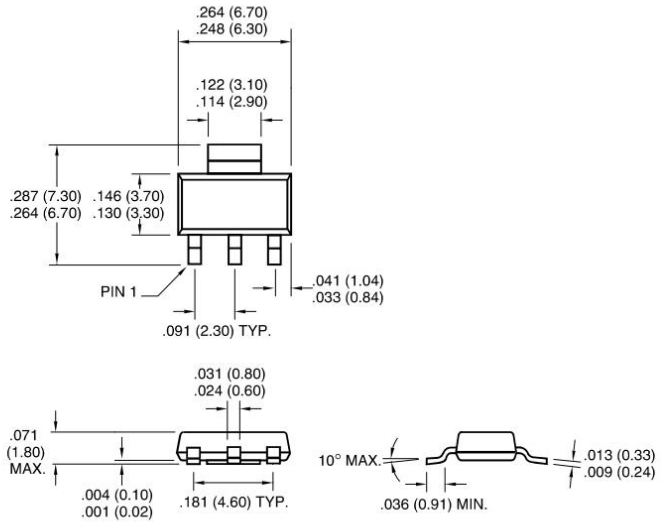
Standard Reel Component Orientation
for TR Suffix Device
(Mark Right Side Up)

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
3-Pin DDPAK	24 mm	16 mm	750	13 in

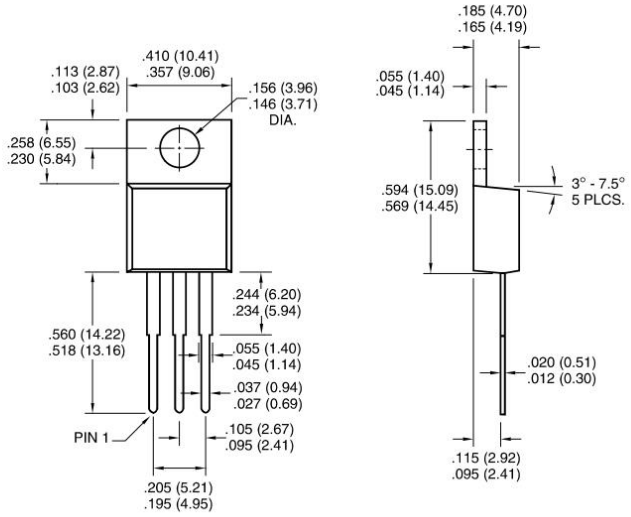
6.3 Package Dimensions

3-Pin SOT-223



Dimensions: inches (mm)

3-Pin TO-220

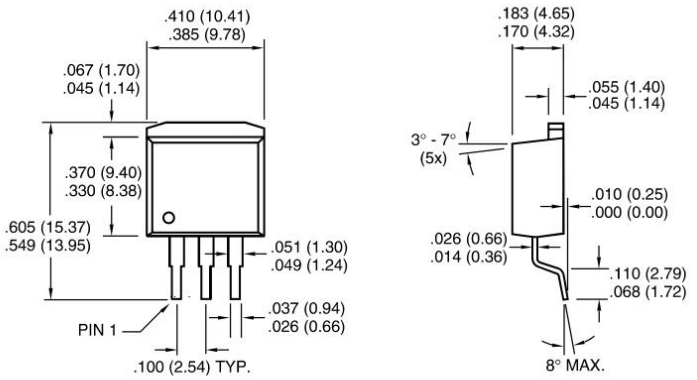


Dimensions: inches (mm)

TC1262

6.3 Package Dimensions (Continued)

3-Pin DDPAK



Dimensions: inches (mm)

TIP41C

TIP41/41A/41B/41C

THINKI SEMICONDUCTOR ®

Pb Free Plating Product

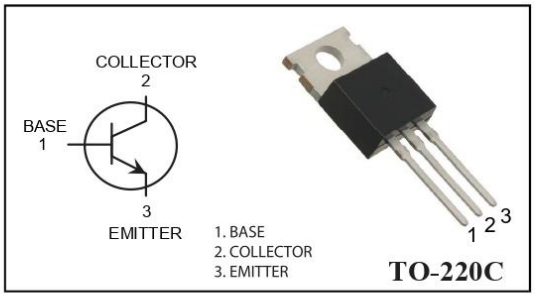
TIP41/TIP41A/TIP41B/TIP41C

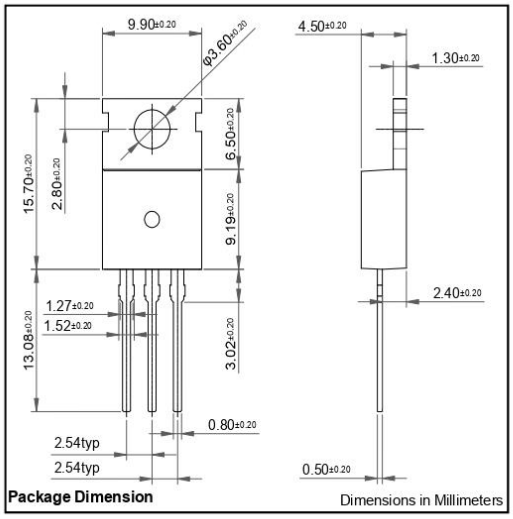
RoHS Pb

NPN Silicon Epitaxial Power Transistor

FEATURES:

* Medium Power Linear Switching Applications
* Complement to TIP42/TIP42A/TIP42B/TIP42C





MAXIMUM RATINGS (T_A=25℃ unless otherwise noted)

Symbol	Parameter	TIP41	TIP41A	TIP41B	TIP41C	Units
V_{CBO}	Collector-Base Voltage	40	60	80	100	V
V_{CEO}	Collector-Emitter Voltage	40	60	80	100	V
V_{EBO}	Emitter-Base Voltage	5				V
I_C	Collector Current -Continuous	6				A
P_C	Collector Power Dissipation	2				W
T_J	Junction Temperature	150				℃
T_{stg}	Storage Temperature	-55-150				℃

TIP41/41A/41B/41C

THINKI SEMICONDUCTOR ®

ELECTRICAL CHARACTERISTICS (Tamb=25℃ unless otherwise specified)

Parameter		Symbol	Test conditions	MIN	MAX	UNIT
Collector-base breakdown voltage	TIP41 TIP41A TIP41B TIP41C	$V_{(BR)CBO}$	I_C=1mA, I_E=0	40 60 80 100		V
Collector-emitter breakdown voltage	TIP41 TIP41A TIP41B TIP41C	$V_{(BR)CEO}$	I_C=30mA, I_B=0	40 60 80 100		V
Emitter-base breakdown voltage		$V_{(BR)EBO}$	I_E= 1mA, I_C=0	5		V
Collector cut-off current	TIP41 TIP41A TIP41B TIP41C	I_{CBO}	V_{CB}=40V, I_E=0 V_{CB}=60V, I_E=0 V_{CB}=80V, I_E=0 V_{CB}=100V, I_E=0		0.4	mA
Collector cut-off current	TIP41/41A TIP41B/41C	I_{CEO}	V_{CE}=30V, I_B=0 V_{CE}=60V, I_B=0		0.7	mA
Emitter cut-off current		I_{EBO}	V_{EB}=5V, I_C=0		1	mA
DC current gain		$h_{FE(1)}$	V_{CE}=4V, I_C=0.3A	30		
		$h_{FE(2)}$	V_{CE}=4V, I_C=3A	15	75	
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C=6A, I_B=0.6A		1.5	V
Base-emitter voltage		$V_{BE(on)}$	V_{CE}=4V, I_C=6A		2	V
Transition Frequency		f_T	V_{CE}=10V, I_C=0.5A f = 1MHz	3		MHz