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Wide Bandgap semiconductor HF-oscillation attenuation method with tuned gate RLC filter

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***Abstract*—Wide Bandgap (WBG) transistors provide better switching performance and higher operating temperatures compared to state of the art Si devices and are suited for high frequency applications due to very short switching times. The main obstacle for implementation of WBG transistors at full potential is the high frequency oscillation in voltage and current during switching transients. Oscillations arise from resonance due to parasitic and device inductances and capacitances. Introduction of WBG transistors depends on the elimination of these oscillations and their negative effect on the performance of power converters. Good layout practice is mandatory, but there is a limit to the reduction of these parasitics and, often, slowing of the semiconductor switching time must be applied. This paper presents a simple methodology for the attenuation of the negative effects of WBG transistor high frequency oscillations without increasing rise and fall times. The proposed methodology is based on determination of the source of feedback resonant frequency between gate and power loops using network analyzer measurement on PCB and utilization of tuned RLC filter. Experimental application of the methodology shows direct relationship between loop resonant frequency and voltage and current oscillations. The proposed method reduces power losses, high frequency oscillations and EMI.**

***Index Terms*—WBG, switching oscillation, switching losses, RLC filter.**

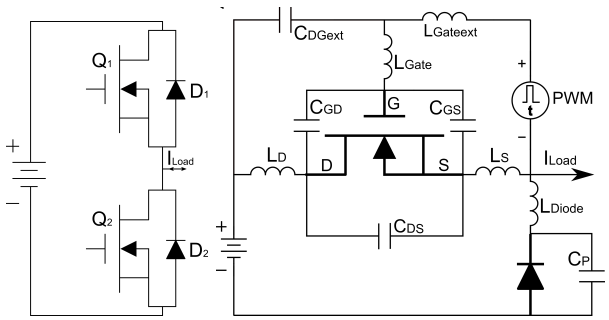
I. Introduction

Wide Bandgap (WBG) transistors have been introduced in power converters in order to improve several characteristics such as switching frequency, switching power losses, conduction losses, operating temperature and volume [1]–[3]. Comparative studies regarding efficiency and switching frequency between WBG semiconductors and Si devices seem to confirm a reduction in power losses of between 30% and 70% [4]–[22].

In spite of their advantages, the use of WBG devices presents high frequency gate-loop and power-loop oscillations due to parasitic effects (figure I, and great research effort has been oriented to reduce such parasitic effects and oscillation in the gate circuits [23]–[37].

Several solutions for oscillation suppression, with different levels of complexity have been presented:

1) Optimization of the designed layout in order to reduce general parasitic effects, and use low inductance devices [38]. External capacitor C_{GDext} (figure 1(b)) is critical and needs to be reduced by means of good layout design, and low $R_{DS(on)}$ and low inductive packages are required when using encapsulated semiconductors.
2) Introduction of snubber circuits. This solution, assisted by a snubber capacitor, reduces MOSFET V_{DS} ringing generated by the MOSFET, DC bus capacitor loop, but not those generated in the MOSFET gate-loop [39], [40].
3) Increase of gate resistance R_{Gate} [41]–[43]. An increment in the gate resistance slows down MOSFET current rising and falling time, reducing the oscillations (figure 2), at the expense of increasing switching time.
4) Use of ferrite beads on L_{Gate} series path to attenuate the gate-loop oscilation [44], [45]. In this case, there is an increase of gate series inductance path, with similar results to increasing gate resistance.
5) Using Active Gate Driver (AGD) solutions [46]–[49]. This solutions require complex gate driver design.



(a) Commutation branch. (b) Parasitics on PCell.

Figure 1. Commutation cell structure and PCell parasitic components.

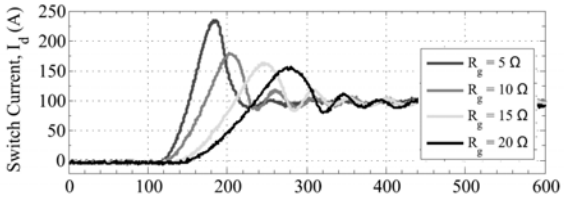


Figure 2. R_{Gate} influence at switching on [43].

These solutions either slow the switching waveforms of WBG transistors or require complicated gate drive designs. This paper proposes a novel methodology to determine the main oscillation source and a tuned RLC filter in the gate circuit to eliminate or attenuate the aforementioned oscillations. In section II the source of high frequency oscillations is studied. Section III presents a new method to tune a gate RLC filter trap to minimize high frequency oscillations. An experimental setup for validating the method is described

and the validation results are presented in section IV. These results show that this methodology can improve power designs and switching waveforms in power converters with WBG transistors are improved with a low cost and simple method.

II. Oscillation Sources

Figure 1(a) shows a typical branch present in many power converter topologies, such as inverters, DC/DC converters, etc. The branch can be separated into two commutation cells formed by an upper MOSFET (Q_1) and a lower Diode (D_2) and, alternatively, by an upper diode (D_1) and a lower MOSFET (Q_2). The upper MOSFET (Q_1) switches its current with the lower diode (D_2) when the load current is positive (this pair will be named PCell). The lower MOSFET (Q_2) switches its current with the upper diode (D_1) when the current is negative (this pair will be named NCell). Positive load current will circulate through the PCell and negative load current will circulate through the NCell.

Figure 1(b) shows the PCell with its parasitic elements, including intrinsic MOSFET capacitances (C_{GD}, C_{GS} and C_{DS}), diode capacitance (C_P), PCB or power module inductances (L_{Gate}, L_S, L_D, L_{Diode} and $L_{Gateext}$), and the externally added capacity (C_{GDext}) introduced by the PCB and the power module.

The oscillations of voltage and current during MOSFET switching can induce oscillations in the gate-loop through L_S and C_{GD} reducing performance [29]. Gate inductance (L_{Gate} and $L_{Gateext}$) is a key parameter in the gate-loop to provide stability to the application. Its value should be kept low and it should not exceed a few tens of nano Henries. High frequency oscillations in the gate can lead to Miller parasitic turn-on arising from the oscillations in C_{GS} [26] .

The loop formed by the external parasitic capacitor C_{GDext}, intrinsic MOSFET capacitor C_{GD}, L_D and L_{Gate} generate ringing [38]. These parameters are mainly affected by the layout design. This loop is affected by dv/dt and di/dt that exist during MOSFET switching, generating high frequency oscillating waveforms.

SiC MOSFETs have higher values of reverse transfer capacitance (C_{rss}) when compared to similar rating Si devices. A large C_{rss} capacitor can increase the possibility of having oscillations and consequently there may be a parasitic turn-on [27]. Another critical source of oscillations is the MOSFET-to-diode path inductance, L_S. It causes overshoot on MOSFET current at turn on, and voltage overshoot at turn off [28].

III. RLC Filter and Tuning Methodology

Direct observation of MOSFET drain current (I_{DS}), drain to source voltage (V_{DS}) and gate voltage (V_{GS}) often shows a match between the oscillation frequency of input gate and output current and voltage waveforms. Feedback from gate to power loop, and vice versa, amplifies the resonance, and pernicious high frequency oscillations arise in the MOSFET current and voltage.

A simple but effective solution to reduce amplification of the oscillations through the gate voltage consists on identifying the oscillation frequency, adding an RLC filter tuned to the feedback loop oscillation frequency. An adequately tuned RLC trap can avoid oscillation feedback between the power and gate loops and mitigate the high frequency oscillations in the voltage and current waveforms of the power converter. The RLC filter should be located as close to the gate as possible (figure 3). This will reduce the amount of feedback current leaking into the MOSFET gate and it will attenuate the power oscillations.

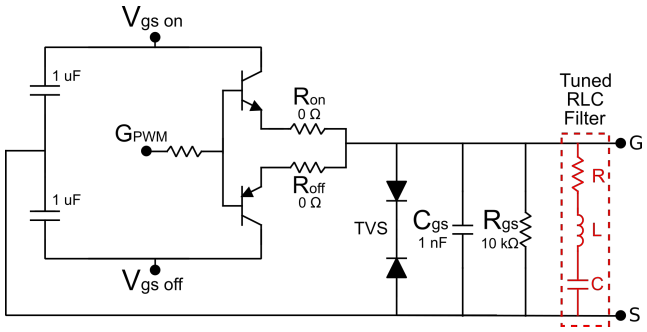
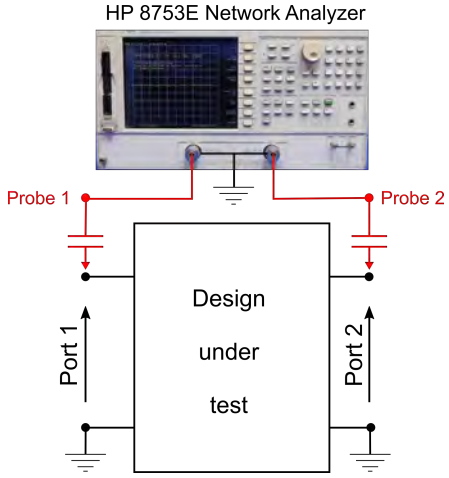
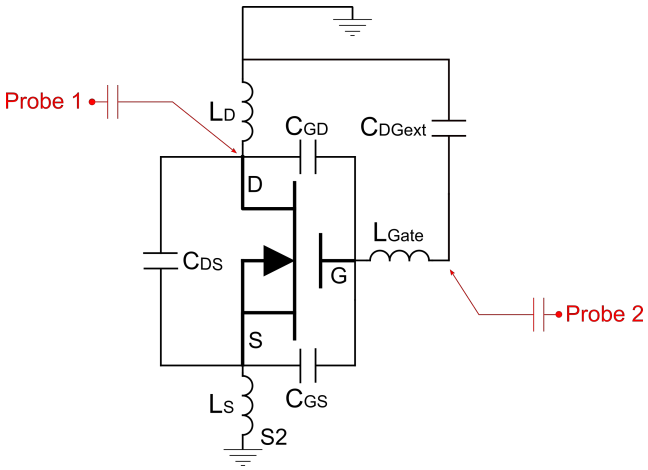


Figure 3. Gate driver circuit and proposed RLC filter.

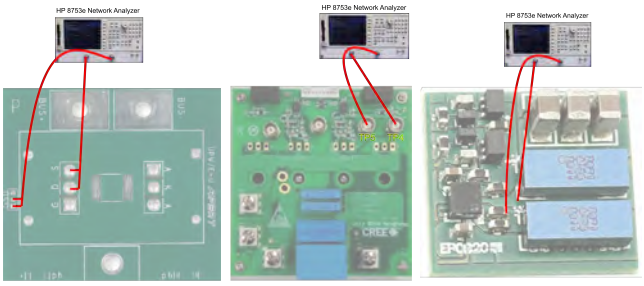


(a) Method - RF black box



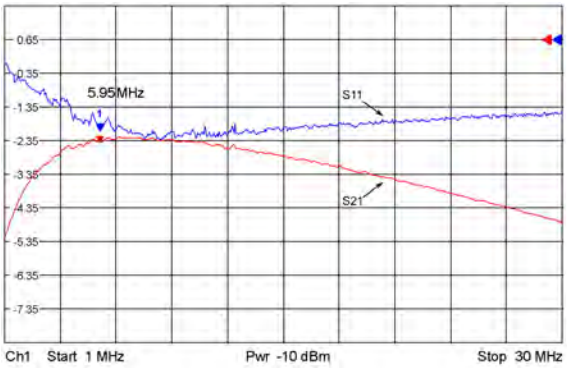
(b) Method - Parasitics schematic.

Figure 4. RF response analysis method.

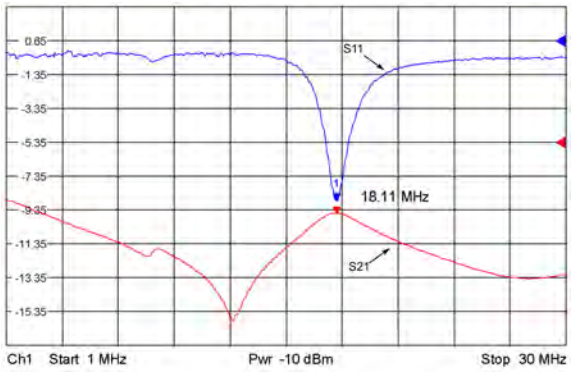


68 mm x 61 mm x 3 mm | 124 mm x 120 mm x 3 mm | 11 mm x 12 mm x 2 mm

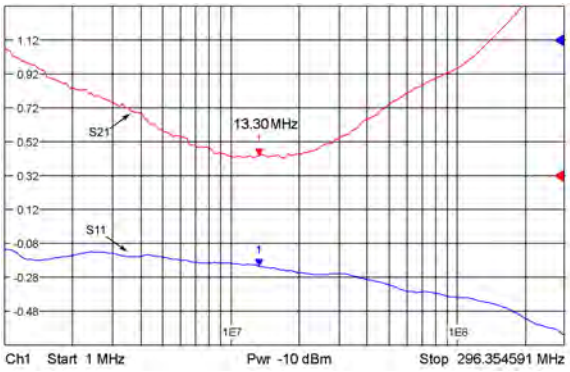
(a) PCell test setup. (b) Cree test setup. (c) GaN test setup.



(d) PCell S_{21} and S_{11} parameters.

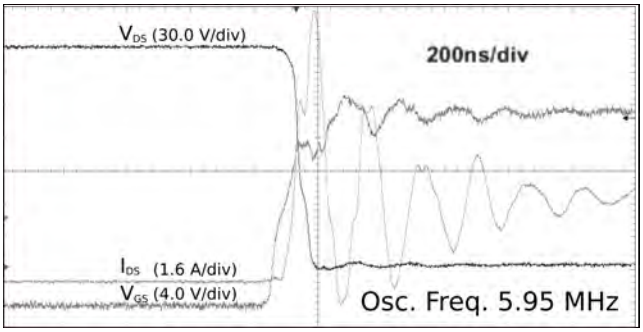


(e) Cree S_{21} and S_{11} parameters.

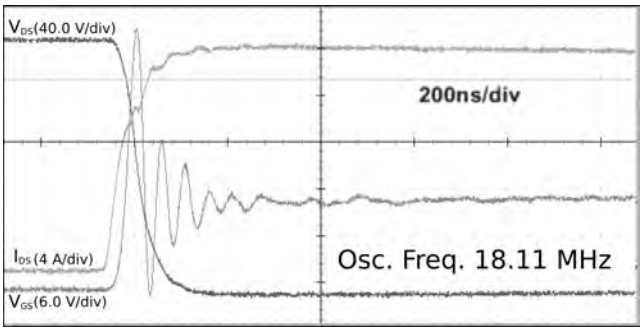


(f) GaN S_{21} and S_{11} parameters.

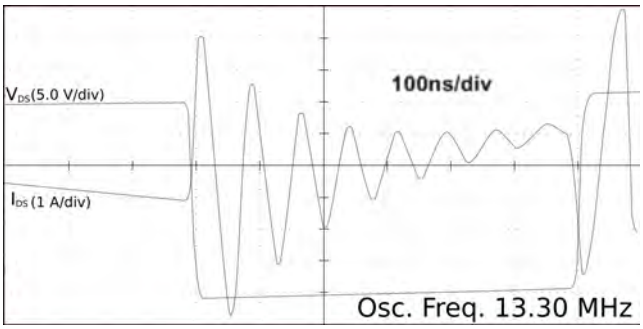
Figure 5. Setup for $f_{oscillation}$ determination and measurement results for S parameters.



(a) Oscillation frequency - PCell.



(b) Oscillation frequency - Cree Evaluation Kit.



(c) Oscillation frequency - GaN.

Figure 6. Results for $f_{oscillation}$.

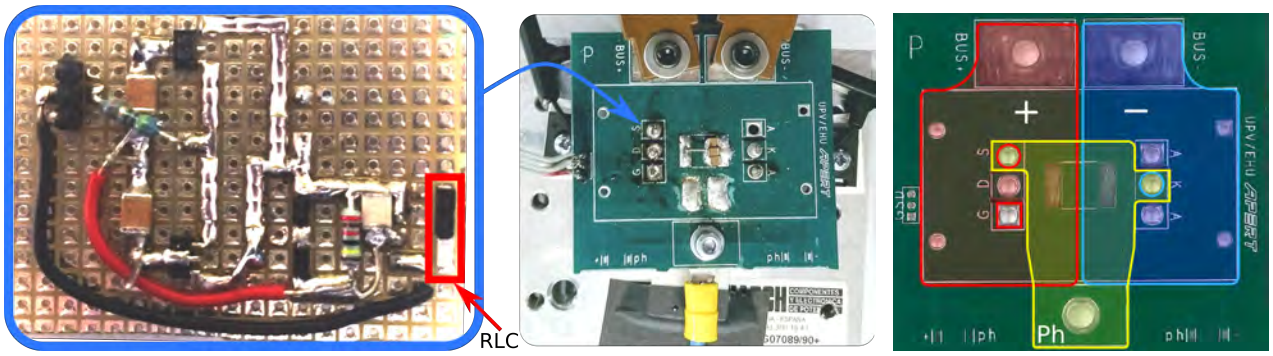
Figure 4 shows the test setup to determine the main resonant oscillation frequency ($f_{oscillation}$) in the design. A network analyser is used to measure power gain between port 2 and port 1 (coefficient S_{21}) and the reflection coefficient at port 1 (coefficient S_{11}) of the circuit. This measurement does not require application of power in the circuit for polarization, and it can be done without connection of the source and the load. The oscillation frequency, $f_{oscillation}$, can be detected as the resonant frequency in the frequency response of parameters S_{21} and S_{11}. V_{DS} is connected to port 2, and V_{GS} to port 1, and a sweep is made at the desired range of frequencies, usually between $30kHz$ and $100MHz$.

The filter inductance and capacitance values are calculated from:

$$f_{oscillation} = 1/(2\pi\sqrt{LC}) \quad (1)$$

And the series quality factor of the resonant filter is:

$$Q_s = (\sqrt{L/C})/R \quad (2)$$



(a) Gate driver, Buck converter and connection location.

(b) PCell main power loop PCB design.

Figure 7. PCell Buck converter.

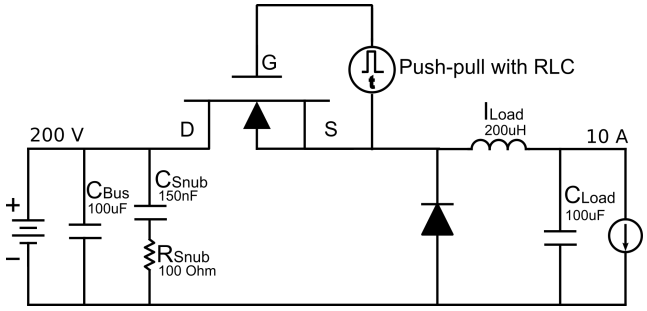


Figure 8. Buck with PCell power circuit.

Selecting a proper value of the filter resistor is important in order to obtain an optimum Q_s value in the filter. If the resistor value is too high, the filter will not divert the feedback current. If the value is too low, part of the gate current that should turn on the MOSFET is diverted. As it will be presented in the following section, experimental results have shown that Q_s values in the range of 1 to 0.5 present the best results.

IV. Experimental Setup and Results

Experimental tests have been done in order to validate the proposal of the main oscillation frequency source and the effect of the gate tuned RLC filter.

A. Determination of main oscillation frequency

In order to confirm the relationship between the resonant frequency of the gate-power loop and the high frequency oscillations, the proposed methodology has been implemented in a Buck converter with three different power circuits with WBG semiconductors. All three circuits have been operated working as a PCell in a Buck converter (figure 8) The first circuit is a proprietary design of a PCell with a SiC MOSFET and a SiC diode (PCell). The second circuit is a Half Bridge SiC demo Board CRD8FF1217P-1 manufactured by Cree (Cree). The third circuit is a Half Bridge GaN demo Board manufactured by EPC (GaN) (table I).

Before operating the Buck converter, determination of $f_{oscillation}$ has been done using a HP 8753E RF Network Analyzer (figure 5). The measured resonant frequencies for the three circuits are shown in table I and figure 5.

Table I
TESTED CIRCUITS CHARACTERISTICS.

	PCell	Cree-cell	GaN-cell
MOSFET	SCT3120AL	C2M0080120D	EPC2021
Diode	C3D25170H	C4D20120D	EPC2021 intrinsic diode
V_{in},V_{out},I_{out}	200V, 100V, 10A	200V, 100V, 10A	24V, 12V, 20A
$f_{oscillation}$	5.95 MHz	18.11 MHz	13.30 MHz

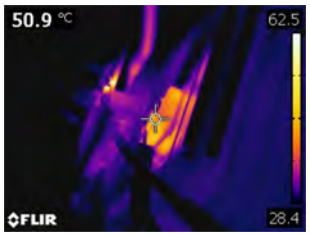
The buck converter has been operated using the three proposed circuits (PCell, Cree Cell and GaN Cell) and the ringing in V_{ds}, I_d and V_{gs} has been measured. Figure 6 shows the voltage and current waveforms in the three circuits, with a full coincidence between the measured resonant frequency in the S_{21} and S_{11} parameters and the ringing oscillations in the power converters, confirming the feedback effect between oscillations in the gate and the power stage.

B. Effect of gate RLC tuned filter

A RLC filter has been designed using the measured $f_{oscillation} = 5.95MHz$ in the network analyser for the PCell proprietary circuit. The values of L and C in the circuit are selected to achieve the desired resonant frequency, and the resistor R value is chosen to achieve various quality factor values for Q (table II).

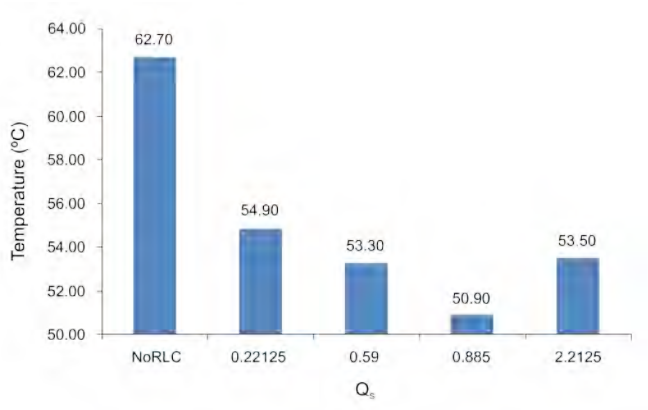
Figure 7(a) shows the PCell Buck converter test setup. The MOSFET and the diode in the PCell are below the PCB on top of a heatsink with forced air cooling. The circuit is divided into two main parts: the PCell power stage in a buck converter and the gate driver using a push-pull configuration. Figure 7(b) shows the Copper areas in the PCB in order to minimize parasitic inductance in the power loop. The gate driver circuit is implemented using a push-pull circuit in order to improve the gate signal integrity by reducing the gate-loop and minimizing external capacitor C_{GDext}. External gate resistors R_{on} and R_{off} are set to 0 Ω; thus, the total gate resistance is only the internal gate resistor, i.e., 18 Ω. Even after implementing recommended PCB good design practice, obtaining a 25 nH parasitic inductance in the gate-loop, including TO-247, measured using a Wayne Kerr 6440B

precision component analyzer, snubber and proper gate driver design, ringing still takes place due to high switching speed of SiC devices and minimum parasitic inductances on both power-loop and gate-loop.



(a) Q_s = 0.885.

(b) No RLC.



(c) Temperature vs. Q_s.

Figure 9. SiC MOSFET temperature for different Q_s values. Thermal camera: Flir T62101.

Table II
SYSTEM POWER LOSSES.

MOSFET switching energy

	Q_s	E_{on} (μJ)	E_{off} (μJ)	E_{total} (μJ)	P (W)
Without RLC	-	259.96	10.36	270.32	16.22
With RLC	R= 8 Ω, Q=2.21	236.98	24.44	261.42	15.69
	R = 3 Ω, Q=0.89	218.05	29.53	247.58	14.85
L=47 nH, C=15 nF	R= 2 Ω, Q=0.59	214.86	34.05	248.91	14.93
	R=0,8 Ω, Q=0.22	257.61	7.77	265.38	15.92

Diode switching energy

	Q_s	E_{on} (μJ)	E_{off} (μJ)	E_{total} (μJ)	P (W)
Without RLC	-	2.46	16.73	19.20	1.15
With RLC	R= 8 Ω, Q=2.21	10.08	7.28	17.36	1.04
	R = 3 Ω, Q=0.89	13.68	21.05	34.73	2.08
L=47 nH, C=15 nF	R= 2 Ω,Q=0.59	9.62	27.76	37.38	2.24
	R=0,8 Ω, Q=0.22	10.83	12.38	23.21	1.39

Total system power losses ($V_{in} = 200\ V$)

	Q_s	I_{in} (A)	V_{out} (V)	I_{out} (A)	Losses (W)
Without RLC	-	5.032	94.40	10.00	62.40
With RLC	R= 8 Ω, Q=2.21	5.025	94.40	10.00	61.00
	R = 3 Ω, Q=0.89	5.013	94.20	10.00	60.60
L=47 nH, C=15 nF	R= 2 Ω,Q=0.59	5.018	94.33	10.00	60.30
	R=0,8 Ω, Q=0.22	5.009	94.00	10.00	61.80

The attenuation of ringing oscillation produces a reduction in overall system power losses. MOSFET switching losses (E_{on} and E_{off}), diode switching losses (E_{rec}) and total system power losses have been measured without the proposed RLC filter and using RLC filters with different Q factor. Results are shown in table II. These results use only average current values and they show only a small reduction in power losses. However, there is a considerable reduction in MOSFET switching power losses (all the power loss difference is switching power loss, conduction power loss are identical with and without tuned RLC filtering) and additional power losses mainly associated in wiring and inductor, because core losses and proximity losses are highly reduced when the current oscillations are reduced. Although switching power losses may be increased in the diode, this power losses are compensated by the improvements in the system and the overall result is the possibility to increase the switching frequency of the converter. In order to show that real power losses are higher than estimated with average currents in the input and output of the converter, thermal imaging analysis has been performed in the switching MOSFET. The results are shown on figure 9. The temperature in the MOSFET is considerably reduced when the tuned RLC filter is used, with a maximum temperature reduction (associated to the switching loss reduction) with a quality factor of $Q_s = 0.89$. In this case, the temperature falls from 62.7ºC to 50.9ºC with the same output power.

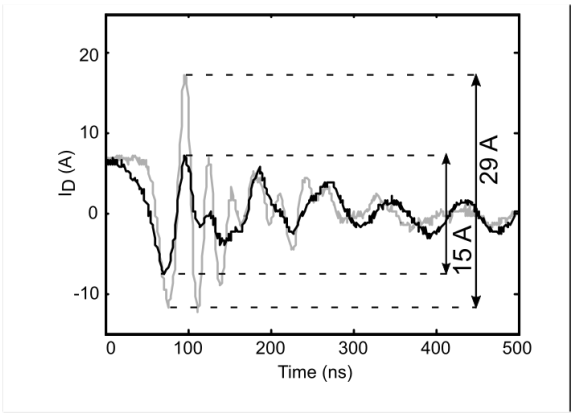
Figure 10 presents the result of introducing a tuned RLC filter in the MOSFET gate in the case of $Q_s = 0.89$. In all cases, a positive waveform oscillation reduction is observed when the tuned RLC filter is introduced (black waveforms) compared to the conventional gate without filter (grey waveforms). Furthermore, additional improvement is achieved by using the RLC filter. Current and voltage overshoots are reduced drastically, by about 90% in voltage overshoot, and a current overshoot reduction of around 35-50%.

C. Near Field Electromagnetic Analysis

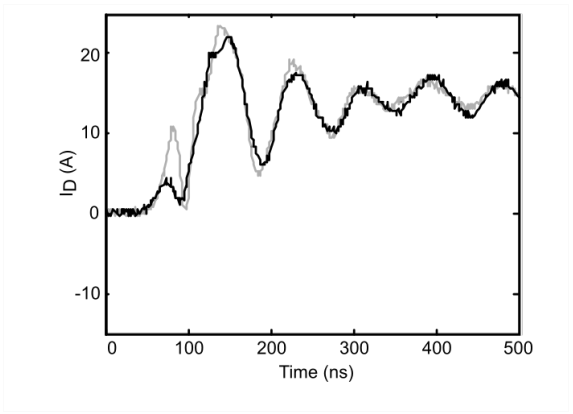
The tuned RLC filter circuit employed to damp the SiC MOSFET gate-oscillation during the switching transitions attenuates considerably radiated EMI in the converter, because it operates as an RF trap. The frequency transfer function is of second order, which implies a slope of 12 dB/oct around the resonant frequency and 6 dB/oct far for the center frequency, as the equivalent RLC impedance becomes pure inductive (higher frequencies) or capacitive (lower frequencies). The series resistance and the equivalent inductance series resistance are the parameters that determine the attenuation bandwidth and the attenuation provided by the circuit.

The study and analysis in the time domain of the RLC circuit performance shown in figure 10 is complemented with measurements of near field electromagnetic emissions of the buck converter. The test set-up employs H near field probes with a frequency range of 9 kHz to 30 MHz. The attenuation path and floor noise of the test set-up is calibrated previously by using the attenuation and floor noise values.

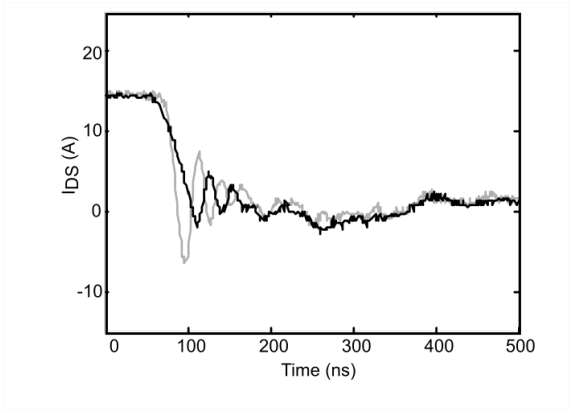
Table III and figure 11 provide H field measurement. Results show that the emissions are mainly within the cell switching frequency range from 9 kHz to 1 MHz, which certifies that the over-damping in the transitions of the switching signal are produced by current loops that generate near H fields, while



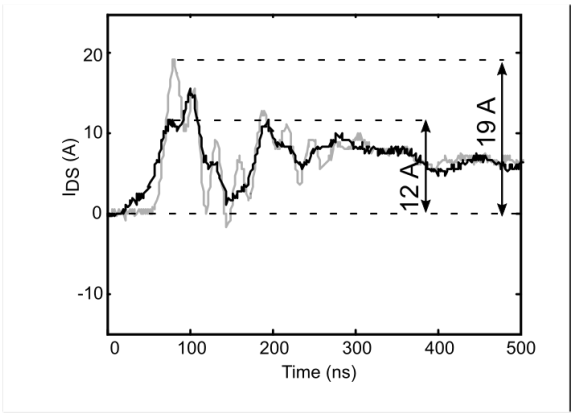
(a) Diode OFF transient current.



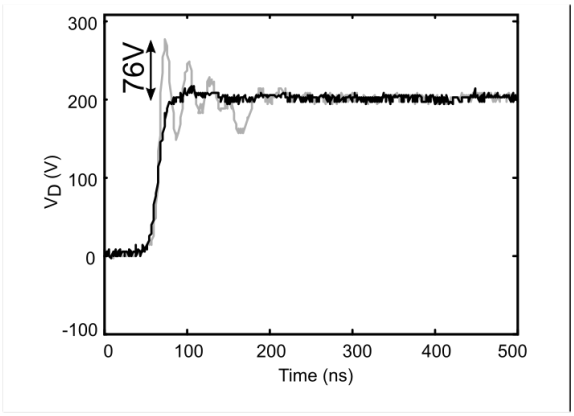
(b) Diode ON transient current.



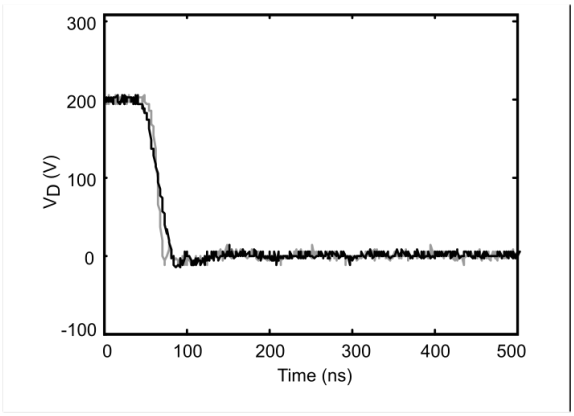
(c) MOSFET OFF transient current.



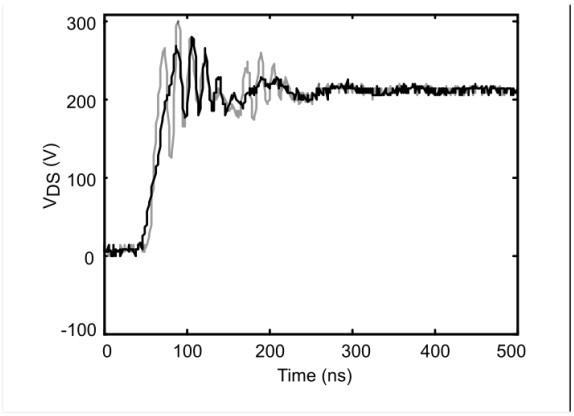
(d) MOSFET ON transient current.



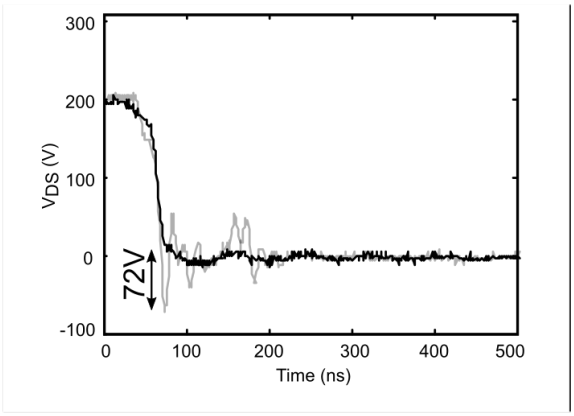
(e) Diode OFF transient voltage.



(f) Diode ON transient voltage.



(g) MOSFET OFF transient voltage.



(h) MOSFET ON transient voltage.

Figure 10. Switching waveforms (grey: without filter; black: with RLC and $Q_s = 0.89$).

Table III
MAGNETIC FIELD SIGNAL COMPARISON 9 KHZ-30 MHZ.

	Q_s	3.20 MHz	8.42 MHz	11.48 MHz	18.00 MHz
Without RLC	-	-27.91 dBm	-35.14 dBm	-30.41 dBm	-40.32 dBm
With RLC	Q=2.21	-28.91 dBm	-38.43 dBm	-32.23 dBm	-47.23 dBm
	Q=0.89	**-30.65 dBm**	**-40.46 dBm**	**-33.28 dBm**	**-49.70 dBm**
L=47 nH, C=15 nF	Q=0.59	-29.24 dBm	-39.82 dBm	-31.17 dBm	-45.61 dBm
	Q= 0.22	-30.56 dBm	-38.83 dBm	-32.25 dBm	-43.59 dBm

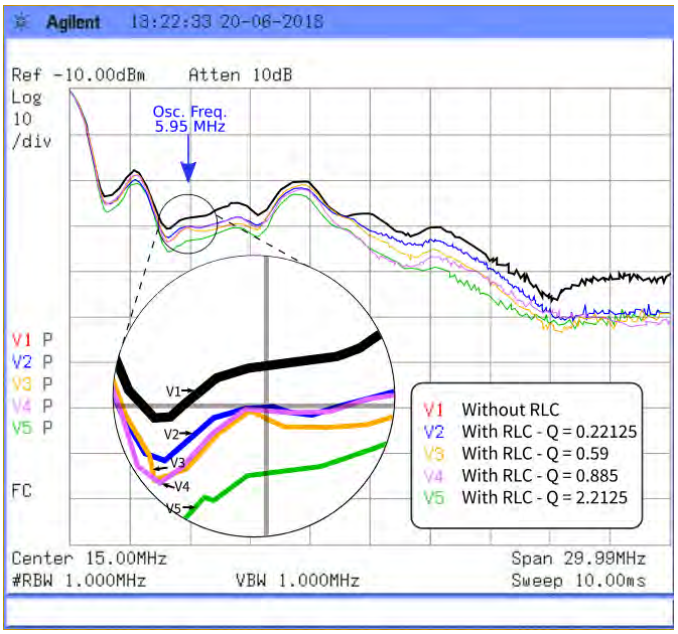


Figure 11. Measurements of EMI spectrum. Analyser: Agilent N9320B; Probe: Rohde & Schwarz 633.0740.00.

the E field in the same frequency range does not produce any noticeable field. H emissions produced by the cell with the tuned RLC filter are, approximately and for the worst case, 3 dB lower that those produced by the circuit without RLC, which implies a reduction of 50% in power losses.

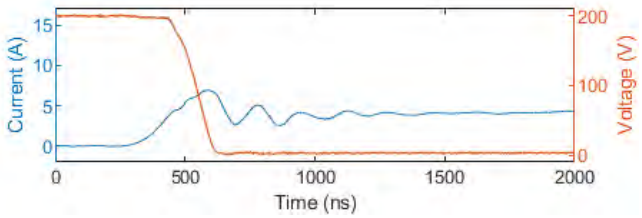
D. Increase gate resistor or use tuned gate RLC filter?

Increasing the gate resistor increases the switching time and reduces the oscillations. In order to compare the effect of increasing gate resistor with introducing the tuned gate RLC filter the Buck PCell converter has been tested with various gate resistor values, with and without the tuned RLC filter. The results are summarized in table IV. Increasing the gate resistor reduces oscillation and reduces overall power loss in the system. The reason for this is that, even if switching time is increased, the current and voltage overshoot are reduced, and the effect of ringing is mitigated, reducing high frequency loss around the converter. However, the introduction of the tuned gate RLC filter always improves the performance. It can be observed that introducing the tuned gate RLC filter with 1.3 ohm resistor is more beneficial than increasing the gate resistor to 20 ohm.

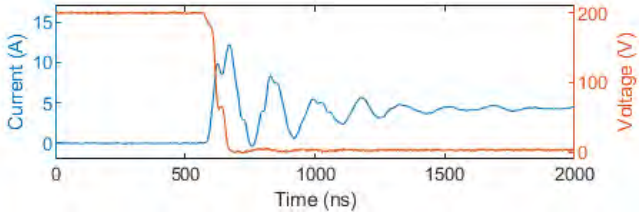
Figure 12 shows the oscillation reduction in the MOSFET current and voltage at turn on with and without RLC tuned filter with gate resistor values 1.3 Ω and 20 Ω.

Table IV
SYSTEM BEHAVIOUR WITH DIFFERENT R_{Gate} VALUES

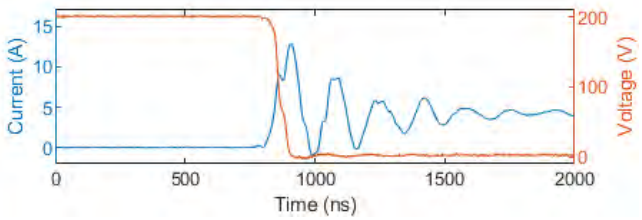
$R_{Gate}(\Omega)$	RLC	Vin (V)	Iin (A)	Vout (V)	Iout (A)	Losses (W)
20	With	200.2	2.62	93.7	5.00	56.02
	Without	200.2	2.72	95.8	5.00	65.54
10	With	200.4	2.66	96.7	5.02	47.88
	Without	200.4	2.80	96.7	5.06	72.07
4.6	With	200.4	2.68	98.0	5.02	45.06
	Without	200.4	2.83	96.4	5.06	79.35
1.3	With	200.4	2.71	98.8	5.05	44.14
	Without	200.4	2.86	96.5	5.06	84.60



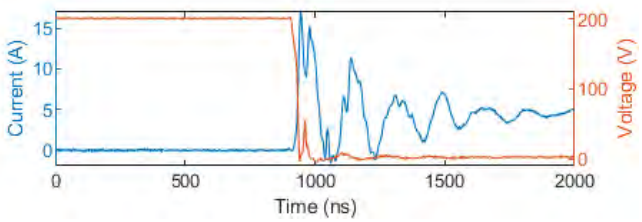
(a) $R_{Gate} = 20\ \Omega$ - With RLC



(b) $R_{Gate} = 20\ \Omega$ - Without RLC



(c) $R_{Gate} = 1.3\ \Omega$ - With RLC



(d) $R_{Gate} = 1.3\ \Omega$ - Without RLC

Figure 12. Results for oscillations at different R_{Gate} values.

E. Tuned gate RLC filter in GaN devices

Similar tests have been done for the GaN setup. Due to the reduced size of the design modifications and measurements could not be done for all the parameters, but the oscillations where clearly reduced when the tuned gate filter was introduced, as shown in Figure 13 with a buck converter switching at 1 MHz. The figure presents the Buck inductor current with (green line) and without (blue line) the tuned gate RLC filter.

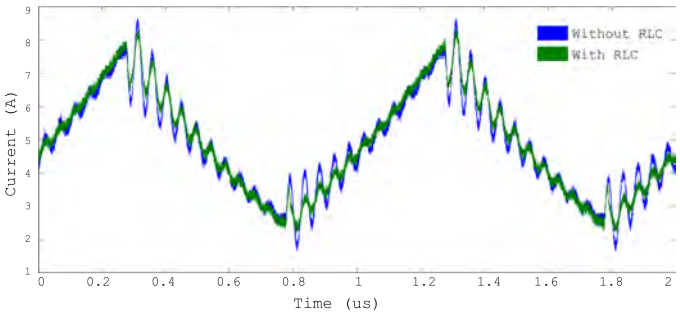


Figure 13. EPC9203 - Current at output inductance

V. Conclusions

The amplification of oscillations through feedback loops (at resonant frequencies) do not allow to use the full potential in power electronics of high switching frequency WBG semiconductors. This paper presents a novel but simple method to determine the main oscillation loop source and attenuate the adverse effect of these oscillations, introducing a gate-oscillation frequency tuned RLC filter at the main oscillation frequency reflected from the power loop to the gate loop.

The effect of gate-oscillation frequency tuned RLC filter has been tested. Experimental results show that the RLC trap is effective against the feedback of the power loop in the appearance of gate voltage oscillation. Mitigating gate oscillations have positive effects on key parameters of the power converter, such as voltage and current overshoot, overall power loss and radiated EMI. Thus, higher switching frequencies can be achieved at a negligible extra cost. Considerable temperature reduction in the switching SiC MOSFET and EMI noise reduction are achieved with the proposed method without the complication and added complexity of Active Gate Drive solutions.

Measurements point out that a quality factor (Q_s) of the RLC trap between 0.5 and 1 provides best results, because with these values there is a compromise between oscillation filtering while still maintaining the necessary drive current in the gate.

The method is a better alternative to increasing gate resistor, because the oscillations are reduced without renouncing to the high switching speeds of WBG devices.

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