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# PRP and HSR for High Availability Networks in Power Utility Automation: a Method for Redundant Frames Discarding

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***Abstract*— Critical systems require zero recovery time when a failure occurs in a communications network. The soon to be implemented standard IEC 62439-3 defines the only two protocols, PRP and HSR, which fulfill this requirement and ensure no frame loss in the presence of an error. These protocols also provide a hot-plugging capability, which allows elements to be added to or removed from the network without interrupting communications and the operation of the plant. The electricity sector has adopted these for power utility automation in the recently published IEC 61850-90-4. The challenge is to obtain an efficient approach for use in electronic devices, capable of managing the characteristic duplicates and circulating frames of these protocols, coupled with agile architectures capable of dealing with real-time processing requirements, fast switching times, high throughput, and deterministic behavior. The main contribution of this paper is the in-depth analysis it makes of network parameters imposed by the application of the protocols to power utility automation and the proposition of a frame management system based on a segmented memory system that improves frame detecting time and uses the smallest memory required in order to resolve all the issues dealt with.**

***Index Terms*—Automation, high-availability, Ethernet, HSR, IEC 62439-3, PRP, redundancy, switching, substation, IEC 61850.**

## I. Introduction

Smart grids are attracting the attention of the electricity sector, and one part of the Electric Distribution Smart Grid Network is the automation network in substations, governed by the IEC 61850 standard. It helps to secure the interconnection and interoperability of devices made by several different manufacturers. Moreover, using and integrating LAN networks in industrial systems and using Ethernet and TCP/IP technologies allows offices to be interconnected with automation networks, which provides business resource planning systems with industrial process data for operational and decision-making purposes. Ethernet offers high throughput and has a dominant position in the Local Area Network (LAN) technologies. However, using Ethernet for industrial automation networks involves adding new, strict requirements and dealing with new challenges [1], [2].

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The IEC 61850 standard series for communications networks and systems for power utility automation establishes requirements in terms of real-time operation communications protocols and availability. Regarding the network infrastructure, the recently published IEC 61850-90-4 [3] has adopted Parallel Redundancy Protocol (PRP) and High-availability Seamless Redundancy (HSR), both defined in the IEC 62439-3 [4], as the preferred Ethernet-based protocols for Station Bus (SB) and Process Bus (PB) in substations. They provide zero recovery time and frame loss protection in the case of a grid failure.

Thanks to the broad acceptance of these protocols in the electricity sector, other industrial sectors are currently testing these new protocols for unified layer 2 high availability field buses and other applications in which their features may be useful [5], [6], such as Time Sensitive Networks (TSN) for industrial and automotive control systems with seamless redundancy and reduced worst case delays, or another means of transport such as trains [7].

Both of the protocols, PRP and HSR, that have been introduced, are based on sending two copies of every frame via two independent paths, so that, if one of them is lost, the other one arrives and there is no break in communication. The redundancy that has been introduced is in the Link layer of the OSI reference model. These protocols add a Link Redundancy Entity (LRE), which manages protocols, functions and frames transparently for the other layers, with which the interface is standard Ethernet. This feature allows the use of existing upper stack protocols and applications, which is required for the use of Ethernet for industrial automation networks in general [8].

PRP provides high availability through two networks. The PRP nodes, called DANs (Double Attached Nodes) are connected to two isolated networks, which operate in parallel as depicted in Figure 1. Frames are duplicated in the source DAN and are sent over both networks; the destination node receives the first copy and accepts it, if it is correct, and then the second copy received is discarded as duplicate.

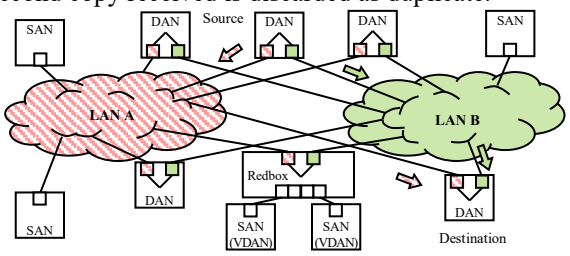



Fig. 1. PRP Network.

PRP networks accept Single Attached nodes (SANs). They may be connected directly to one of the LANs or as a Virtual DAN (VDAN) to the two networks through the use of a Redundancy Box.

HSR operation is similar to PRP but HSR uses a single LAN. The basic topology, a ring, uses two independent paths (clockwise and counterclockwise) as depicted in Figure 2. DANs forward frames from one port to the other, unless they are the sole destination of the frame, or unless they have already sent the same frame in the same direction. HSR networks do not accept SANs connected directly because they cannot forward frames, therefore Redboxes become absolutely necessary.

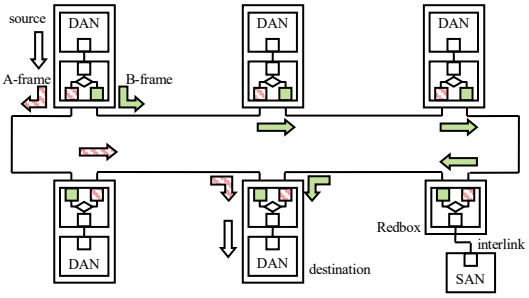



Fig. 2. HSR Network.

The increase in availability involves a number of costs. PRP requires two LANs and nodes cause some delay due to encoding, decoding and discarding. HSR has also a number of drawbacks, i.e., the delay caused by each node in the ring, and the halving of the effective bandwidth [9], [10]. The computation requirements for the HSR nodes are higher because of processing HSR frames, removing duplicates and circulating frames (described below) and switching all the traffic.

Apart from the original PRP and HSR operation, defined in the standard, a number of possible improvements to these protocols have been published in different papers: Quick Removing QR and Virtual Rings [11], Removing the Unnecessary Redundant Traffic RURT [12], Link Reduction [5], Port Locking [13], Dual Virtual Paths DVP [14], a Novel packet transmission scheme [15]. Some of them look interesting and may be included in future versions. Nevertheless they do not affect the proposed discarding method.

The present work started with the introduction of the PRP and HSR and applications. Section II analyzes the redundant frames introduced by these protocols, which must be discarded (duplicates and circulating frames), and section III analyzes the requirements for frame detection. Section IV proposes a memory system and the considerations taken into account, and sections V and VI present the prototype that has been developed and simulations for validation. The paper finishes with conclusions and future work.

## II. Duplicates and Circulating Frames

Although they have been introduced before, it is a good idea to define these frames:

- A duplicate is one that arrives after a copy of the original frame arrives correctly from another port.
- A circulating frame is one that arrives after a copy of the original frame arrives correctly from the same port. In a ring, they appear when a multicast frame has lost its source, or when a unicast frame has lost its source and destination [16].

Due to the similar operation and likelihood of interconnecting PRP and HSR, it is convenient to use the same frame discarding method. The IEC 62439-3 [4] leaves the designer free to choose a method to manage them and establishes its requirements:

- Never reject a legitimate frame, while occasional acceptance of a duplicate can be tolerated.
- Be capable of eliminating more than one duplicate.

### A. PRP Trailer, HSR Tag and Frame Identification

In order to control the frames that have arrived and recognize duplicates and circulating frames both protocols add extra information to the Ethernet frames. PRP adds a Redundancy Control Trailer (RCT) and HSR adds a HSR Tag, as depicted in Figure 3 and Figure 4.

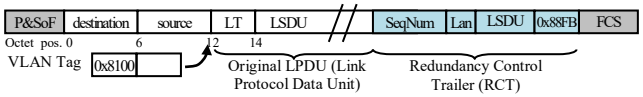



Fig. 3. PRP frame.

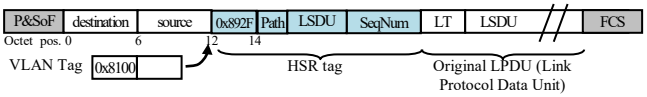



Fig. 4. HSR frame.

PRP RCT and HSR Tag help to recognize PRP and HSR frames and identify frames in order to determine whether they arrive again as duplicates or circulating frames. Their fields are:

- PRP-1 Suffix (0x88FB) / HSR Ethertype (0x892F): They help to identify PRP and HSR frames.
- Lan/Path Id: This indicates, in general, the sending port. In PRP it indicates the LAN (A or B), and in HSR ring it indicates the direction (clockwise or counterclockwise).
- Link Service Data Unit (LSDU) size: It is the size in octets of LSDU + RCT/Tag.
- Sequence Number (SN): This is used to control duplicates and circulating frames. Each time a node sends a frame, SN is incremented by one.

Therefore, the pair formed by the Origin MAC address (MACo) + SN identifies frames and is used to detect and discard duplicates and circulating frames. Hence, the information on each received frame must be stored in a memory to be checked every time a frame arrives in order to detect whether it has arrived before.

### B. Sequence Number Reutilization

It is worth mentioning the need for SN reutilization. The SN field is composed of 2 octets, so that after $2^{2 \cdot 8} = 65536$ frames, SN is properly repeated. SN can be repeated after $t_{wrap\_Min\_teor}$ (1), in the worst case, in which the shortest possible frames arrive continuously one after another (8 octets P&SoF + 70 octets HSR/PRP shortest frame + 12 octets gap).

$$t_{wrap\_Min\_teor} = 2^{16} \cdot (8 + 70 + 12) \cdot 8 \,/\, data\_rate = \begin{cases} 471.8\ ms\ (FEth) \\ 47.2\ ms\ (GEth) \end{cases} \quad (1)$$

Therefore, frames should not be remembered more than this time. This time is different for Fast Ethernet (FEth) with 100 Mb/s and Gigabit Ethernet (GEth) with 1000 Mb/s. The IEC 62439-3 establishes as $t_{wrap\_Min}$: 400 ms (FEth). This also allows node reboot at any SN position.

### C. Duplicates and Circulating Frames Detection: Cases

In order to identify duplicated, circulating or new frames, it is necessary to analyze the different possible cases. A number of timeslots will be defined:

- $t_{residence\_Max}$ and $t_{residence\_Min}$: The maximum and minimum time that frames are remembered for frames discarding.
- $t_{skew}$: Time between a frame and a duplicate.

Figure 5 shows a number of cases presented in the IEC 62439-3 for duplicate discard analysis in which presented frames have the same MACo + SN. This diagram is also used for circulating frames. In this case, all the frames arrive over the same port.

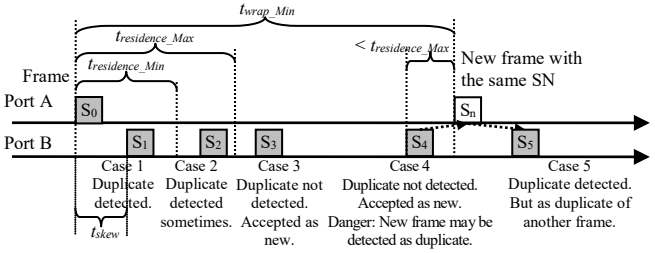



Fig. 5. Duplicate discard cases: collected in the IEC 62439-3.

Cases 1, 2 and 3 are the expected cases in the normal operation of PRP and HSR while cases 4 and 5 must be avoided:

- Case 1 ($t_{skew} < t_{residence\_Min}$): The frame is considered a duplicate.
- Case 2 ($t_{residence\_Min} < t_{skew} < t_{residence\_Max}$): The frame is sometimes considered a duplicate while on other occasions it is not.
- Case 3 ($t_{skew} > t_{residence\_Max}$): The frame is considered a new frame.
- Case 4 ($t_{skew} < t_{residence\_Max}$ *between* $S_4$ *and* $S_n$): A non detected duplicate can cause a new frame to be considered a duplicate. This must be avoided because it rejects legitimate frames.
- Case 5 ($t_{wrap\_Min} < t_{skew}$): This frame, $S_5$, is considered a duplicate of $S_n$, when it is a duplicate of $S_0$. In this case a duplicate is eliminated by chance. This is not acceptable.

Figure 6 defines another two cases, 6 and 7, not defined in the standard and which must be avoided too.

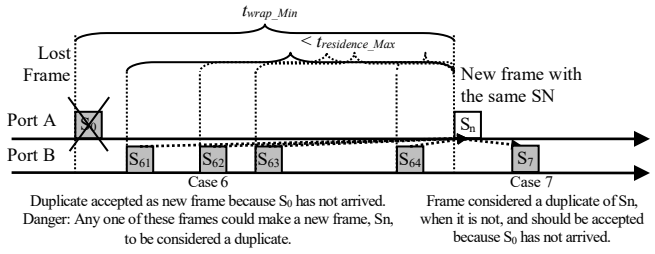



Fig. 6. Duplicates discard cases: not considered in the IEC 62439-3.

These happen when a frame, $S_0$, does not arrive or is incorrect.

- Case 6 ($t_{skew} < t_{residence\_Max}$ *between* $S_{6X}$ *and* $S_n$): A duplicate $S_{61}$, $S_{62}$, $S_{63}$ or $S_{64}$ is accepted as new (strength of PRP and HSR). But a new frame, $S_n$, can be considered a duplicate if the timeslot between them is less than $t_{residence\_Min}$ or $t_{residence\_Max}$.
- Case 7 ($t_{wrap\_Min} < t_{skew}$)*:* A duplicate $S_7$, arrives later than the new frame, $S_n$. Thus, $S_7$ should be accepted but it can be discarded as a duplicate of $S_n$.

A way to avoid undesirable cases would be to consider:

- *"*$t_{skew} \leq t_{round} < t_{wrap\_Min} / 2$*"*: Hence, $S_4$, $S_5$, $S_{64}$ and $S_7$ would never appear. This condition is extended to HSR by the inclusion of time between a frame and a circulating frame (the time it takes a frame to turn round completely, $t_{round}$). The network must be designed carefully in order to avoid large time differences.
- *"*$t_{residence\_Max} < t_{wrap\_Min} / 2$*"*: Thus, $S_{6X}$ will not cause the elimination of $S_n$ when $S_0$ does not arrive.

## III. IEC 61850: Requirements for HSR and PRP

The application to power utility automation networks imposes a number of tight requirements on PRP and HSR. An IEC 61850 frame loses its usefulness if it is not received in a timely manner, and being late could be worse [3]. Thus, latency, throughput and reliability will be analyzed in order to obtain the conditions to be fulfilled by the discarding method.

### A. Latency

Latency, the worst delay of all possible associations, becomes a factor to control specially in HSR in which every node adds a delay to the frames that crosses it. IEC 61850-5 [17] establishes different types of traffic based on latency, with the most restrictive latency of 3 ms for TT6 traffic type in substations. It includes Generic Object Oriented Substation Events (GOOSE) traffic and Sample Value (SV) traffic. According to the IEC 61850-90-4 [3], each node concerned, source and destination, has a maximum processing time of 1.2 ms. Thus, the remaining time to cross the network will be given by (2).

$$Latency_{Max} = 3 - 2 \cdot 1.2 = 0.6\ ms \quad (2)$$

The delay added by each HSR node, $T_1$, can be broken down into three parts (3) as depicted in Figure 7.

$$T_1 = t_1\ (receiving) + t_2\ (switching) + t_3\ (waiting) \quad (3)$$

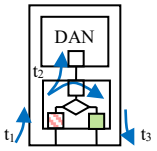



Fig. 7. Delays in a HSR node. Source node includes $t_3$, and destination $t_1 + t_2$.

These terms refer to parts of the reception/forwarding operation process of the frames in nodes. The following time calculations are for FEth and must be divided by 10 for GEth.

- $t_1$ depends on the operation mode used.
  - Store-and-Forward (SF): The whole frame is received before switching. This depends on the size of the frame: from 70 octets up to 1528 octets plus P&SoF. It results in a time range from 6.24 µs to 122.88 µs.
  - Cut-Through (CT): Switching starts after receiving P&SoF, addresses and HSR Tag to minimize the delay added in the nodes. The theoretical value is 2.08 µs for the regular HSR frame and 2.4 µs if it has the VLAN tag.
- $t_2$ is the time taken to decide whether to forward/receive/ discard a frame and it depends fundamentally on the time needed to check whether the frame has arrived before or not.
- $t_3$ is the time a frame has to wait to be sent because another frame is being sent. It is in the range of 0 (no frame is being

sent) to $t_{3Max}$ = 123.84 µs for FEth (the longest frame is being sent: 1528 octets + 8 octets P&SoF + 12 octets gap).

Latency can be reduced by acting on these terms:

- $t_1$ is made minimum by using CT which entails hardware implementation, e.g. Field Programmable Gate Arrays (FPGAs).
- $t_3$ is eliminated/reduced by avoiding/reducing waiting times in nodes. It may be improved by synchronized traffic generation on nodes and/or by controlling frame size. If delivered frames were limited in length, the waiting times would be shorter. On the other hand, if traffic generation is controlled and synchronized in the network, waiting times in the nodes can be avoided or reduced. The IEC 62439-3 includes the use of IEEE 1588 [18] to ensure accurate synchronization.
- $t_2$ is the last term with which the delays in nodes can be reduced. It is directly related to the way of checking whether a frame is new or a duplicate or circulating frame.

The main challenge is that a memory has to be rounded every time a frame arrives to check whether it is already in the memory. Every HSR node in the ring has to carry out the search, which adds a forwarding delay to the frame. This fact limits the quantity of nodes allowed in a HSR ring. The theoretical worst scenario occurs when two nodes are next to each other as shown in Figure 10a. Frames must cross every other node in the ring if the direct link which links 1 and *N* has failed.

The maximum number of nodes, *N*, of a HSR ring is given by (4) in this theoretical worst scenario, when the largest Ethernet frame is transmitted with the latency restrictions imposed by TT6 traffic: 0.6 ms (2).

$$\begin{aligned} N - 1 &= Latency_{Max} / (T_1 + t_L) \\ N &= 1 + Latency_{Max} / (t_1 + t_2 + t_3 + t_L) \end{aligned} \quad (4)$$

Where $t_L$ is the delay in each link.

PRP only checks duplicates at destination, so this time the requirement is not so decisive. However, a fast method common to PRP and HSR simplifies implementations and node development.

### B. Throughput

The throughput is defined as the amount of data that can be transported by unit of time. In the context of Power Utility Automation, each node, in the PB, can generate about 5 or 6 Mb/s of SV traffic plus Manufacturing Message Specification (MMS) and GOOSE messages. The traffic transmission structure should be as shown in Figure 8 [3].

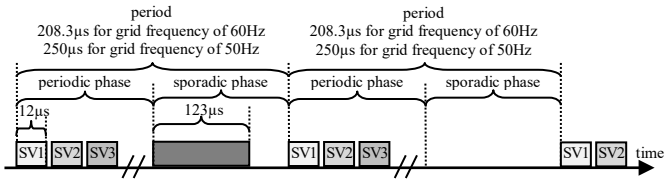



Fig. 8. Example of Process Bus traffic.

Thus, the expected traffic implies a maximum of 6 nodes in the worse case for FEth and 20 nodes if PB is only dedicated to SV traffic [3]. For GEth, the traffic capability is multiplied by 10. Thus, the number of supported nodes is multiplied by the same factor, i.e., up to 200 nodes with only SV traffic.

### C. Reliability

Reliability is related to the probability of a frame being lost because of congestion, not because of physical failure. Hence, physical failures can be dealt with through redundancy, while overload can affect both redundant paths.

The way to avoid a DAN or Redbox becoming a bottleneck is to assure that the response to a request concerning an arrived frame is given before a new frame arrives with a new request. Consequently, if we consider the minimum frame in HSR, 70 octets + P&SoF + gap, its duration will be $t_{Min}$ (5); the time between two requests made by a port in the worst case.

$$t_{Min\_FEth} = (8 + 70 + 12) \cdot 8 / 10^8 = 7.2\ \mu s \Rightarrow t_{Min\_GEth} = 0.72\ \mu s \quad (5)$$

Therefore, for the most generic solution, the memory system should be able to response in $t_{Min}$ to as many requests as the device has ports: Two for a DAN and three for a Redbox.

### D. Summary of Requirements

Table 1 summarizes the requirements that a generic discarding method of duplicates and circulating frames should comply with in order to be applicable in PRP and HSR nodes, for the standard typical communications described in the IEC 61850.

Table 1. Summary of requirements and design limits.

| | FEth | GEth |
|---|---|---|
| **Design HSR/PRP** | $t_{skew} \le t_{round} < t_{wrap\_Min} / 2$<br>$t_{residence\_Max} < t_{wrap\_Min} / 2$ | |
| | *With* $t_{wrap\_Min}$ = 400 ms:<br>$t_{skew} \le t_{round} < 200$ ms<br>$t_{residence\_Max} < 200$ ms | *With* $t_{wrap\_Min}$ = 40 ms:<br>$t_{skew} \le t_{round} < 20$ ms<br>$t_{residence\_Max} < 20$ ms |
| **Latency** | *Latency* ≤ 600 µs<br>*N - 1 = Latency / (*$t_1$+$t_2$+$t_3$+$t_L$*)* | |
| | *With* $t_2 = t_L = 0$:<br>*CT:* $N(t_{3Max})$=5; $N(t_3$=0) = 251<br>*SF:* $N(t_{3Max})$=3; $N(t_3$=0) =3 | *With* $t_2 = t_L = 0$:<br>*CT:* $N(t_{3Max})$=48; $N(t_3$=0) = 2051<br>*SF:* $N(t_{3Max})$=25; $N(t_3$=0) = 48 |
| **Throughput** | *6 nodes*<br>*20 nodes with only SV traffic* | *153-60 nodes*<br>*200 nodes with only SV traffic* |
| **Reliability** | $t_2 \le t_{Min\_FEth}$ = 7.2 µs | $t_2 \le t_{Min\_GEth}$ = 0.72 µs |

## IV. Proposed Discarding Method

In order to fulfill the requirements presented in the previous sections for the use of PRP and HSR in power utility automation networks, a proper selection of the memory configuration scheme and the hardware architecture is critical.

In his master thesis, J. Xiaozhuo [16] compares circular buffers, hash tables and a combination of both. According to this, circular buffers are the simplest method and are better at detecting redundant frames but this method is too slow; hash tables are the most complex solution, they are faster but they need to control collisions, an appropriate hash function has to be chosen and the entries' age must be controlled. The combination of both had an intermediate behavior by using three tables per port and for the only particular case of SV traffic.

The present work proposes another solution, a new frame discarding method based on a segmented memory, in order to to remember arrived frames and detect when they arrive again as duplicates or circulating frames. Moreover, it takes into account the parameters analyzed for power utility automation.

### A. Segmented Memory with Simultaneous Searches

Figure 9 shows the memory structure and operation flow. The contribution presented in this paper proposes a discarding method that uses a segmented memory. Writing is done one entry after another (0 to *n*-1) sequentially as in a Circular Buffer. So as to improve the reading rate, the memory is divided in segments, *s*. These segments are read in parallel and are compared with arrived frames.

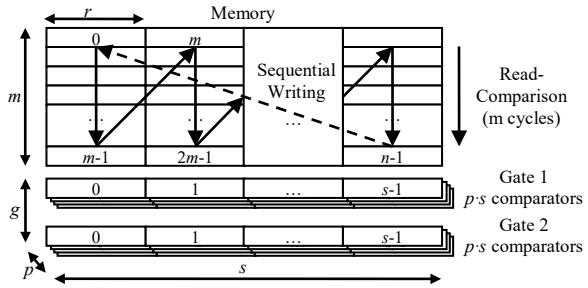



Fig. 9. Segmented memory with simultaneous searches.

If the number of positions, *n*, is maintained constant and the number of segments, *s*, is increased, there is a reduction in the delay. But, the complexity and amount of resources used in the design are increased. This solution can be modeled as a set of sequential memories in parallel, or a set of Content Addressable Memories (CAMs) read sequentially. If each parameter is brought to the limit, the boundaries obtained are:

- CAM memory: *n* segments of 1 position. The CAM memories needed would have a size not suitable for medium FPGAs [19].
- Circular Buffer (a linear FIFO): 1 segment of *n* positions. In a common circular buffer a simple search involves reading every position one after another. The delay introduced by this task is not allowable for this application [16].

Thus, these boundaries do not offer an optimum solution. It is necessary to find out the number of segments as a tradeoff between an acceptable delay and the implementation complexity.

It is worth mentioning two additional mechanisms introduced in the proposal. These are represented in Figure 12.

- Dual port memories (in order to avoid confusion with "node ports", "memory ports" will be referred to as gates): by using dual port memories, searching time is divided by the number of gates, $g = 2$.
- Simultaneous searching: each entry searched will be compared at the same time with read entries. Hence, *p* searches can be done simultaneously, one per each port.

### B. General Considerations

#### 1) Number of Memory Positions Required

This section defines a procedure to calculate the required memory size for the frame discarding method.

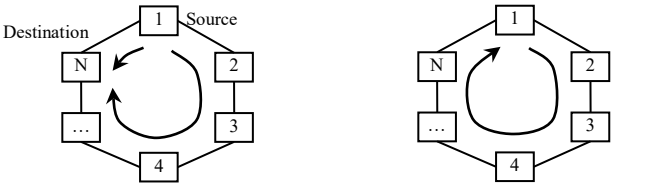
*a) Maximum*

No more than $2^{16} = 65536$ frames must be remembered because after this number of frames, MACo + SN can be correctly repeated as seen in section *II.B*. This number is halved if the first condition of Table 1 is taken into account. But, the aim is to use the lowest amount of resources, so that what really determines the limit for implementation will be the minimum number of positions needed.

*b) Minimum I: The Worst Case Considered*

The worst scenario occurs when a frame of the biggest size turns right round the ring, $t_{round}$, as seen in Figure 10b, and this frame has to wait the maximum time in every node because each node is also sending a frame of the biggest size, $t_{3Max}$. Meanwhile, frames of minimum size are continuously arriving through the other ports, $t_{Min}$. Thus, the number of memory positions needed, *n*, will be given by (6).

$$n = N \cdot (t_1 + t_2 + t_3 + t_L) / t_{Min} \quad (6)$$




a) Maximum latency in the worst case. b) Longest path for a whole lap to the ring.

Fig. 10. The worst cases of time delays in a HSR ring.

*c) Minimum II: Synchronization and Same Length Frames: Number of Positions = Number of Nodes*

This section analyzes a common scenario in substations already seen in section *III.B*, which could optimize previous quantities of number of positions. The maximum number of nodes considered, 200 nodes, occurs for a case with only SV traffic and node transmissions synchronized, as expected according to [3]. In this situation, the number of positions can be reduced to the number of nodes, as shown in (7), because every node sends synchronized frames of the same size [16]. In other words, before a node receives through one port the frame sent through the other one, the node also receives one frame of every each other node in the ring.

$$n = N \quad (7)$$

#### 2) Entries' size and number of memories

The frames that are processed in the hardware are identified with MACo + SN. This information needs to be remembered. In order to know through which port frames arrived, a memory per each port should be needed. However, two more considerations will be added so as to optimize the system:

- If it is taken into account that the same frames (MACo + SN) are going to be received through the different ports; these entries could occupy a common position in a memory if an extra octet is added to store the input port.
- Erroneous frames can also be stored in the extra octet. i.e. when the CRC of the frame is erroneous or the frame is cut.

Therefoe, it is possible to limit the memory requirements to a single memory regardless of the number of ports. Each entry in the memory will be of $r = 9$ octets as depicted in Figure 11.

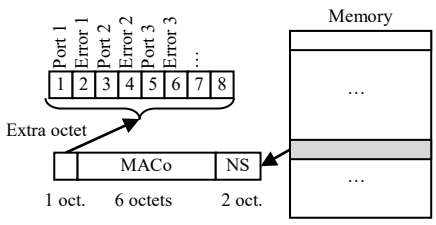



Fig. 11. Size of entries of the memory.

*3) Aging of Entries: Rewriting*

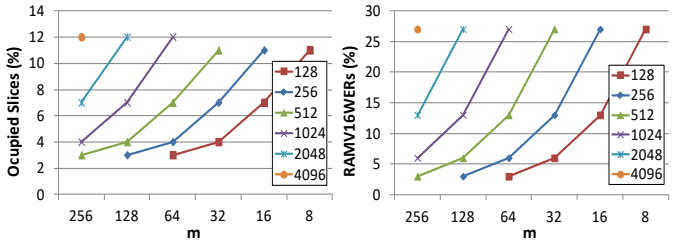
According to the IEC 62439-3, entries should not be remembered more than $t_{wrap\_Min}$. Moreover, as seen in section *II.C*, this time has been limited to less than $t_{wrap\_Min}$ / 2. Using sequential rewriting of entries is an added advantage for controlling the age of entries. Once the number of memory positions has been defined, if a minimum writing rate is assured, old entries will be rewritten by new ones. If a new entry does not arrive in less than $t_{overload}$, defined by (8), the oldest entry is deleted.

$$t_{overload} = t_{residence\_Max} / n < (t_{wrap\_Min} / 2) / n \quad (8)$$

## V. Prototype and Implementation

A system with a memory configuration as described before with a Finite State Machine (FSM) has been implemented using the Xilinx ISE 13.2 [20] to comply with the desired requirements in a reconfigurable device. The board chosen is the SP605 Evaluation Kit [21] with a Spartan 6 XC6SLX45T FPGA running a system clock of $f_{sys}$ = 100 MHz. Three simultaneous searches were considered in order to respond to the most general implementation of Redboxes, with three ports. Memories from 128 to 4096 positions (power of two) were implemented with the proposed memory system and the sizes of segments considered were from 256 down to 8 positions (power of two).

Figure 12 shows the percentage of occupied slices and BlockRAMs used in the implementations for the sizes considered. The amount of resources used increases with the reduction in the size of the segments, *m*, i.e., the increase in the number of segments, *s*.




a) Occupied Slices (%). b) BlockRAMs (%).

Fig. 12. Resources used in the FPGA.

### A. Size of Segments

Segments of 64 positions ensure that the discarding method supports the maximum frame rate through three ports at the same time for the most demanding case of GEth, as shown in section *III.C* associated with reliability. If the fact that both gates, $g$ = 2, of the memory are used is taken into account, the time needed to read all the positions of the memory is given by (9).

$$t_{Memory} = m / g / f_{sys} = 64 / 2 / 10^8 = 0.32\ \mu s \quad (9)$$

Each simultaneous search adds a number of extra cycles, $c_{Extra}$ which include:

- $c_{comp}$: 1 cycle required by the FSM after a search.
- $c_{search}$: entry searching time. 3 or 4 cycles depending on the presence of the entry in the memory or not, respectively.
- $c_{update}$: entry updating time: a frame might have an error the registration of which in the memory adds other 6 cycles.

Those extra cycles per port must be added in the worst case, i.e, a search that is interrupted by the answers to other simultaneous searches and updates. The result is a maximum $t_2$ given by (10), behind the limit established by reliability in (5).

$$t_{2\_Max} = m / g + p \cdot (c_{comp} + c_{search\_notfind} + c_{update}) / f_{sys} = \\ = t_{Memory} + t_{Extra} = 0.32 + 0.33 = 0.65\ \mu s < 0.72\ \mu s \quad (10)$$

On the other hand, in the best case, in which data is found in the first comparison, $t_2$ is reduced to $t_{2\_Min}$=*0.06µs*.

In the worst case, the delay added by each node will have a maximum value defined by (11), i.e., less than 5 µs as the IEC 61850-90-4 establishes for HSR nodes [3]. The other terms that affect the latency, $t_3$ and $t_L$, do not depend on the discarding method used and are minimized/eliminated by the network design and operating procedure.

$$t_{1\_Max} + t_{2\_Max} = 2.4 + 0.65 = 3.5\ \mu s\ (FEth) \\ t_{1\_Max} + t_{2\_Max} = 0.24 + 0.65 = 0.89\ \mu s\ (GEth) \quad (11)$$

### B. Discussion and Number of Entries

This section establishes the number of nodes supported, *N*, by the proposed memory system versus the memory positions required, *n*. This is summarized in Figure 13. Curves *La.FEth* and *La.GEth* are given by Latency (4); curves *ro.FEth* and *ro.GEth* are given by equation (6) and curve $n = N$ is given by equation (7), $t_L$ is neglected.

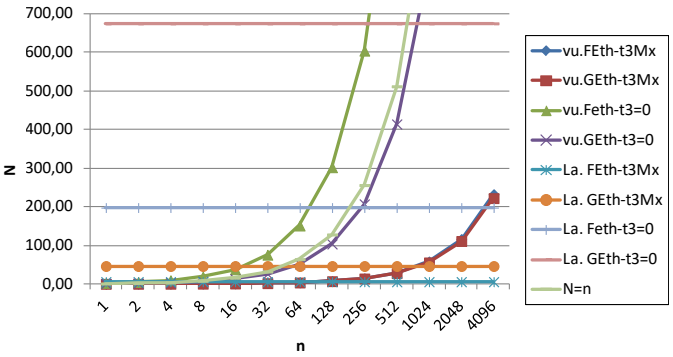



Fig. 13. The number of nodes supported versus the number of memory positions.

Two different scenarios are analyzed below according to the results obtained in Figure 13:

- Scenario I: The worst expected case in which frame generation is not synchronized, with $t_{3Max}$:
  - FEth: Memories of 128 positions (2x64) are enough for substation networks of up to 5 nodes –limited by latency, equation (4)–. Bigger memory structures do not increase the number of nodes because this is limited by the delay accumulated in the nodes.
  - GEth: Memories of 128 positions are enough up to 6 nodes –limited by equation (6)–. Using 256 positions or 512 positions improves results to 13 and 27 nodes respectively –limited by (6)–. But the best result is obtained with memories of 1024 positions (16x64), which support up to 46 nodes –limited by latency,

equation (4)– close to the theoretical 48 nodes given for $t_2 = 0$ in Table 1.
  - For the case given by the equation (7), the maximum 200 nodes desired for GEth and only SV traffic given by throughput would be supported with 256 positions.
- Scenario II: The case of synchronized frame generation with $t_3 = 0$:
  - FEth: 128 positions (2x64) support the maximum of 20 nodes established by throughput and fulfills equations (4), (6) and (7).
  - GEth: 256 positions (4x64) support the maximum of 200 nodes established by throughput and fulfills equations (4) and (6).
  - According to the case given by the equation (7), 128 positions would support no more than 128 nodes. In order to support at least 200 nodes according to (7), 256 positions (4x64) would be needed.

Therefore, the best configuration obtained would be 1024 positions (16x64) according to latency, throughput and reliability, and this covers the maximum number of nodes for every considered scenario. This optimum configuration is valid for FEth and for GEth as well. But, should there be fewer resources available; 512, 256 or 128 positions may be acceptable with loss of performance (fewer nodes). Table 2 shows the resources used for memory configurations with 64-position segments.

Table 2. Resources used depending on memory size for m = 64 positions.

| ***n* (positions)** | **128** | **256** | **512** | **1024** |
|---|---|---|---|---|
| ***s* x *m* (segments x size)** | **2x64** | **4x64** | **8x64** | **16x64** |
| **Slice Reg. (%)** | 1 | 1 | 1 | 1 |
| **LUTs – Look up Tables (%)** | 2 | 3 | 5 | 9 |
| **Occupied Slices (%)** | 3 | 4 | 7 | 12 |
| **RAMB16BWERs (%)** | 3 | 6 | 13 | 27 |

## VI. VALIDATION

In order to validate the proposed memory management method, a set of simulations have been performed. The results show the proper operation and the compliance of the required times for searches and updates. Some of these will be presented in order to show the correct operation and compliance with the time requirements.

### A. Considerations for simulations

Memory and segment size considered for simulations have been reduced in order to show the correct operation, the extra cycles are fixed and common for these simulations and the actual complete system. The parameters used for the simulations are presented in Table 3.

Table 3. Simulation parameters.

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| Number of positions | $n = 32$ | Size of pieces in memory positions | $m = 8$ |
| Number of segments | $s = 4$ | Size of entries in octets | $r = 4$ |
| Residence time minimum in µs | $t = 7$ | Number of ports | $p = 3$ |
| Number of gates (dual port mem.) | $g = 2$ | Number of octets (MACo + SN) | $c = 3$ |
| System clock frequency (MHz) | $f_{gs} = 100$ | System clock period (ns) | $T_{gs} = 10$ |

### B. Simulations

Figure 14 depicts a search with a negative result and the writing of the new entry in the memory. *Port 0* starts looking for *0x801b*. After rounding the whole memory, the search is completed without finding the value. System answers with *output_valid(0)='1'* (output signal valid in port 0) and *hit_out ='0'* (not found). *Data_out* and *address_out* indicate the written data and the position in which it was stored. After another $c_{search\_notfind} = 4$ cycles, the system returns to the previous situation and continues the process.

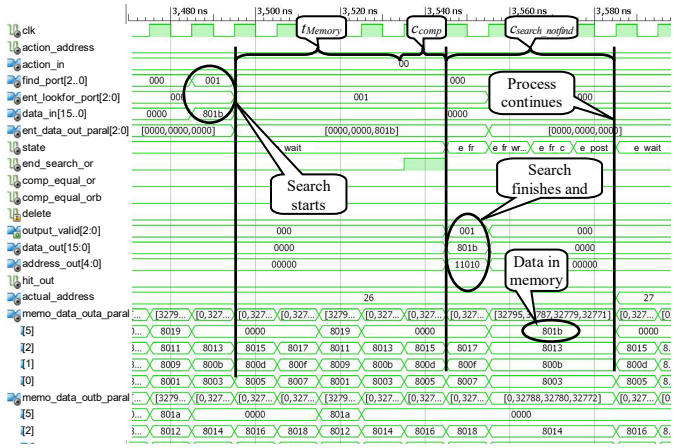



Fig. 14. Search in which data was not in memory. Process lasts $t_{Memory}$ + 5 clock cycles.

Figure 15 depicts two simultaneous searches with a positive result. Each piece of data found adds $c_{comp}$ + $c_{search\_find}$ = 4 clock cycles to the process. The first search is started by *port 2* and looks for *0x101b* (the last 3 octets *0x01b*). The second search is started by *port 1* and looks for *0x201e* (the last 3 octets *0x01e*). When the first piece of data is found the following is indicated: *output_valid(2) = '1'* (output valid in port 2) and *hit_out = '1'* (found); *address_out* indicates memory address *"11010"* and *data_out* gives data which was in that position *0x801b*. Data is updated by adding new bits of the most significant byte (logic "OR" function): "*0x1 OR 0x8 = 0x9"*; and new data stored in memory will be *0x901b.* The second search (*0x201e*) continues and when data is found, the system returns the old value (*0x801e*) stored in the memory and updates this (*0xa01e*) in the same way.

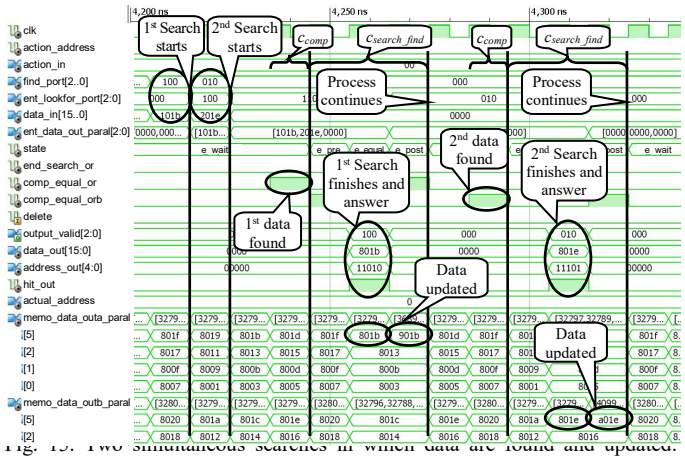



Fig. 19. Two simultaneous searches in which data are found and updated. Each successful search adds 4 clock cycles = $c_{comp} + c_{search\_find}$.

As seen in the time diagrams presented, the system that has been developed complies with the established design requirements.

## VII. Conclusions and Future Work

This work presents a memory system for detecting duplicates and circulating frames in HSR and PRP protocols, which are defined in the IEC 62439-3. The proposed approach fulfills the strict latency, throughput and reliability requirements of power utility automation networks, as described in the recently published (2013) first edition of the IEC 61850-90-4 [3].

This research proposed a segmented memory of 1024 positions (16x64) as a technical alternative because it covers the widest range of possible generic scenarios. For systems with fewer available resources; 128, 256 or 512 positions may suffice, if the observed limits of number of nodes, traffic structure, application and throughput are taken into account.

The proposed memory management method is applicable to DANs and Redboxes for PRP and HSR networks in a medium size FPGA, with good performance for power utility automation networks. For other applications in which high availability may be desirable, the general operation will probably have more relaxed restrictions than substations. Therefore, performance would be appropriate and much better.

Future work would include testing the solution in HSR/PRP nodes and Redboxes for real networks to be applied in substations or power utility automation networks in general. Further development in this field also includes analysis of PRP and HSR combined networks, introduction in the model of IEEE 1588 frames processed on the fly and the study of the effect of Ethernet frame authentication in each node. Reliable Ethernet Networks, synchronization and cyber-security are hot research topics. They establish the basis for the new generation of Cyber-Physical-Production-Systems that pose new challenges for industry and for the research community.

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