Performance of a superconducting breaker for the protection of HVDC grids

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Abstract: Future multi-terminal high-voltage direct current (HVDC) grids will be essential for the electric power system expansion. However, there are still several technical, economic and legal obstacles that interfere with the construction of those grids. One of the main technical issues is the interruption of DC currents when a fault occurs, due to the high values of DC fault currents that can exceed the DC circuit breaker's (DCCB) interruption capability in few milliseconds. In order to overcome that limitation, a superconducting DCCB (S-DCCB) is presented in this study. The proposed S-DCCB is based on the combination of a superconducting fault current limiter, a mechanical DC circuit breaker and a current limiter reactor. The presented S-DCCB is modelled and simulated by PSCAD/EMTDC software on a four-terminal HVDC system. Its behaviour is proven to be satisfactory for several fault scenarios. DC fault currents are initially limited and afterwards interrupted by the S-DCCB in an operation time that fulfils DC grids' protection requirements.

1 Introduction

Currently, high-voltage direct current (HVDC) links are used for the electric power system expansion. These HVDC links can be found nowadays in submarine connections of isolated systems, such as offshore wind farms, gas platforms or islands. They are also adequate for the reinforcement of existing AC grids and the interconnection of asynchronous AC grids. With an increasing number of point-to-point HVDC links, it would be optimal to connect them directly, whenever it is technically feasible, building multi-terminal HVDC (MTDC) grids. Several MTDC links have been in service for some years (e.g. the Quebec-New England system, the SACOI link). More recently, the Zhoushan link was commissioned in 2014 and the North-East Agra system in 2017. Supergrid DC topologies, such as an European supergrid [1], have also been proposed in the literature based on the MTDC concept. Nevertheless, there are still several factors hindering the evolution of those MTDC links [2, 3].

Grid protection is one of the main technical obstacles, given that the recently commercially available DC circuit breakers (DCCBs) have a restricted current breaking capability and operation speed that is associated with very high costs. In point-to-point HVDC systems, fault protection was assured by the trip of AC-side breakers. However, in MTDC grids, this procedure is not the optimal solution for a secure power supply and hence, possible alternative DC protection schemes and detection algorithms are under study, as introduced in [4]. A possible approach is to reduce the fault current and then, interrupt the limited current with conventional circuit breakers. Fault current limiting technologies are traditionally classified in conventional and advanced technologies. On the one hand, conventional technologies rely on building new substations, bus splitting, upgrading the existing circuit breakers, current-limiting reactors (CLRs) [5], or high resistance grounding. However, conventional solutions present several technical and economical disadvantages [6]. On the other hand, the solid-state fault current limiters (SS FCLs) [7] and superconducting fault current limiters (SFCLs) stand out among the advanced technologies, due to their high efficiency [8]. The performance of a SS FCL in a two-terminal voltage source converter (VSC)-HDVC was already studied by the authors in [9] and the electromagnetic simulations showed a fast and correct response. Also, fault current limitation by SFCLs has been

thoroughly analysed for both AC and DC systems. Thus, Schettino *et al.* described in [10] the use of a resistive SFCL in a 12 bus high-voltage CIGRÉ benchmark AC transmission system. Also for direct current, the resistance varying characteristics of SFCL have been considered in [11]. Therefore, SFCLs are a promising solution for future MTDC grids, due to their low impedance during normal conduction state and rapid increase of impedance under faults. Repetitive operation with an adequate recovery is also provided [12].

Given the performance of SFCLs for DC systems, several authors have studied the combination of SFCLs with lower rating circuit breakers as a feasible solution for the protection of MTDC links. In [8], the authors present the experimental results of a DCCB consisting of an SFCL connected in series with a conventional gas circuit breaker. The superconductor's limiting capacity increases the breaking capability of the DCCB and thus, it is pointed out as an emerging technology for DC current interruption. However, the application of the interrupting device is restricted to an MV DC circuit. Other authors have also worked on solutions based on the combination of mechanical DCCBs (M-DCCB) with SFCLs. Garcia *et al.* introduced a protection strategy for a three-terminal HVDC system based on the series connection of a resistive SFCL with a M-DCCB in [13]. Existing M-DCCBs are capable of interrupting HVDC currents within several tens of milliseconds, but this is too slow to satisfy the requirements of a reliable HVDC grid. DCCBs based on the solid state semiconductors (SS-DCCB) can easily overcome the limitations of operating speed, but they need a large number of electronic switching devices that cause excessive losses. To overcome these shortcomings, [14] introduces a topology of hybrid DCCB (H-DCCB). The use of H-DCCBs allows to interrupt higher fault currents in shorter times [15]. Also, Khan *et al.* present in [16] a modification of a H-DCCB, by replacing the CLR with a SFCL. This innovation allows installing a H-DCCB with a lower breaking capability and moreover, the device can interrupt bidirectional current flows. Its effectiveness is validated by simulation means in MTDC systems. However, the installation of an H-DCCB and superconducting tapes increases the overall cost of the solution.

As an alternative, the present paper studies the performance of a superconducting DCCB (S-DCCB), which consists of a series connection of the SFCL with an active current injection M-DCCB and a CLR. The inclusion of the reactor reduces the requirement
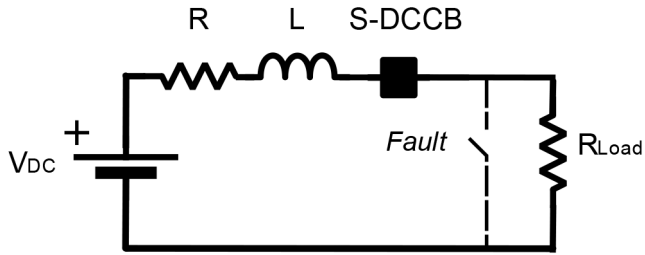
for fault current limitation of the SFCL, by limiting the initial rate-of-change of current. Thus, the critical current of the superconducting tape is reduced. The design of the S-DCCB was already introduced by the authors in [12], where three DCCB concepts were compared: active current injection M-DCCB, SS-DCCB and H-DCCB. It was concluded that by the use of the SFCL the response of the hybrid and active current injection CBs are equalised in terms of maximum current breaking capability. Therefore, with an SFCL it is easier to adapt the response of the system to the maximum rating of a DCCB. Thus, the M-DCCB can be suitable for the protection of HVDC systems, since higher interruption times do not lead to higher fault currents when SFCLs are used.

In the present paper, the performance of the S-DCCB with an M-DCCB is assessed in four-terminal HVDC systems for different fault scenarios. Protection algorithm strategies are out of the scope of the paper and can be studied in other references, such as [17]. The paper is structured as follows. The S-DCCB is presented in Section 2, where the design of the device is justified in order to meet the requirements needed for a fault interrupting device in an MTDC. The S-DCCB is based on a resistive-type SFCL and its model is introduced in Section 3, where the model is validated with a test DC circuit, after parameterisation according to the test circuit characteristics. In Section 4, the S-DCCB is installed in an MTDC system and its performance is evaluated under different fault scenarios. The sensitivity of the fault interruption process is studied in Section 5 and finally, the conclusions of the paper and further work are presented in Section 6.

2 Design of the superconducting breaker

The protection device for MTDC systems proposed in this paper consists of a resistive SFCL in series connection with a conventional M-DCCB and a CLR, as shown in Fig. 1. Thus, the fault current will be restricted by both the SFCL and the CLR up to the maximum interruption capability of the DCCB. In order to protect against overvoltage during the current interruption, a surge arrester is connected in parallel with the DCCB, whereas the SFCL will be protected by a fixed shunt resistor.

2.1 Requirements of a fault interrupting device in HVDC grids

The fault interrupting device proposed in the present paper is designed for modular multilevel converter (MMC) technology, which is considered as a suitable technology for HVDC grids. Half-bridge topology is extensively used on account of the reduced cost and losses, although these cells do not have DC fault blocking capability [18].

The features of the converters determine the design of the HVDC fault interrupting device. Nevertheless, the characteristics of DC faults must also be considered, as these faults delimit the demand of the protection system. DC faults are characterised by a high rate of the rise and high steady-state current. In an HVDC grid the DCCB must guarantee the fault clearing of the affected line without a large system outage [2]. A fault interrupting device for DC grids should meet the following requirements [19]:

- A high current breaking capability, especially for HVDC grid protection.
- A fast operation time, in order to protect the converter equipment from damage.
- A counter voltage capability, which must be larger than the grid voltage, in order to demagnetise the grid inductance and dissipate the magnetic energy in the circuit.

The main transient parameters of the DC interrupting device are its current breaking capability, interruption time, maximum voltage withstand capability and the repetitive current interruption capability. In addition, the rated continuous characteristics of the device must also be adequate for the installation point, namely the rated current, overload current, and rated voltage.

Among the abovementioned parameters, current breaking capability comprises the breaking capability of the DCCB,

Fig. 1 *Design of the S-DCCB*

considering that the fault current has been limited by the SFCL and the CLR. Interruption time includes from fault inception instant until the final current suppression. Nevertheless, as the paper considers S-DCCB, quenching time and recovery time must also be taken into account. However, recovery time is negligible in permanent faults. When the effective fault interruption is verified with a proper algorithm, the active power flow of the voltage is restored by the converter control [13].

2.2 Design of the DCCB in the S-DCCB

An M-DCCB is the main component of the fault interrupting device for HVDC grids proposed in the paper. The operation principle of the DCCB is based on the active current injection concept. The DCCB is composed of three parallel paths as shown inside the dotted rectangle in Fig. 1: nominal current path, commutation path and energy absorption path. The nominal current path consists of a conventional circuit breaker. The commutation path is constituted by a pre-charged capacitor C_{DC} in combination with an inductance L_{DC}. The pre-charging of the capacitor is performed by a DC power supply.

The operation of the DCCB is based on the generation of an artificial zero crossing by active current injection. Therefore, the capacitor discharges through the inductance. Finally, a zero crossing is generated, which leads to a current interruption in the nominal current path. The remaining energy is dissipated in a surge arrester bank.

M-DCCBs are robust and present a rather fast operation. Nevertheless, they are the slowest option among DCCB types and are commonly considered as non-suitable for HVDC grids [2]. Fault currents in meshed HVDC grids can be very large. Hence, in order to limit fault currents, an SFCL and a CLR will be used in the S-DCCB presented hereby.

The surge arrester in the energy absorption path of the DCCB limits the recovery voltage. Besides, the deionisation of a DC fault is achieved through the counter voltage provided by surge arresters, which must have an increased energy absorption capability. Thus, the counter voltage amplitude must be set to 1.5 times the maximum DC side voltage and its minimum energy dissipation capability will be adapted to the project characteristics [20].

2.3 Design of the SFCL in the S-DCCB

The resistive SFCL must reduce fault currents down to values within the current breaking capability of the DCCB. Under normal operation, SFCLs present negligible resistance, when the temperature is maintained within the critical temperature. However, for faults exceeding a critical current, the resistance increases and as a result, the fault current is restricted. Hence, SFCLs produce a fast and effective current limitation within the first current rise and allow repetitive operation with fast and automatic recovery [13]. The main design parameters of a resistive SFCL are its critical current, response time and minimum and maximum resistance.

Regarding the design of the SFCL as part of an HVDC fault interrupting device, different approaches have been considered in the literature. Some authors use generic SFCLs with specific size

Fig. 2 *Test circuit for S-DCCB validation*

Table 1 Specifications of the DC Test Circuit

Parameter	Symbol	Value
DC voltage source	V_{DC}	400 kV
source resistance	R	1 Ω
source inductance	L	0.1 H
R_{min} of SFCL	$R_{SFCL\ Min}$	0.1 Ω
R_{max} of SFCL	$R_{SFCL\ Max}$	131 Ω
critical current	I_c	1.875 kA
transition time	τ	2 ms
inductance of DCCB	L_{DC}	290 μH
capacitance of DCCB	C_{DC}	17.7 μF
current breaking capability of DCCB	I_b	3.5 kA
surge arrester reference voltage of DCCB	—	1.5 p.u.
fault neutralisation time of DCCB	—	5 ms

and standard parameters, such as Khan *et al.* in [16, 21] and Mokhberdoran *et al.* in [22]. Other authors design the limiter in the function of the specifications of the project. As an instance, Xiang *et al.* in [8] select the length of a YBCO superconductor tape based on the rated voltage of the DC system. Also, Garcia *et al.* in [23] study a REBCO tape and its sizing is based on technical and economic criteria. The critical current of the tape is 3200 A and determines the width of the tape. The length of the superconducting material is set by the rated voltage and the limitation duration, which is considered to be two times the total clearing time. In the present paper, the maximum resistance of SFCL is selected based on the project characteristics (Section 3), but the manufacturing characteristics of the limiter are out of the scope of the work.

2.4 Design of the CLR in the S-DCCB

The main purpose of the CLR in the DC breaker is to reduce the rate of the rise of current and to limit the fault current peak. In the S-DCCB presented in the paper, fault current limitation will be implemented by the combined action of the CLR and the SFCL, as shown in Fig. 1. However, there are three main trade-offs in limiting reactors design [24]. On the one hand, fast current changes will be hindered and the impact of the reactor on system stability will have also to be assessed. On the other hand, the application of a large line reactor is constrained by its cost and physical size as well as its impact on the controllability of the HVDC grid [2].

3 Modelling and validation of the superconducting breaker

The model of the S-DCCB is described in this section and validated with a test circuit.

3.1 Modelling of the S-DCCB

The complete model of the DCCB proposed in the present paper includes the model of an SFCL element, the model of an M-DCCB with active current injection principle and the CLR. Both the SFCL and the CLR are installed in series in the main current path (Fig. 1). The SFCL and CLR models must be parameterised according to the current breaking capability of the DCCB. The model of the

DCCB is composed of three parallel paths, as indicated in Section 2.

The model of the SFCL element consists of the superconducting material and a parallel resistor, which reduces overvoltage during faults and diverts fault current. Several modelling approaches have been considered in the literature, as indicated in [25]. In the present paper, the SFCL has been represented by an exponential model, characterised by the following parameters: critical current I_c, transition time τ, and minimum and maximum value of the quenched resistance ($R_{SFCLmin}$ and $R_{SFCLmax}$, respectively). Based on the literature, the critical current is set to 1.5 p.u. and the response time to 2 ms, which is the transition time needed to reach the quenched resistance after the fault current exceeds the critical current. The resistance of the SFCL is shown in (1).

$$\begin{aligned} R_{SFCL}(t) &= R_{SFCL\ Min}, && \text{if } i < I_c \\ R_{SFCL}(t) &= R_{SFCL\ Max} \cdot \left(1 - e^{-((t-t_0)/\tau)}\right), && \text{if } i \geq I_c \end{aligned} \quad (1)$$

where t is the time, t_0 is the first instant once the fault current is higher than the critical current and $R_{SFCL\ Max}$ at each pole is calculated as indicated below

$$R_{SFCL\ Max} = \frac{(v_{DC}/I_b) - R_{conv}}{2} \quad (2)$$

where

$$R_{conv} = \frac{v_{DC}}{I_p} \quad (3)$$

R_{Conv} is the equivalent resistance added by the VSC converter to the circuit in fault state. This parameter has been calculated with an equivalent reduced model [26]. v_{DC} is the voltage of the DC bus, I_p is the prospective peak value of short-circuit current, I_b the peak value of the current limited by the SFCL (and hence, it defines the breaking capability of the DCCB) and $R_{SFCLmax}$ is the maximum value of the quenched resistance. It must be taken into account that in a symmetric configuration half of the maximum resistance is necessary for each pole.

The limiting factor (LF) is the ratio between the prospective current, I_b, in the absence of the SFCL device and the limited current, I_p, in the presence of the SFCL, as indicated below

$$LF = \frac{I_b}{I_p} \times 100 \quad (4)$$

3.2 Validation with a test circuit

In the present study, the S-DCCB, as designed in Sections 2 and 3, will be validated through simulation means with a test circuit [15]. The test circuit is composed of an ideal 400 kV DC source, source resistance and inductance R and L, the fault interrupting device under test S-DCCB (detailed scheme in Fig. 1) and a resistive load R_{Load} (Fig. 2). Table 1 indicates the parameters of the test circuit and includes the parameterisation of the S-DCCB. Note that the fault neutralisation time comprises the relay time for detection.

The model of the proposed S-DCCB has been validated with the simulation of a permanent pole-to-pole fault at 2.0 s. Fig. 3 depicts the current of the circuit. The dotted line represents the current with the CLR and SFCL but without the SFCL and the solid line shows the limited current with the CLR, SFCL and DCCB.

Therefore, the proposed model reduces the fault current to a lower value that will not damage the components of the system and which can be interrupted by M-DCCBs. Therefore, the operation of the protection system must not be so critically fast and there is slightly more time available for the tripping of the circuit breaker. In this manner, the operation time of the M-DCCB is appropriate for the system, in spite of being larger than the H-DCCB′s
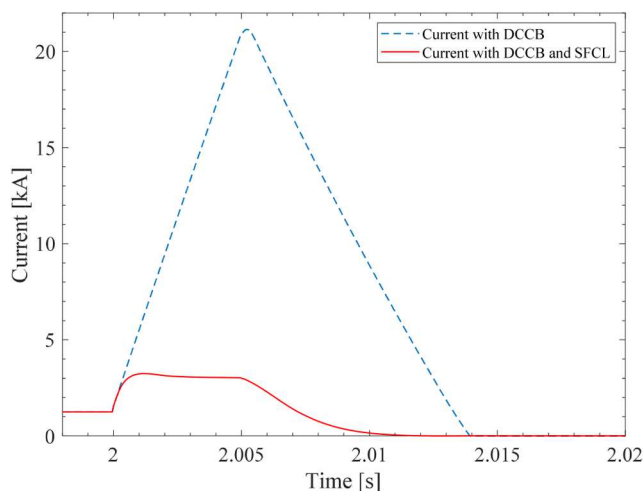
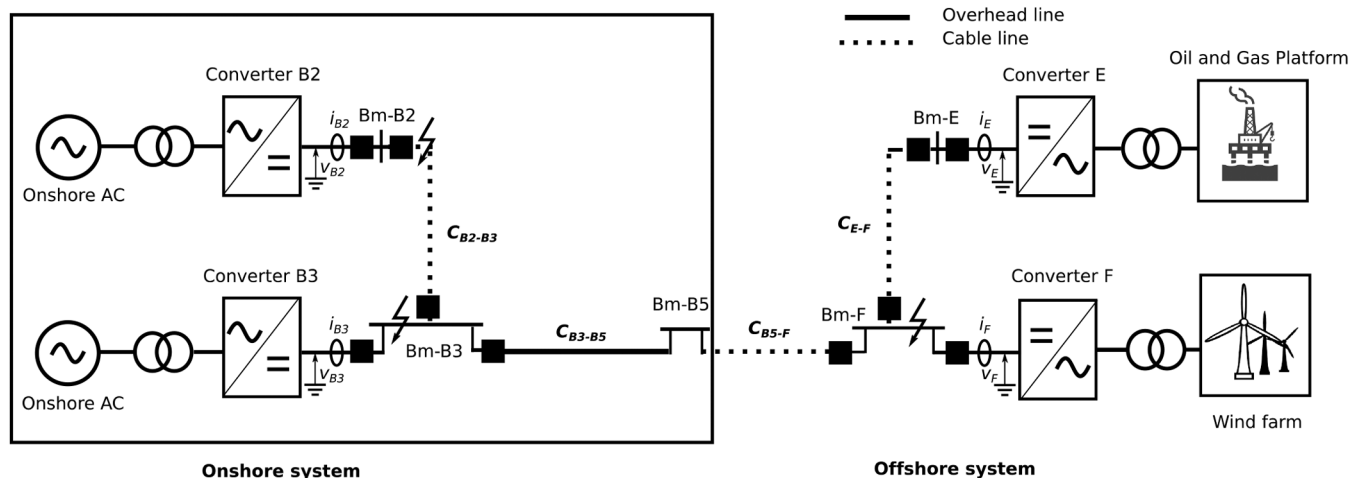**Fig. 3** *Current of the test circuit with and without SFCL*

Fig. 4 *Four-terminal symmetric monopole HVDC system*

Table 2 Specifications of the MTDC System

Parameter	Symbol	Value
AC converter side voltage (B2-B3)	V_{AC}	380 kV
AC converter side voltage (E-F)	V_{AC}	145 kV
frequency	F	50 Hz
AC grids short-circuit power	S_{SC}	30 GVA
DC rated voltage	V_{DC}	±200 kV
MMC converter arm inductance	L_{arm}	15%
length and type of line B2-B3, E-F	C_{B2-B3} C_{E-F}	200 km cable
length and type of line B3-F	C_{B3-B5} C_{B5-F}	100 km overhead in series with 100 km cable

operation. As a consequence, the S-DCCB model is hereby validated since it fulfils the requirements stated in Section 2.

4 Performance of the superconducting breaker in an MTDC system

The performance of the S-DCCB proposed in this paper has been studied within the MTDC system shown in Fig. 4 with PSCAD/EMTDC software package.

The MTDC system under analysis is based on the CIGRÉ B4 DC grid test system. This system is an MTDC symmetric monopole HVDC link composed of four MMC half-bridge converters. Converter B2 and B3 are connected with AC grids, converter F is a 500 MW wind power plant and converter E is a 33

MW offshore load. Table 2 shows the specifications of the MTDC system.

Grid side converters, B2 and B3, control the voltage and active power/reactive power, whereas converter F controls active and reactive power and converter E controls voltage and frequency. Valves are protected against overcurrent with a maximum IGBTs current limit of 2 p.u. The S-DCCB is represented by a black square. Each pole of all DC links includes an S-DCCB, as validated in Section 3.2. Therefore, when there is a fault in a line, the SFCLs operate and a trip order is given to the respective circuit breakers.

Protection algorithms are out of the scope of the paper. Nevertheless, it must be noted that a detection delay of 1 ms has been considered, as well as travelling waves delay of 1 ms per 200 km. The results of the study cases depict the currents and voltages measured in the points shown in Fig. 4.

In HVDC symmetric monopole systems, pole-to-pole faults are the most severe events, because of the produced high-fault currents. Therefore, these faults have been thoroughly analysed in this section. Nevertheless, pole-to-ground faults have also been briefly considered. Finally, the sensitivity of the S-DCCB on the MTDC system is studied when the fault location, fault resistance, SFCL transition time, SFCL triggering current and CLR size differ.

4.1 Pole-to-pole fault

A permanent solid pole-to-pole fault is applied at bus Bm-F at 2.0 s. Fig. 5 shows the prospective voltage and current of converter F as well as the actual voltage and limited current of converter F, with the S-DCCB. In order to analyse the DCCB stresses during the breaking process, Fig. 5 also depicts the components of the
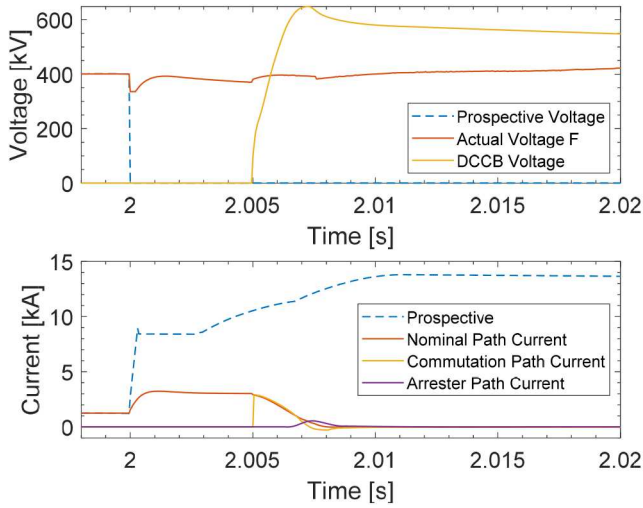
Fig. 5 *Prospective and limited voltage and current for converter F*
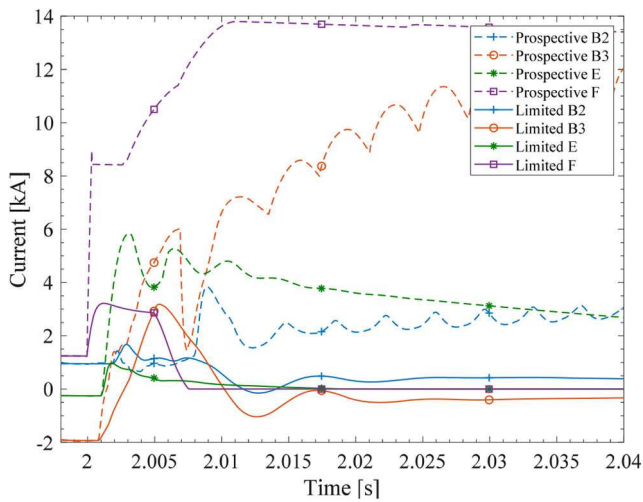
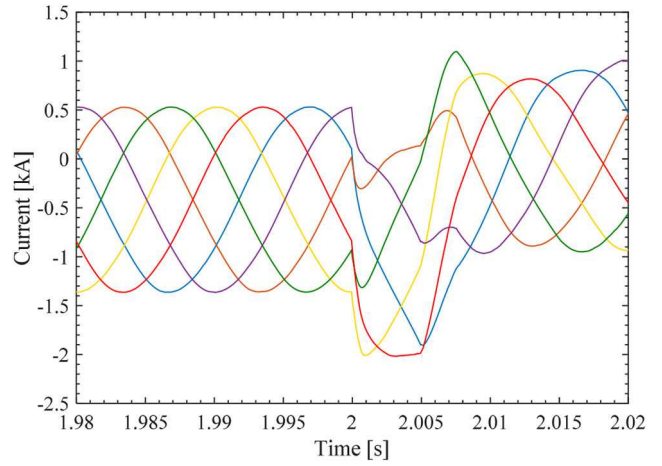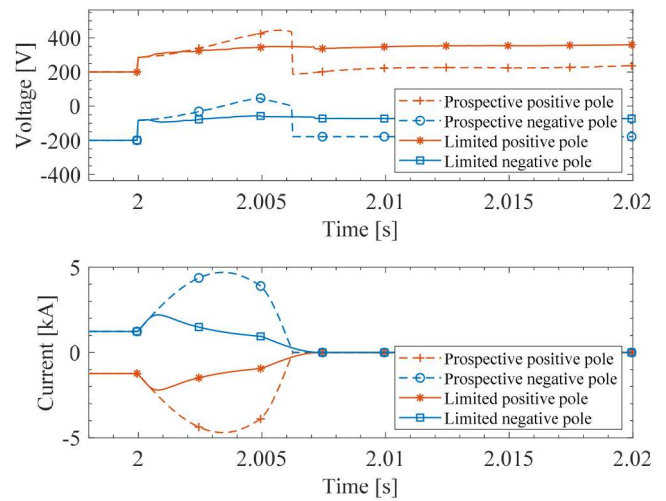**Fig. 6** *Prospective and limited currents for converters*

Fig. 7 *Arm currents of converter F*

Fig. 8 *Prospective and limited voltage and current of converter F for negative pole-to-ground fault at bus Bm-F*

current distribution within the three DCCB paths and the voltage across it.

The nature of the CLR limits the rising rate of the discharge current. When the current reaches the critical value, the FCL quenches and develops an exponential resistance that limits the peak current in converter F to 3.22 kA. This value is below the breaking capacity of the DCCB. Hence, the operation of the S-DCCB brings the current exponentially to zero in a few milliseconds, resulting in an interruption time of 7.6 ms. The LF is 64.02%. Regarding voltage, although there is a sharp initial decrease in steady-state, it is within the admissible voltage limits (0.84 p.u.) due to the action of the S-DCCB, finally, the rated value is kept.

Fig. 6 shows the prospective current with no S-DCCB and the limited current due to the operation of the S-DCCB for all converters. In the MTDC system, the travelling waves spread away from the fault point at a given speed which is determined by the LRC characteristics of the overhead lines and submarine cables. Once the wave reaches the end of the faulted line, part of it will be transmitted to the other side of the bus. The impedances of the lines determine the transmission coefficients of the wave. Accordingly, converter F must withstand the highest stress, as it is located near the fault. This converter is the most affected one and the connection with the mainland is lost when the DCCBs of line B3-F trip. In those conditions, initially, the offshore park cannot continue feeding the load whilst the AC grids continue operating after recovering. This way, reliable DC grid operation is ensured, as the S-DCCB can guarantee fault clearing without a large system outage.

The SFCLs limits the peak currents from 6.03 to 3.18 kA in converter B3, from 3.83 to 1.68 kA in converter B2 and from 5.85

to 0.97 kA in converter E. Therefore, the LFs are 52.74% in converter B3, 43.86% in converter B2 and 83.42% in converter E, respectively.

In order to validate the correct performance of the proposed S-DCCB in the MTDC system operation, the most stressed converter has been studied. Thus, the limited arm currents for converter F are shown in Fig. 7. As represented in the time evolution graphic, the converter currents are below the maximum withstand capability and therefore, they operate within the safe operating area. Even though the fault is located adjacent to converter F, it does not block the converter. Accordingly, it can be concluded that the operation of the superconducting DCCB is suitable for the MTDC system operation.

4.2 Pole-to-ground fault

In this section, the performance of the S-DCCB is briefly discussed in a pole-to-ground fault at bus Bm-F. A negative pole-to-ground fault is produced at 2.0 s. The voltage and current for both poles in converter F, with and without the S-DCCB, are displayed in Fig. 8. The current and voltages of both poles are symmetric, as a result of having considered a monopolar system.

The prospective values show the evolution of the voltages and currents with no S-DCCB. The voltage of the affected pole drops to −47.44 kV, whilst the voltage of the other pole rises. Consequently, the current increases.

With the proposed S-DCCB, the current peak is limited from 4.69 kA to 2.21 kA (LF of 52.88%), and the voltage is reduced to −56.54 kV.
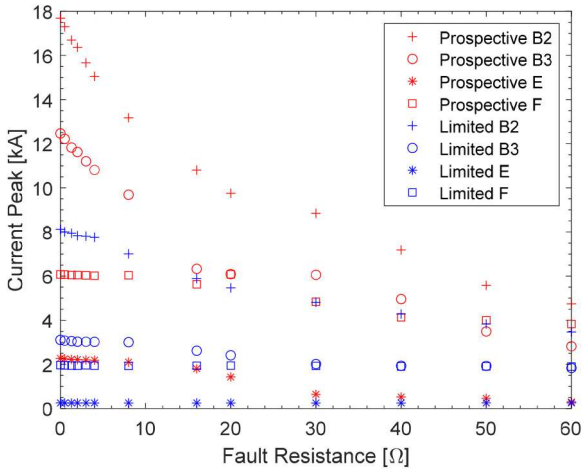
Fig. 9 *Prospective and limited peak currents for different fault resistances. Pole-to-pole fault at line B2-B3*
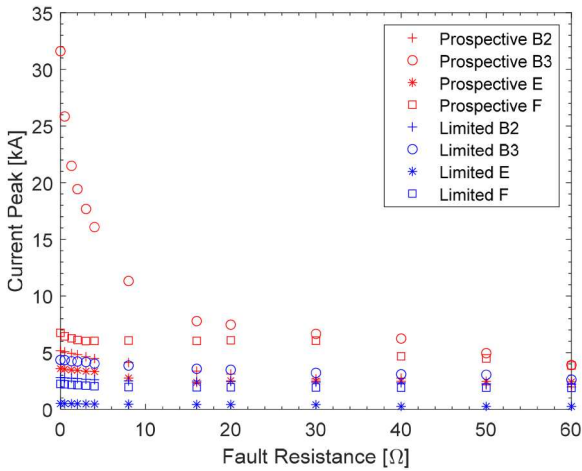

Fig. 10 *Prospective and limited peak currents for different fault resistances. Pole-to-pole fault at bus Bm-B3*
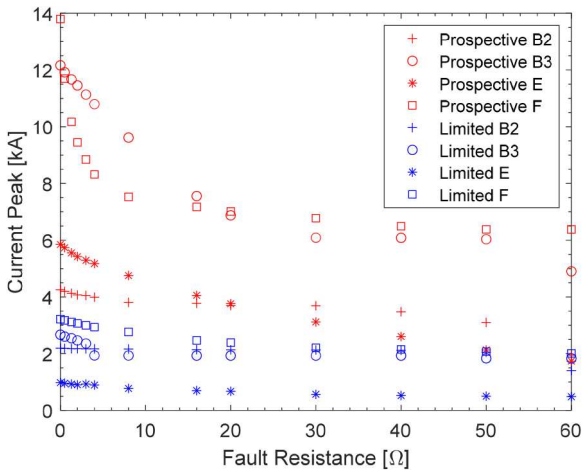

Fig. 11 *Prospective and limited peak currents for different fault resistances. Pole-to-pole fault at bus Bm-F*

5 Sensitivity of the fault interruption process of the superconducting breaker

5.1 Influence of fault resistance

Next, the influence of fault resistance is discussed for pole-to-pole faults with different fault locations. In this section, the worst fault case scenarios have been considered. Therefore, faults are located at the end of line B2-B3 (Fig. 9), at bus Bm-B3 (Fig. 10) and at bus Bm-F (Fig. 11), as shown in Fig. 4. The resistance of the fault
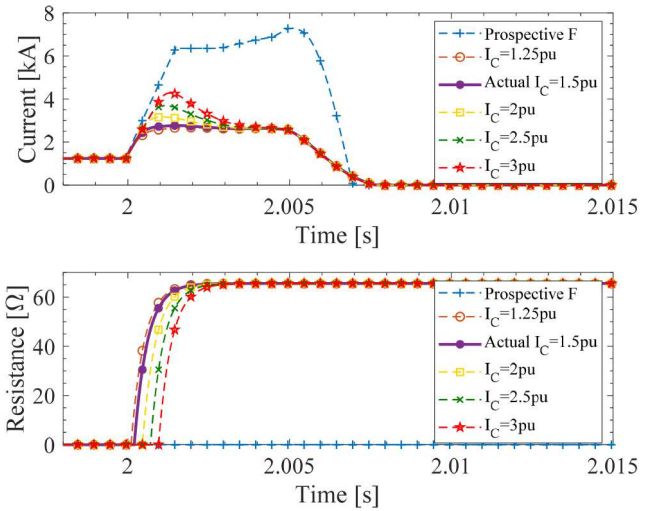
Fig. 12 *Prospective and limited currents and R_{SFCL} for different critical currents*

Table 3 Peak currents for different critical currents

I_C, p.u.	Peak current, kA
	7.2843
1.25	2.6808
1.5	2.7657
2	3.1629
2.5	3.6915
3	4.2808

varies between 0 and 60 ohm in each case. It can be seen in the figures that higher resistances in the current path lead to less severe current stresses. Limited currents due to the SFCL are significantly smaller than prospective currents.

The worst-case scenarios can be observed in solid faults, in the converter which is located closer to the fault point. There are two particularly remarkable cases. In faults near Bm-B2 (Fig. 9), converter B2 withstands the highest limited peak current, 8.12 kA. Besides, in Fig. 10, the most severe current stress appears in converter B3. The proposed device restrains the prospective peak fault current from 31.61 to 4.35 kA. These figures are decisive for determining the rating of the DCCBs located in those points, as the DCCBs should have a higher breaking capability than the restricted fault currents.

5.2 Influence of SFCL characteristics

For previous cases, the characteristics of the SFCL in the superconducting circuit breaker under study correspond to the values indicated in Table 1. However, the present paper enlarges the study to the analysis of the impact of the critical current (I_C) and transition time (τ) on the system performance. This sensitivity analysis is based on the fault case scenario analysed in section 4.1, i.e. a pole-to-pole fault at bus Bm-F, at 2.0 s with a 0 Ω fault resistance.

In Fig. 12, several critical currents from 1.25 to 3 p.u. have been considered. Table 3 summarises the peak currents exposed in Fig. 12. For bigger triggering currents, the transition time enlarges and the resistance of the SFCL increases later. As a result, peak currents and fault current rise time variation are higher. The considered smaller critical current of 1.25 p.u. leads to a peak current of 2.68 kA, whilst for 3 p.u. the peak current is 4.28 kA.

In Fig. 13 the influence of the transition time between 1 and 4 ms is analysed. Table 4 digests the peak currents in Fig. 13. A transition time of 1 ms, leads to a peak current of 2.63 kA. For larger transition times, the resistance of the SFCL is developed slower and the peak currents increase. Therefore, for 4 ms, the peak current is 3.24 kA. Once again, it is verified that smaller transition times lead to the lowest peak currents.
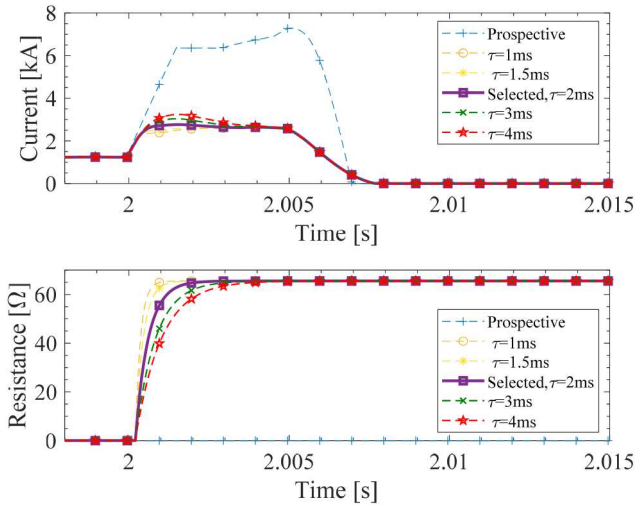
Fig. 13 *Prospective and limited currents as well as R_{SFCL} for different transition times*

Table 4 Peak currents for different transition times

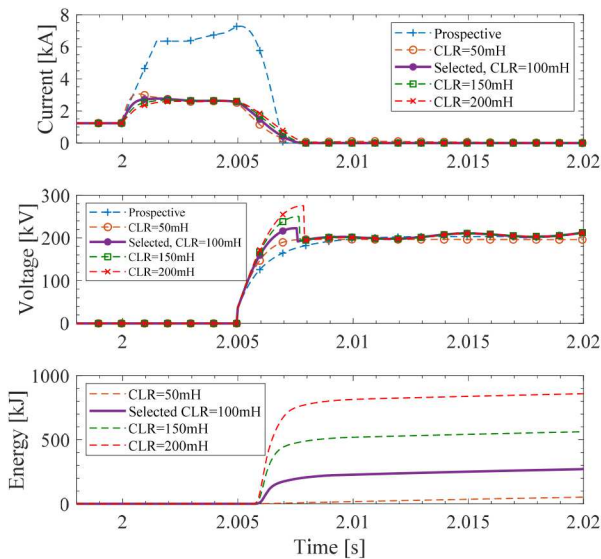| τ, ms	Peak current, kA
—	7.2843
1	2.6344
1.5	2.6363
2	2.7657
3	3.038
4	3.2401

Fig. 14 *Prospective and limited currents and voltages as well as surge arrester energy for different CLR sizes*

Table 5 Peak currents and voltages for different CLR

CLR, mH	Peak current, kA	Peak voltage, p.u.
0	7.2843	1.164755
50	3.0633	1.0035835
100	2.7677	1.165605
150	2.6696	1.251357
200	2.634	1.376492

5.3 Influence of CLR size

This subsection analyses the impact of the size of the reactor in the S-DCCB design. The objective is to reduce the current to a value that is below the breaking capability of the circuit breaker, for

successful protection of the MTDC system. A larger CLR value reduces the peak current and smoothens the initial change of the rate of current after the fault occurrence. In Fig. 14 the performance of converter F is shown for CLRs that vary from 50 to 200 mH. Table 5 summarises the peak currents and voltages shown in Fig. 14. Once more, the same fault analysed in Section 4.1 is considered. Thus, a 200 mH CLR results in a 2.63 peak current, whilst a 50 mH CLR leads to 3.06 kA. Besides, larger line reactors increase the circuit breaker maximum voltage, from 1.16 p.u. with a 100 mH reactor to 1.37 p.u. with a 200 mH reactor. However, higher CLR values, increase the system line constant and difficult the performance of the control system. Moreover, it must also be considered the impact of the CLRs in the energy that the DCCB must dissipate. With this objective, Fig. 14 shows the energy in the surge arrester bank of the DCCB. It can be observed that the energy increases sharply for higher CLR values.

The design parameter was initially set to 100 mH, as introduced in Section 2, which represents a good trade-off between the fault current limitation and the cost and bulk issues that can be determinant for offshore installations. In an HVDC grid, the CLR value must be optimised by considering the DCCB requirements, i.e. breaking capability, interruption time and surge arrester dissipation energy. Besides, the control and protection system requirements must be also considered. In protection systems, CLRs are used to demarcate the borders of protection zones by damping external signals. Therefore, the value of the CLR has a big impact on the selectivity of the protection algorithms.

6 Conclusions

An S-DCCB for MTDC systems has been presented in this paper. The proposed breaker is composed of an M-DCCB connected in series with an SFCL and a CLR. The model of the DCCB is based on the active current injection concept, whereas the SFCL is modelled as a resistive type. The aim of both SFCL and CLR is to reduce the current requirements of the circuit breaker.

First, the proposed S-DCCB design has been validated with a test circuit, in order to verify the limitation of the fault current by the SFCL within the breaking capability of the mechanical breaker. Then, its performance has been studied in an MTDC system with several fault scenarios, modifying the fault location and fault resistance. Pole-to-pole faults close to the offshore wind farm converter have been identified as the most demanding fault case scenarios. As a result of the simulation studies carried out for the present work, it can be concluded that the performance of the S-DCCB is correct because the fault current is neutralised in a reasonable time while its maximum is limited to a secure value. Converters are also prevented from getting damaged as current does not surpass 2 p.u. at any time. Furthermore, only affected lines and/or terminals are disconnected, leaving the rest of the system functional.

In addition, the sensitivity of the S-DCCB in the MTDC system has been analysed, including the influence of several design parameters of the SFCL. Thus, the maximum SFCL resistance, the transition time, SFCL triggering current and CLR size have been modified and the response of the MTDC system has been analysed. Based on the simulations, it can be concluded that smaller transition times lead to the lowest peak currents. Also, larger CLR sizes reduce both the peak current and the initial slope of fault current. However, it is known that larger CLR sizes lead to greater difficulty in system operation, so this compromise must be verified.

As a conclusion, the present work has verified that the proposed S-DCCB limits and interrupts the fault current properly with a low rating M-DCCB. Therefore, it shows good behaviour for the correct protection of the MTDC system. The proposed S-DCCB operates properly in the most demanding fault scenarios of the MTDC system.

7 Acknowledgments

8 References

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