

Analysis of DC-DC power supply systems for pulsed loads from green electronics perspective

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Abstract

Discontinuous loads frequently compromise the performance of their power source and electronics. They cause voltage and current ripple at the source and load, and introduces electromagnetic interferences. Also, they affect the efficiency of the power source. The aforementioned issues are particularly relevant in battery powered electronics. In order to minimize these unwanted effects, it is necessary to introduce a power supply architecture between the load and the source that should filter and/or regulate the currents and voltages. This architecture could be made solely of passive components or could use DC-DC regulators. The present work classifies and characterizes the most relevant architectures available. A novel switched power supply architecture for pulsed loads with adaptative input current is also introduced. A mathematical analysis of the conditions and characteristics that the regulated architectures should fulfil to obtain the maximum performance in terms of efficiency and green electronics are provided. The simulation and experimental results shown in this paper demonstrate the theoretical analysis.

I. INTRODUCTION

A load with a pulsed or discontinuous current consumption pattern compromises the performance of its power supply and electronics because [1], [2]:

- 1) It produces voltage ripple at the energy source and load terminals.
- 2) Current ripple at the input terminals is generated. This ripple increases the energy losses in the internal resistance of the power source. Consequently, it reduces the efficiency of the electronic system. Electromagnetic interferences are also introduced [3].
- 3) Depending of the power supply architecture, it requires over-sizing of the power supply electronics.

In order to reduce or eliminate all this technical problems, the use of basic filtering techniques with passive components with DC-DC converters is required [4]–[6]. Fig. 1 and Table I summarize the characteristics and performance of the most common power supply architectures available for pulsed loads [7]. [The architectures are classified in increasing order of electronics complexity and size. Their most significant parameters are compared with those of a direct connection between the load and power source. Fig. 1 shows the simplified block diagrams of the aforementioned power supply architectures and their expected input and load current and voltage waveforms.](#)

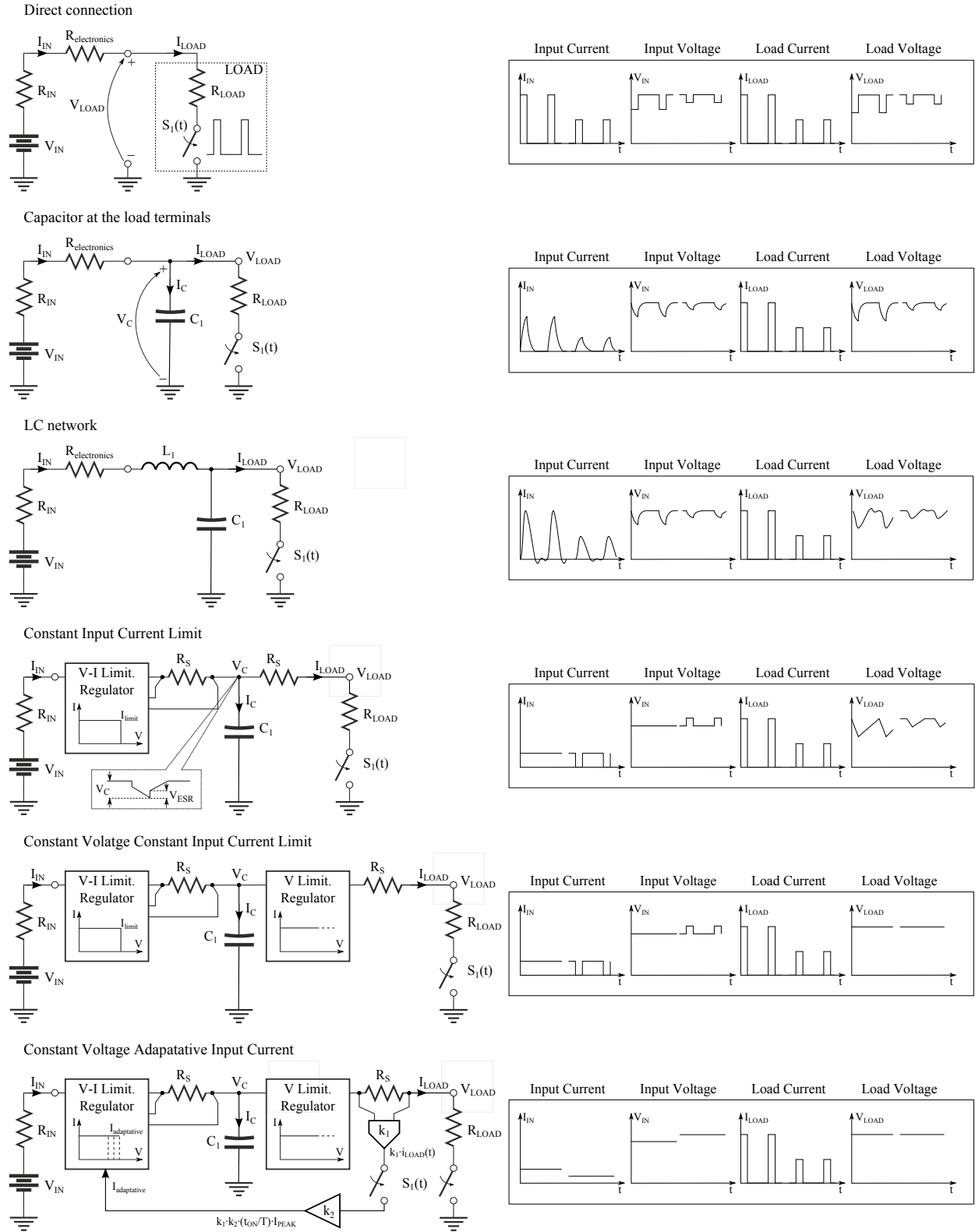


Fig. 1. Block diagrams and comparison between voltage and current waveforms of power supply architectures for systems with discontinuous loads.

TABLE I
COMPARISON OF POWER SUPPLY ARCHITECTURES FOR ELECTRONIC SYSTEMS WITH DISCONTINUOUS LOADS.

Parameter	Direct connection	Passive components		Voltage converters		
		<i>C in the load</i>	<i>LC network</i>	<i>Const. I limit</i>	<i>Const. Output V</i>	<i>COVAIC</i>
V_{IN} ripple	High	Medium	High	Medium	High	No
Overcurrent	No	No	Yes	No	No	No
Undercurrent	No	No	Yes	No	No	No
Efficiency	High	High	High	High/Avg.	High/Avg.	High/Avg.
EMC	Poor	Average	Poor	Average	Average	Average
Size	None	Medium	Medium	Medium /High	Medium /High	Medium /High
I_{IN} ripple	High	Medium	High	Low	Low	No
$I_{IN}(t = 0)$ overcurrent	Yes	Yes	Yes	No	No	No

Table I and waveforms of Fig. 1 highlight the COVAIC (Constant Input Output Voltage and Adaptive Input Current) architecture as the one that shows the best electrical performance [7]. This architecture maintains the input current and voltage constant, with independence of the value of the load current. It also does not present output voltage ripple. As a drawback it implies a complex architecture with a relatively high number of components, common to all DC-DC architectures [8]–[10]. Besides, its efficiency depends on of the architecture implementation and the pulsed load characteristic parameters [11], [12]. One of those alternative implementations of the COVAIC architecture could be based on the CUK architecture [13]. However, its main drawbacks are the loop stability and response and that CUK converter provides a negative output voltage.

From the perspective of green electronics, regulated architectures require further analysis of their efficiency in order to define the conditions that should be met to have good performance and high enough efficiency [14]–[17]. Although direct connection to the power source seems to have higher efficiency, regulated alternatives, like the COVAIC architecture, have less energy losses in the internal resistance of the power source. This is because the current that they sink is always the average current value, not the pulsed current waveform as in direct connection. This fact is particularly relevant in battery powered electronics, because it extends the battery life-cycle [18]–[20]. Therefore, regulated power supplies could also have better efficiency if certain conditions are met.

The present work studies which are the requirements that a regulated power supply architecture should meet to have the same or higher efficiency than a direct connection to the power source. This is done using a mathematical analysis of the efficiency of DC-DC converters for pulsed loads. The results are verified with an structural model [21] of direct connection between a Lithium-Ion battery and the pulsed load, and a model of COVAIC architecture [7]. In order to obtain a COVAIC architecture with high efficiency, an improvement of the basic architecture, is

presented.

II. EFFICIENCY ANALYSIS OF DC-DC REGULATORS FOR PULSED LOADS

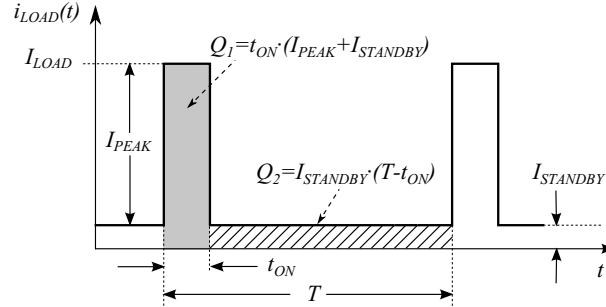


Fig. 2. Generic current waveform of a pulsed load.

The efficiency analysis of the architectures (Fig. 1) can be simplified in two test cases: direct connection and a generic regulated architecture [22]. The efficiency η_a for a direct connection is obtained as a function of the power source (P_{IN}) and the power losses (P_{LOSSES}) between the source and the load. In this case the only existing power losses are those produced in the battery internal resistance and protection electronics, thus:

$$\eta_a = \frac{P_{LOAD}}{P_{IN}} = \frac{P_{IN} - P_{LOSSES}}{P_{IN}}. \quad (1)$$

Fig. 2 shows the generic load current waveform. Examples of this type of loads are the wireless systems such as base stations, mobile terminals and wireless sensors, smartphones, energy harvesters, medical sensors, etc. The power losses in the distributed resistance ($R_{LOSSES} = R_{IN} + R_{electronics}$) and source internal resistance (R_{IN}) is solved in Eq. (2), where R_{IN} is the source internal resistance and $R_{electronics}$ the distributed resistance [21] between load and source. In this paper the standby current, $I_{STANDBY}$, is considered much smaller than the load current, I_{LOAD} to simplify the description without loss of the validity of the presented results.

$$\begin{aligned} P_{LOSSESa} &= R_{LOSSES} \cdot i_{INrms}^2(t) = \\ &= R_{LOSSES} \cdot \int_0^{t=T} i_{IN}^2(t) \cdot dt = R_{LOSSES} \cdot D \cdot I_{IN}^2, \end{aligned} \quad (2)$$

where V_{LOAD} is the nominal load voltage, I_{LOAD} the load peak current, R_{LOAD} the equivalent load resistance (which is a time function of V_{LOAD} and I_{LOAD}), T the load period, t_{ON} the active load cycle, and D the duty cycle (function of T and t_{ON}).

In these conditions and bearing in mind that $i_{IN}(t) = i_{LOAD}(t)$ for a direct connection, the efficiency of the system is:

$$\eta_a = 1 - \frac{R_{LOSSES} \cdot I_{LOAD}}{V_{IN}} = 1 - k, \quad (3)$$

TABLE II
PARAMETERS REFERENCE VALUES RANGE OF THE TEST CONDITIONS

Parameter	Value			Units
	<i>min.</i>	<i>nom.</i>	<i>max.</i>	
V_{IN}	3.0	3.6	4.2	V
R_{IN}	-	42	-	$m\Omega$
$R_{electronics}$	-	178	-	$m\Omega$
$\prod_{i=1}^N \eta_i$	0	0.6	1	
D	0	1/8	1	
V_{LOAD}	-	3.3	-	V
I_{LOAD}	0.001	2	4	A

where V_{IN} is nominal source voltage. The efficiency η_b for a regulated architecture is obtained similarly using Eq. (1):

$$\eta_b = 1 - \frac{R_{LOSSES} \cdot I_{IN}}{V_{IN}}, \quad (4)$$

where I_{IN} is related to I_{LOAD} through the power balance between input and output by means of a second order equation:

$$P_{LOAD} = \prod_{i=1}^N \eta_i \cdot (V_{IN} \cdot I_{IN} - R_{LOSSES} \cdot I_{IN}^2). \quad (5)$$

Solving Eq. (5) for the DC current I_{IN} and replacing its result into Eq. (4), the equivalent efficiency of the regulated system η_b results in the following expression, where the positive solution is the only one with physical meaning.

$$\eta_b = \frac{1}{2} \pm \frac{1}{2} \cdot \sqrt{1 - \frac{4 \cdot R_{LOSSES} \cdot V_{LOAD} \cdot I_{LOAD} \cdot D}{V_{IN}^2 \cdot \prod_{i=1}^N \eta_i}}. \quad (6)$$

In order to obtain real efficiency values, the following term must fulfil the next in-equation:

$$\frac{4 \cdot R_{LOSSES} \cdot V_{LOAD} \cdot I_{LOAD} \cdot D}{V_{IN}^2 \cdot \prod_{i=1}^N \eta_i} \leq 1. \quad (7)$$

Duty cycle and converter equivalent efficiency are the two parameters that provide more information about the effects of discontinuous currents in the efficiency. The reference values used in this study are the nominal values shown in Table II. These values are common in battery powered consumer electronics such as smart-phones. [Traces of Fig. 3 are obtained combining the data of Table II with Eq. \(6\) and Eq. \(7\) and solving the resultant equation with Matlab.](#) Fig. 3(a) shows the efficiency of a regulated architecture vs a direct connection for different values of load duty-cycle (D). Fig. 3(b) shows the aforementioned efficiency comparison for different equivalent efficiencies (η_i) of the regulated architecture. Both set of traces (Fig. 3) highlight how the efficiency converges to zero in the limit when Eq. (7) tends to one. The minimum requirements that a regulated architecture should meet to obtain the same efficiency performance as the direct connection are defined in Fig. 3 (with the intersection of the regulated architecture efficiency traces and the direct connection efficiency base line).

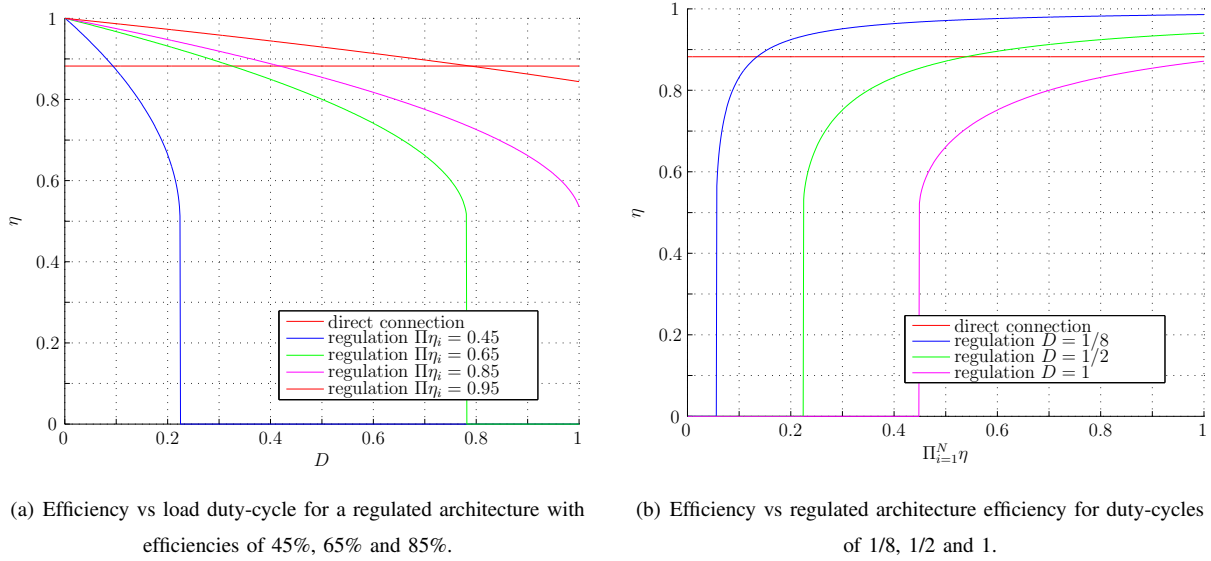


Fig. 3. Direct connexion vs. regulated architecture efficiency.

III. SIMULATION RESULTS

A direct connection to the load (Fig. 4(a)) and the generic COVAIC architecture with switched regulators (Fig. 4(b)) are compared for the test conditions specified in Table II. **Simulations have been carried out using PSpice and KeySight ADS simulation software.**

Fig. 4(a) shows the Spice structural model of a direct connection. This model is made of an equivalent circuit of a Lithium-Ion battery with nominal voltage of 3.6 V and a discontinuous load model. The battery is represented with a DC voltage source and an equivalent series resistance. These resistances are the internal resistance of the battery, the distributed resistance of the PCB tracks and connectors, the series resistance of the fuse and the ON resistance of the MOSFET that constitute the battery protection circuit [19].

The switched COVAIC architecture model is represented in Fig. 4(b) [7]. It uses the same battery and load structural models of Fig. 4(a). The circuit of Fig. 4(b) includes the structural model of a capacitor that the COVAIC architecture requires. The two switched regulators are implemented with generic behavioural models [9], [23]. Each regulator has an efficiency of 80%, which implies that each have an equivalent efficiency of 65%. The adaptive input current operation mode of the model is obtained through an adaptive control loop [24]. This loop sets the input current limit of the architecture input regulator to the average power that the load demands in each cycle of the pulsed load.

The traces of Fig. 5 provide the tuning parameters and the conditions that the COVAIC architecture should meet to have the same or better efficiency figures than the direct connection. In Fig. 5 the equivalent efficiency of the regulated architecture is compared with the efficiency of a direct connection in the same conditions. The efficiency data is presented in Fig. 5(a) as a function of the load duty-cycle. Fig. 5(a) compares the efficiency of the COVAIC architecture with the direct connection as a function of the load duty-cycle for equivalent efficiencies of 45%,

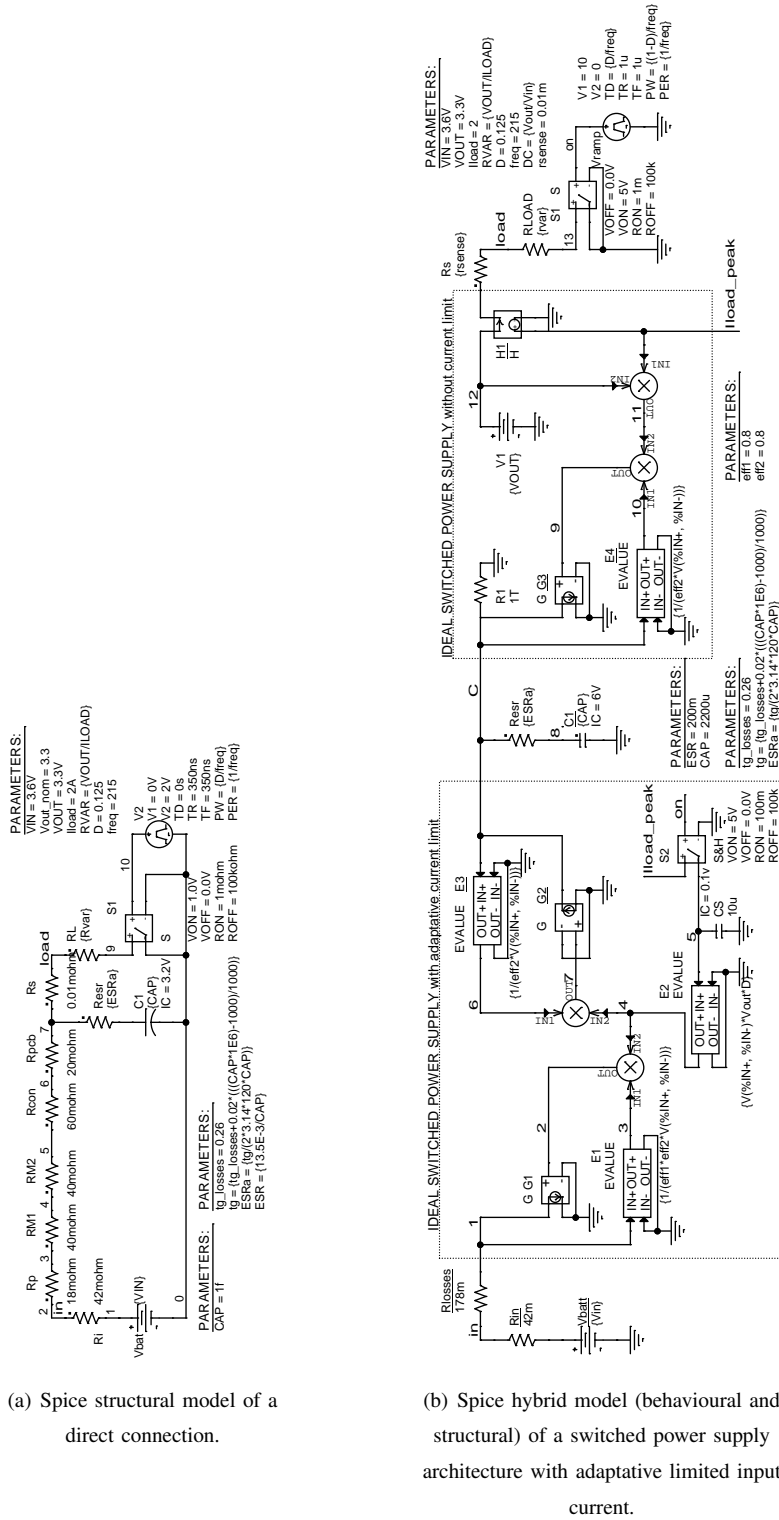


Fig. 4. Structural and behavioural schematics of the direct connection and the switched COVAIC architecture to connect a Lithium-Ion battery to a pulsed load.

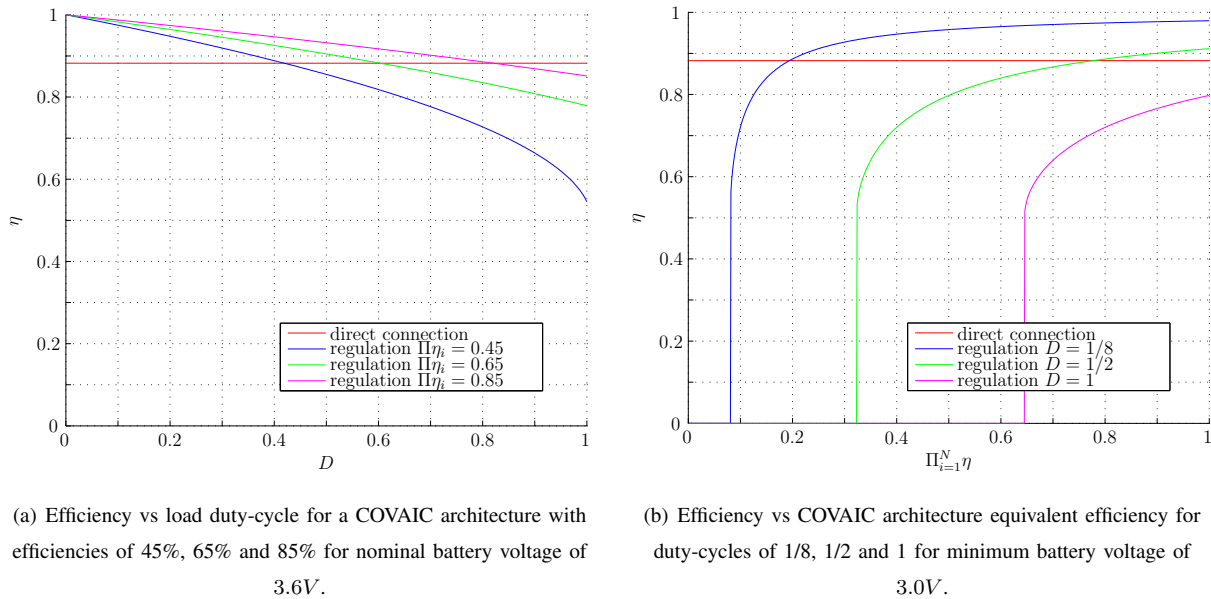


Fig. 5. Direct connexion vs. COVAIC efficiency.

65% and 85% with the direct connection efficiency. Similarly, Fig. 5(b) compares the efficiency of both alternatives for load duty-cycles of 1/8, 1/2 and 1. Taking the duty-cycle value of 1/8 used in Fig. 4(b), Fig. 5(a) traces state that the regulated architecture requires an equivalent efficiency better than approximately 40%. With this value of minimum equivalent efficiency, both alternatives have the same efficiency. The performance of the direct connection and the COVAIC architecture are compared in Fig. 6 for these conditions. Fig. 6 verifies the performance of the two architectures through the efficiency figure, the load power, and the voltage and current waveforms at the load and the input for battery voltages minimum, nominal and maximum. The results show that Fig. 5 provides an accurate value of equivalent efficiency because the COVAIC architecture has the same efficiency (Fig. 6(b)) as the direct connection (Fig. 6(a)). Moreover, the results verify that the COVAIC architecture suppress the input current ripple (Fig. 6(l)). The direct connection has a current ripple equal to the one at the load (Fig. 6(k)). Furthermore, the COVAIC architecture does not show load voltage ripple (Fig. 6(f)), which also remains constant, independently of the battery voltage level.

On the contrary, the direct connection has voltage ripple at the load terminals and the voltage level depends of the battery voltage (Fig. 6(f)). Finally, the regulated architecture, unlike the direct connection, maintains the load power constant (Fig. 6(d)) with independence of the load current (Fig. 6(i)) and the input voltage (Fig. 6(h)).

Table III extend the results to all the architectures shown in Fig. 1. They compare the different architectures for the same pulsed load and in the nominal test conditions stated on Table II. Table III shows that to reduce the input ripple it is required a capacitor connected to the load, and the magnitude of the input voltage ripple is a direct function of the capacitance. To reduce the input current ripple it is required a DC-DC converter. The first two architectures with voltage converters have a input current ripple that is always the rms of the load current, but it is

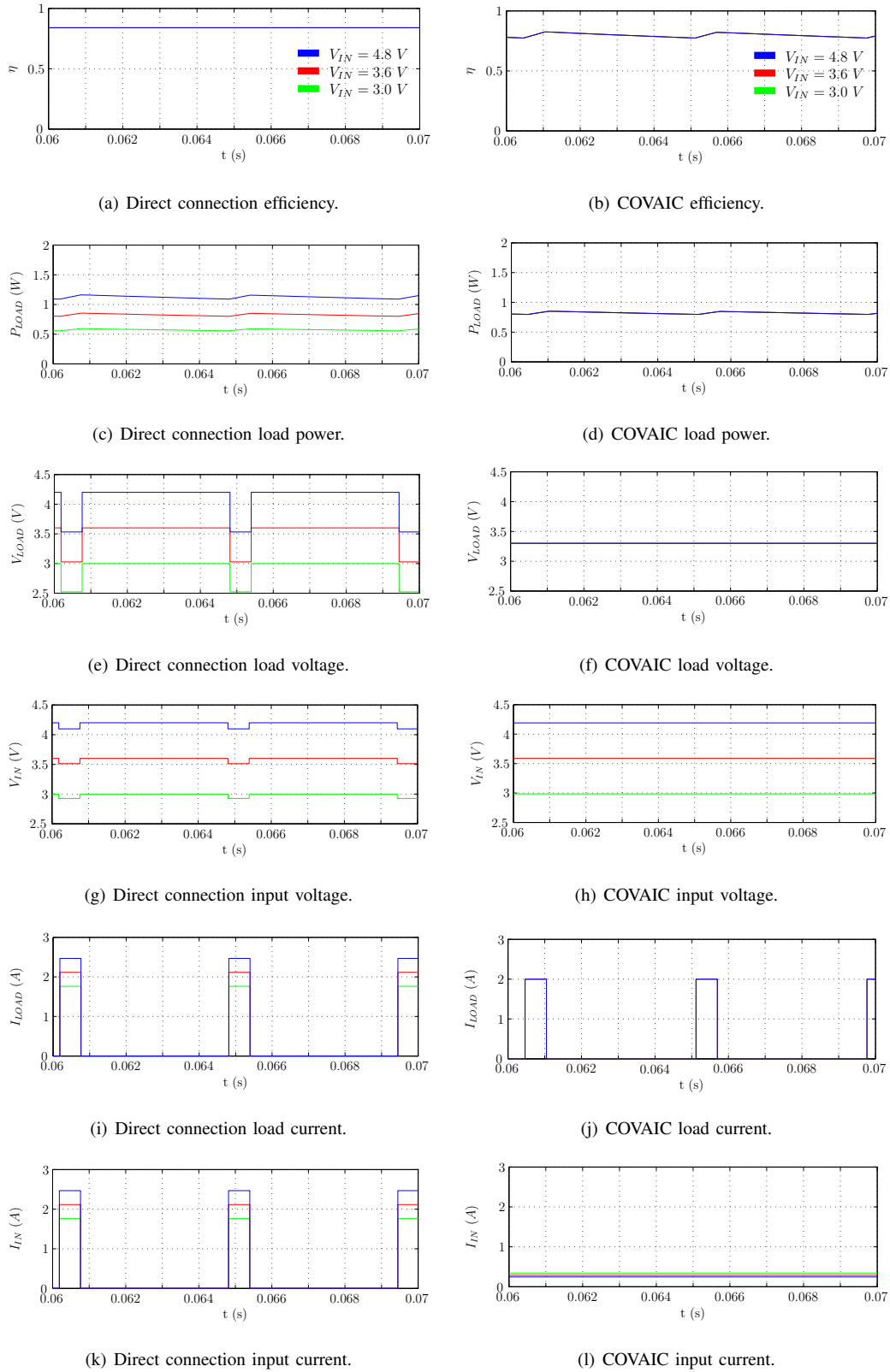
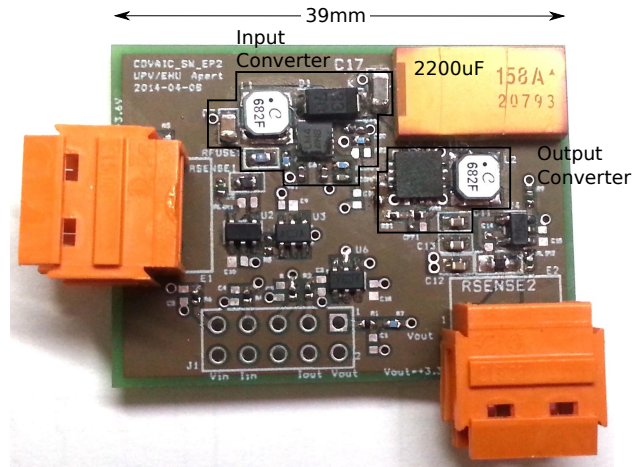


Fig. 6. Efficiency, load power, and voltage and current waveforms at the load and the input for a Lithium-Ion battery at minimum, nominal and maximum voltage.



(a) COVAIC switched regulator prototype.

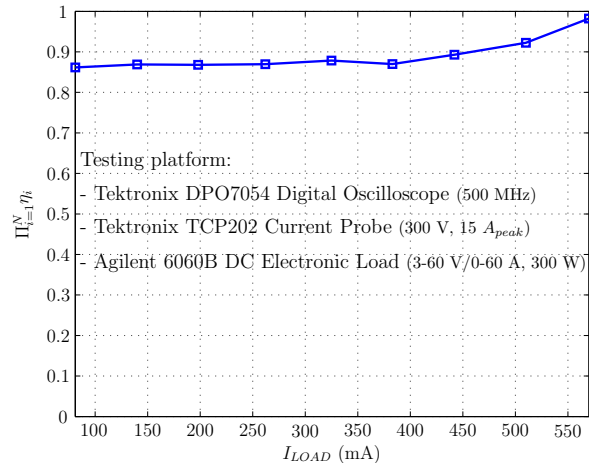
(b) COVAIC switched regulator prototype η vs. I_{LOAD} .

Fig. 7. Picture of the COVAIC switched regulator prototype ($V_{IN} = 3.6V$, $V_{LOAD} = 3.3V$, $I_{LOADmax\ rms} = 350mA$, $I_{LOAD\ peak\ max.} = 1A$) and its efficiency performance.

necessary employ the COVAIC architecture to completely suppress this ripple. Concerning the load voltage ripple, it is suppressed with a double regulated architecture like the Constant Output Voltage and the COVAIC. Finally the efficiency results confirms mathematical and simulation results, i.e., converter architectures have the same or higher efficiency than a direct connection and better performance.

IV. EXPERIMENTAL RESULTS

The COVAIC test platform shown in figure Fig. 7(a) has been designed and built in order to validate experimentally simulation and analytical results. The prototype includes two commercial switched regulator made of discrete components ADP1614 and TPS62110 (Fig. 7(a)). It also includes additional electronics for data acquisition of voltage and current, which are used for programming the adaptive loop on external systems. Table IV summarizes the prototype parameter range and test conditions. Both switched converters have a high switching frequency of $6MHz$. They also include PWM and PFM control mode together with a skip mode functionality that provides low quiescent current and, consequently, good efficiency without the presence of a load.

The total efficiency of the architecture ($\Pi_{i=1}^N \eta_i$) is show on Fig. 7(b) as a function of the load current. The efficiency has been obtained through the current and voltage mean values measured with the test platform specified in Fig. 7(b). The efficiency measurements have been introduced on Fig. 5(a) and Fig. 5(b) in order to compare the prototype performance against a direct connection to the power source. This allows to identify in which operation conditions the prototype presents a better performance. Table V provides a comparison between the theoretical performance of the behavioural model and the prototype. The prototype input current ripple is due to the skip mode functionality of the switched controllers employed and the control loop dynamic response. The aforementioned ripple could be improved increasing the capacitor value, reducing the capacitor ESR and/or slowing the response

TABLE III

COMPARISON OF POWER SUPPLY ARCHITECTURES FOR A PULSED LOAD CONNECTED TO A LITHIUM-ION BATTERY ($V_{IN} = 3.6 V$, $V_{LOAD} = 3.3 V$, $I_{LOAD} = 2 A$, $1/8$ OF DUTY-CYCLE AND CONVERTERS $\eta_i = 0.8\%$.)

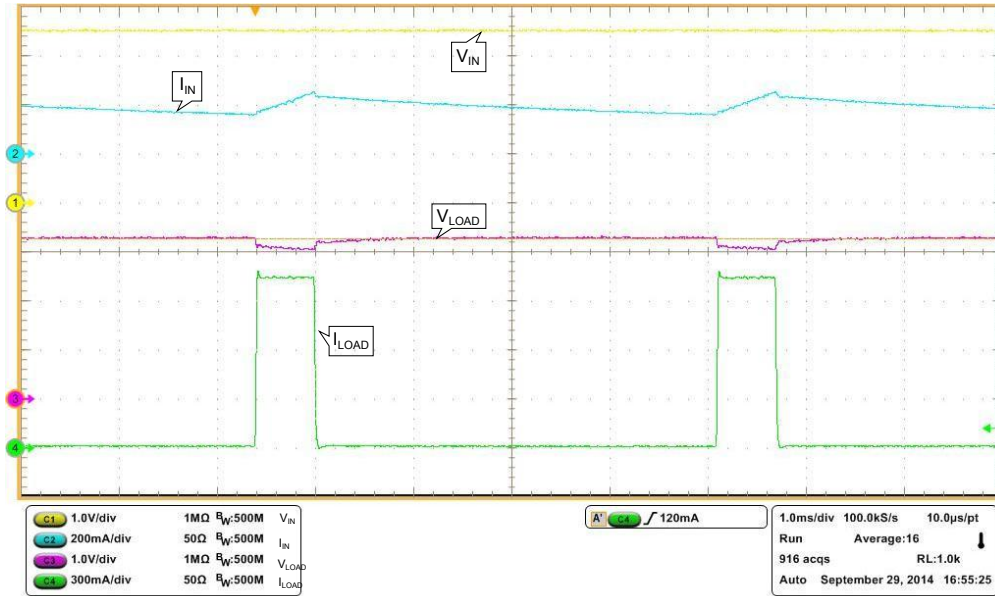
Parameter	Direct connection	Passive components		Voltage converters		
		<i>C in the load</i>	<i>LC network</i>	<i>Const. I limit</i>	<i>Const. Output V</i>	<i>COVAIC</i>
C_1	-	4700 μF	470 μF	4700 μF	4700 μF	4700 μF
L_1	-	-	100 μH	-	-	-
V_{IN} ripple	80.8 mV	12 mV	2.63 V	12 mV	12 mV	0 V
I_{IN} ripple	1.924 A	1.237 A	2.648 A	0.291 A	0.366 A	0 A
V_{LOAD} ripple	423.3 mV	276.7 mV	1278 mV	375. mV	30 mV	30 mV
I_{IN} Undercurrent	0 V	0 V	-642.5 mA	0 V	0 V	0 V
Efficiency	88.1%	85.4%	77.8%	98.8%	97.7%	97.7%
EMC	Poor	Average	Poor	Average	Average	Average
Size	$\simeq 0 \text{ mm}^2$	$\simeq 2.25 \text{ mm}^2$	$\simeq 3.25 \text{ mm}^2$	$\simeq 2.95 \text{ mm}^2$	$\simeq 2.95 \text{ mm}^2$	$\simeq 3.37 \text{ mm}^2$
$I_{IN}(t = 0)$ overcurrent	$\simeq 0 A$	$\simeq 10A$	-	-	-	-

of the adaptive control loop. A load voltage ripple caused by the equivalent series resistance of the inductor, output current sense resistance, PCB and connectors is also noticeable.

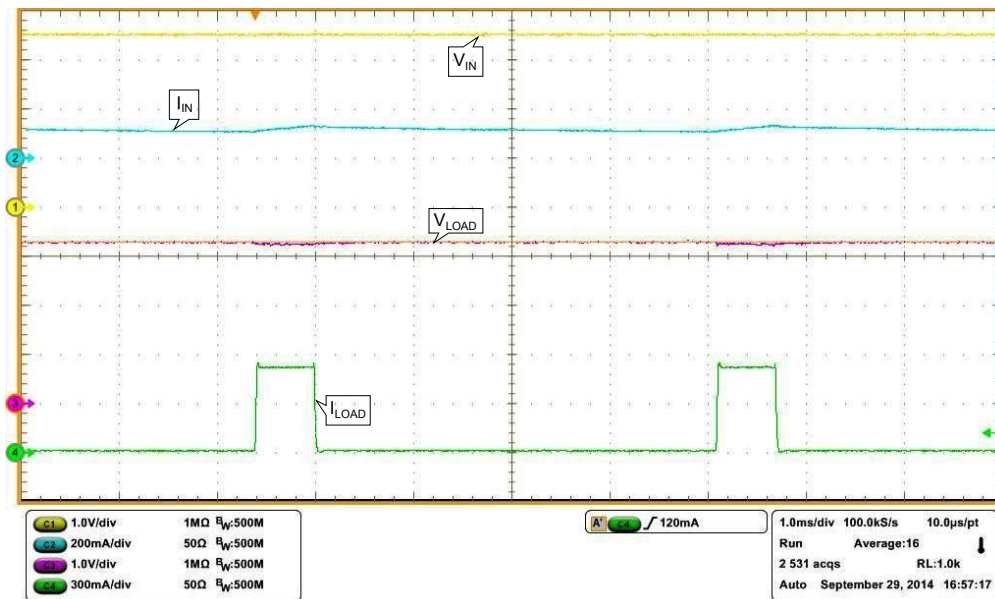
Table V provides the capacitor voltage ripple. This ripple is function of the capacitor value, its ESR and the load current. On the other hand, Table VI compares the prototype and the direct connection. Its input and output current and voltage waveforms in normal test conditions for different levels of load are show in the oscilloscope captures of Fig. 8. Figs. 8(a) and 8(b) show the voltage and current waveforms of the prototype at 1A and 0.5A, respectively. It is important to note that the input current waveform of Fig. 8(a) has the same shape of the prototypes load power (Fig. 6(d)), which guaranties that the mathematical model is valid and the prototype works as expected.

V. CONCLUSION

This work analyzes the effects of a pulsed load on the performance of an electronic system and its power source. The paper presents the most relevant architectures that could be used to power a discontinuous load. They are classified according to their electrical and EMC performance, and characteristics. The article also analysis mathematically the performance of each architecture from the perspective of green electronics, i.e., its efficiency. The aforementioned analysis provides the tools to configure the parameter of power supply DC-DC architectures for pulsed loads in order to achieve the same efficiency figures of a direct connection. Simulation and measurement results certify that the mathematical expression are accurate. They state that the architectures with DC-DC regulators have better performance than a direct connection and they could also have the same or higher efficiency. Finally,



(a) Voltage and current waveforms for $I_{LOAD} = 1A$.



(b) Voltage and current waveforms for $I_{LOAD} = 500mA$.

Fig. 8. COVAIC input and load current and voltage waveforms at nominal voltage $V_{in} = 3.6V$ and 1/8 duty cycle.

the models include in the article provide tools to characterized the performance of power supply architectures with discontinuous load and, at the same time, configure them to achieve the same efficiency figures of a direct connection to the load.

TABLE IV
COVAIC PROTOTYPE PARAMETER RATINGS

Parameter	Value			Units
	<i>min.</i>	<i>nom.</i>	<i>max.</i>	
V_{IN}	3.0	3.6	4.2	V
$\prod_{i=1}^N \eta_i$	0.86	0.88	1	
D	0	1/8	1	
V_{LOAD}	-	3.3	-	V
I_{LOAD}	0.001	0.5	1	A
$I_{LOAD \text{ mean}}$	0.01	250	450	mA

TABLE V
COVAIC SIMULATION MODEL vs PROTOTYPE VOLTAGE AND CURRENTS WITH A SHUNT CAPACITOR OF 2200 μF AND NOMINAL INPUT VOLTAGE $V_{IN} = 3.6V$.

Parameter	$I_{LOAD} = 0.25 \text{ A}$		$I_{LOAD} = 0.5 \text{ A}$		$I_{LOAD} = 0.75 \text{ A}$		$I_{LOAD} = 1 \text{ A}$		Unit
	Model	Prototype	Model	Prototype	Model	Prototype	Model	Prototype	
$I_{IN \text{ mean}}$	44.8	85	88.7	118.8	135.3	158.9	180.4	196.3	mA
$I_{IN \text{ ripple}}$	0.12	5	0.25	15	0.4	35	0.6	75	mA
$V_C \text{ ripple}$	34.2	153.2	68.4	308.3	105.4	410.5	142.5	540.5	mV
$V_{LOAD \text{ ripple}}$	0	5	0	40	0	80	0	120	mV
V_{LOAD}	3.3	3.299	3.3	3.295	3.3	3.29	3.3	3.268	V

TABLE VI
DIRECT CONNECTION vs COVAIC PROTOTYPE VOLTAGE AND CURRENTS WITH A SHUNT CAPACITOR OF 2200 μF AND NOMINAL INPUT VOLTAGE $V_{IN} = 3.6V$.

Parameter	$I_{LOAD} = 0.25 \text{ A}$		$I_{LOAD} = 0.5 \text{ A}$		$I_{LOAD} = 0.75 \text{ A}$		$I_{LOAD} = 1 \text{ A}$		Unit
	Dir. Conn.	Prototype	Dir. Conn.	Prototype	Dir. Conn.	Prototype	Dir. Conn.	Prototype	
$V_{IN \text{ ripple}}$	62.1	0	44	0	140	0	160	0	mV
$I_{IN \text{ mean}}$	62.1	85	91.9	118.8	121.8	158.9	158	196.3	mA
$I_{IN \text{ ripple}}$	0.264	0.05	0.522	0.015	0.774	0.35	1.038	0.075	A
$V_{LOAD \text{ ripple}}$	80	5	154	55	230	100	340	180	mV
V_{LOAD}	3.52	3.299	3.42	3.295	3.36	3.29	3.26	3.268	V

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REFERENCES

- [1] K. Kankanamge and N. Kularatna. 'Improving the End-to-End Efficiency of DC-DC Converters Based on a Supercapacitor-Assisted Low-Dropout Regulator Technique'. *IEEE Transactions on Industrial Electronics*, 61(1):223-230, January 2014.
- [2] B. Sahu and G.A. Rincon-Mora. 'An Accurate, Low-Voltage, CMOS Switching Power Supply With Adaptive On-Time Pulse-Frequency Modulation (PFM) Control'. *IEEE Transactions on Circuits and Systems*, 52(2):312-321, 2007.
- [3] J. Balcells, A. Santolaria, D. Orlandi, A. Gonzalez, and J. Gago. 'EMI Reduction in Switched Power Converters Using Frequency Modulation Techniques'. *IEEE Tran. on Electromagnetic Compatibility*, 47(3): 569-576, 2005.
- [4] N. Kularatna, J. Fernando, K. Kankanamge and L. Tilakaratna. 'Very low frequency supercapacitor techniques to improve the end-to-end efficiency of DC-DC converters based on commercial off the shelf LDOs'. In *IEEE Conf. Proc. Industrial Electronics (IECON)*, pages 721-726, 2010.
- [5] U.R. Prasanna, A.K. Rathore, and S.K. Mazumder. 'Novel Zero-Current-Switching Current-Fed Half-Bridge Isolated DC/DC Converter for Fuel-Cell-Based Applications'. *IEEE Transactions on Industry Applications*, 49(4):1658-1669, 2010.
- [6] D. Satou, N. Hoshi, and J. Haruna. 'Characteristics of cell voltage equalization circuit using LC series circuit in charging and discharging states'. In *Proc. of the Industrial Electronics Society Conference (IECON)*, pages 514-519, 2013.
- [7] J.M. de Diego and J.I. Garate. 'System for eliminating current surges in electronic system and equipment having intermittent current consumption'. Spain Patent 2372084 (2012). U.S. Application Patent 20027005 (2013).
- [8] V. Gupta, G.A. Rincon-Mora, and P. Raha. 'Analysis and design of monolithic, high PSR, linear regulators for SoC applications'. In *Proc. of the IEEE International SoC Conference*, pages 311-315, 2004.
- [9] C. P. Basso. 'Switch-Mode Power Supplies: SPICE Simulations and Practical Designs'. Ed. McGraw-Hill, New York, 2008.
- [10] Z.H. Shen and H. Min. 'Combination method of DC-DC converter and LDO to improve efficiency and load regulation'. *Electronics Letters*, 12(10):615-617, 2011.
- [11] C. K. Tse. 'Circuit Theory of Power Factor Correction in Switching Converters'. *International Journal of Circuit Theory and Applications*, 31(2):157-198, March 2003.
- [12] C. K. Tse, M. H. L. Chow and M. K. H. Cheung. 'A Family of PFC Voltage Regulator Configurations with Reduced Redundant Power Processing'. *IEEE Transactions on Power Electronics*, 16(6):794-802, November 2001.
- [13] Reza Forooshfar, Ehsan Adib and Hosein Farzanehfard. 'New single-stage, single-switch, soft-switching three-phase SEPIC and Cuk-type power factor correction converters'. *IET Power Electronics*, 7(7):1878-1885, 2014.
- [14] B. Aksanli, T.S. Rosing, and I. Monga. 'Benefits of green energy and proportionality in high speed wide area networks connecting data centers'. In *Proc. of the Design, Automation and Test in Europe Conference and Exhibition (DATE)*, pages 175-180, 2012.
- [15] J.R. Miller and D.M. Ryan. 'Power System Optimization Using Energy Storage'. In *IEEE Proc. of Energy Tech*, pages 1-6, 2011.
- [16] V. Yousefzadeh, E. Alarcon, and D. Maksimovic. 'Efficiency optimization in linear-assisted switching power converters for envelope tracking in RF power amplifiers'. In *Proc. of the International Symposium on Circuits and Systems*, 2: pages 1302-1305, 2005.
- [17] A. Lindiyaa, S. Palani and Iyyappana. 'Performance Comparison of Various Controllers for (DC-DC) Synchronous Buck Converter'. *Procedia Engineering*, 38: 2679-2693, 2012.
- [18] R.B. Sepe, A. Steyerl and S.P. Bastien. 'Lithium-ion supercapacitors for pulsed power applications'. In *IEEE Proc. of the Energy Conversion Congress and Exposition*, : pages 1813 – 1818, 2011.
- [19] B. Scrosati and J. Garche. 'Lithium batteries: Status, prospects and future'. *Journal of Power Sources*, 195: 2419-2430, 2010.
- [20] F.I. Simjee and P.H. Chou. 'Efficient Charging of Supercapacitors for Extended Lifetime of Wireless Sensor Nodes'. *IEEE Tran. on Power Electronics (ECCE)*, 23(3): 1526-1536, 2008.
- [21] T. Hirai, A. Ohnishi, N. Nagaoka, N. Mori, A. Ametani and S. Umeda. 'Automatic Equivalent-Circuit Estimation System for Lithium-Ion Battery'. In *Proc. of the International Universities Power Engineering Conference (UPEC)*, pages 1-5 , 2008.
- [22] Zeljko Ivanovic Branko Blanusa and Mladen Knezic. 'Analytical power losses model of boost rectifier'. *IET Power Electronics*, 7(8):2093-2102, 2014.
- [23] C. Shetty, A. Kadle and A.B. Raju. 'A simplified approach to the first order approximations of a closed loop, non isolated dc-dc converter with synchronous rectifier circuit behavior by using the ORCAD PSPICE'. *Fifth International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom 2013)*, pages 309 - 318, 2013.

- [24] Sucheng Liu, Luowei Zhou and Weiguo Lu 'Simple analytical approach to predict large-signal stability region of a closed-loop boost DC/DC converter'. IET Power Electronics, 6(3):488-494, 2014.
- [25] Linlin Gu, Xinbo Ruan, Ming Xu and Kai Yao 'Means of Eliminating Electrolytic Capacitor in AC/DC Power Supplies for LED Lightings'. IEEE Transactions on Power Electronics, 24(5):1399, may 2005.