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Rapid Control Prototyping platform to regulate a high-current low-voltage DC/DC power converter prototype to feed superconducting electromagnets

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***Abstract*— Superconducting electromagnets are key components in modern scientific particle accelerators. For example, among other tasks, they are used to focus particle beams in the collision points. Their magnetic field needs to be precisely controlled by regulating the power electronics that feed such magnets. This work discusses the most relevant aspects regarding the digital implementation of an FPGA-based Rapid Control Prototyping (RCP) platform intended to regulate a high-current low-voltage two-quadrant Series Capacitor (SC) DC/DC power converter prototype. This converter has been developed to study the powering of the Inner Triplet (IT) superconducting electromagnets of the High Luminosity (HL) upgrade of the Large Hadron Collider (LHC) at CERN. The design guidelines, based on the well-known Model Based Design (MBD) approach, are highlighted, and implementation details are provided. Experimental results that show the correct operation of the RCP platform are finally presented.**

***Index Terms*— Keywords - Large Hadron Collider, Series Capacitor converter, DC/DC converter, Rapid Control Prototyping**

I. Introduction

The Large Hadron Collider (LHC) at CERN is the biggest and most powerful particle accelerator currently in operation [1]. Hadron (proton) and heavy ion beams are accelerated to 7 TeV to produce particle collisions. The detection and analysis of the resultant particles at the collision points provides valuable information for scientists to further the understanding of the standard model of particle physics [2], [3].

A major upgrade, named High Luminosity (HL)-LHC, is being carried out at CERN to increase the luminosity (L) or rate-of-collisions of the accelerator by a factor of five [4]. Current quadrupole Inner Triplet (IT) electromagnets will be substituted by more powerful large aperture Nb_3Sn ones [5]. From an electrical point of view, these electromagnets behave as inductive loads (L_{mag}). The wiring resistance (R_w) is very low, as a superconducting link is used instead of copper busbars. The magnetic field is controlled by regulating the current circulating throughout the magnets. In this context, power electronics play a relevant role for supplying energy to these electromagnets [6]–[10].

From late 2019 to mid 2022, the Applied Electronics Research Team (APERT) of the University of the Basque Country (UPV/EHU) worked with the Accelerator Systems Department (SY) of CERN within the project *"Collaboration in the Study of Power Converter Topologies for Inner Triplet magnets with Energy Recovery in the framework of the High Luminosity upgrade for the LHC at CERN"*. Within the scope of this project, a $[\pm 10\ V,\ 1000\ A]$ two-quadrant interleaved DC/DC power converter prototype unit has been developed, tested and validated. In addition, a novel digital control approach has been proposed for the converter [10]. This work discusses and provides details about the digital implementation of the proposed control solution. The controller does not only include the closed-loop regulation and PWM algorithms themselves, but it also needs to incorporate a number of features such as a state machine that governs the high-level operation of the converter, diagnosis and alarm blocks, data conditioning, etc.

During the APERT/CERN collaboration, a Rapid Control Prototyping (RCP) approach has been followed to implement the controller, as the industrialization of the control system has not been a target during the realization of the project. According to [11], the term RCP defines a set-up or phase of real-time simulation in which a re-programmable controller is used for the fast development of a control algorithm without worrying about writing code (automatic code generation tools avoid possible errors generated during hand coding). Following the Model Based Design (MBD) approach and relying on the well-known V-Cycle for controller testing, the development time is significantly reduced [12], [13]. By definition, the MBD approach uses a system model as an executable specification throughout development. This working paradigm supports system- and component-level design and simulation, automatic code (or VHDL) generation, and continuous testing and verification [14].

Regarding the physical digital real-time platform used to implement the controller of the power converter prototype, an OPAL-RT OP4200 RCP device has been selected [15]. This XilinX ZynQ (XC7Z030)-based RCP device allows to take advantage of the fast response of its FPGA to meet the requirements of the control algorithm. In addition, its cassette-based architecture makes it possible to scale the type and number of I/Os, tailoring the physical controller to the application. As previously stated, both CPU and FPGA firmwares integrated in the OP4200 device have been developed by following a model based approach.

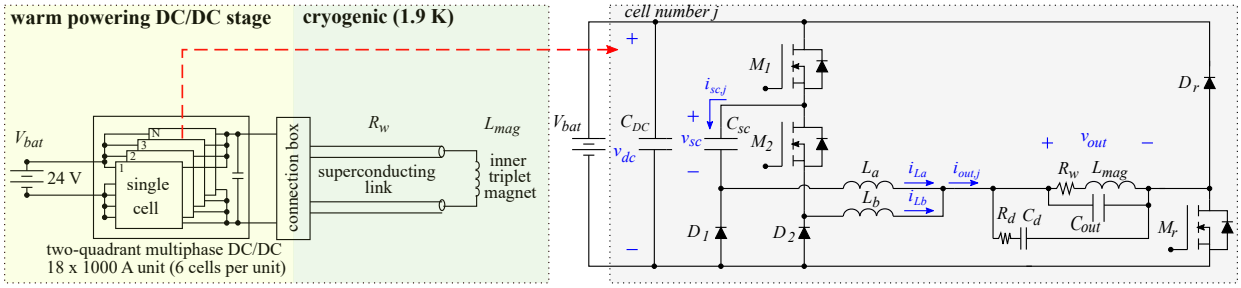
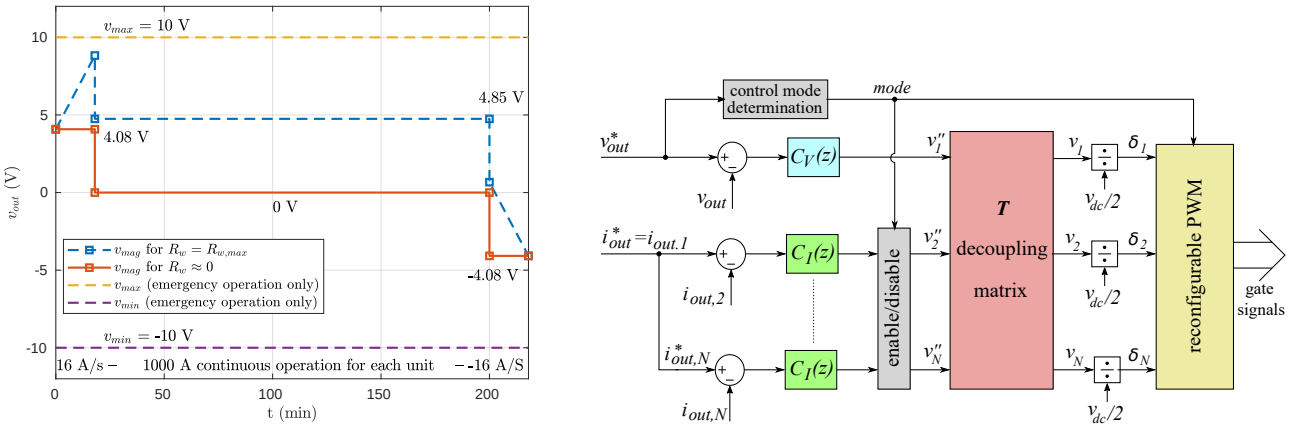


Fig. 1: Proposed two-quadrant DC/DC power converter, constituted by 6 series capacitor architecture based cells.



(a) Operation profiles of the power converter.

(b) Simplified closed-loop control and modulation block diagram.

Fig. 2: Power converter operation profiles and control algorithm block diagram.

In the following, operation and control principles of the developed power converter are first explained, and the most relevant RCP implementation details are discussed. Finally, experimental results that show the correctness of the digital implementation of the RCP platform are shown, and a number of conclusions are outlined.

II. Operation and Control Principles of the High-Current Low-Voltage DC/DC Converter

Figure 1 shows the general diagram of the developed $[\pm 10\ V,\ 1000\ A]$ power converter unit. The converter must provide positive or negative output voltages to regulate the current (and magnetic field) of the electromagnet (figure 2(a)). The proposed unit is composed of six paralleled two-quadrant DC/DC converter cells, each rated at 166 A and connected to a 24 V battery pack at the input side. This modular approach provides fault tolerance to the system with minimum control reconfiguration requirements in many cases.

The buck stage of the proposed architecture is based on the series capacitor (SC) converter [16], [17] (figure 1, switches M_1, M_2, D_1, D_2, inductors L_a, L_b and capacitor C_{out}). The SC buck has been selected as the operation of the converter under high step-down conditions is improved in terms of output voltage ripple and efficiency [10]. On the other hand, the M_r switches provide regenerative (fourth quadrant) operation capabilities (positive output current, negative output voltage), reducing the time to de-energize the magnet (note that, as busbar resistance R_w is low, de-energizing L_{mag} by free-wheeling requires an excessive amount of time). The damping net R_d, C_d is optional, and can be incorporated at the output side of each cell to avoid possible resonances around the switching frequency [10].

Regarding the control algorithm, an accurate high-level controller determines the reference voltage v^*_{out} to be applied by the power converter to track a given magnet current profile during operation [18]. This high-level controller has ppm-level requirements for magnet current regulation. Then, the proposed closed-loop control diagram (figure 2(b)) regulates the output voltage v_{out} of the converter while, in buck mode, it also balances the currents of all the paralleled cells ($i_{out,j},\ j \in \{2,3,\dots 6\}$) by setting $i^*_{out,j} = i_{out,1}$. This independent control of the output voltage and cell currents is possible thanks to the decoupling matrix $\mathbf{T}$ proposed by the authors in [10]. It is important to note that the mean value of the measured currents can be determined for each modulation period by oversampling. This way, a precise current balancing between cells is achieved. A comprehensive mathematical explanation of the closed-loop controller is provided in [10]. As detailed in the following, the two operation modes, buck and regenerative, require the reconfiguration of the control algorithm and modulation scheme.

A. Buck mode (first quadrant operation)

The buck mode represents more than 97 % of the operation time of the converter, leading to cycles of 10 hours (or more) of continuous operation [10]. For that reason, the proposed

solution has been optimized for the working conditions within the first quadrant.

When the output reference voltage $v^*_{out} > 0$, the multiphase converter is configured to operate as an interleaved DC/DC SC buck converter. To do so, all the return switches M_r remain permanently ON. Each cell MOSFETs M_1 and M_2 are then modulated according to the duty cycle δ_j determined by the closed-loop controller (an independent duty cycle value for each cell to achieve an adequate current balancing). An interleaving of 50 % the modulation period is applied between each M_1 and M_2 MOSFETs when $\delta_j \leq 0.5$, leading to naturally balanced currents through inductors L_a and L_b (figure 3(a)). Furthermore, all j-th cells' switches are interleaved a time period of $t_{d,j}$ with respect to the first cell ones to minimize the output voltage ripple:

$$t_{d,j} = \frac{(j-1)}{2N} T_s, \; j = \{2, 3 \cdots N\}, \tag{1}$$

where T_s is the modulation period and, in particular, $N = 6$ for the developed power converter prototype.

Although in normal operation $\delta_j \leq 0.5$, the power converter should provide output voltages up to $+10\ V$, leading to values of $\delta_j > 0,5$. In such cases, the inductor currents would become unbalanced if the previously explained modulation pattern is applied. However and by modifying the modulation pattern, i.e., saturating the width of the pulse of M_1 to 50 % the modulation period T_s and extending the pulse of M_2 symmetrically according to the value of δ, it is possible to keep the cells' inductor currents balanced (figure 3(b)) [19].

B. Regenerative mode (fourth quadrant operation)

The regenerative mode is only applied during turn-off and does not have special precision or output voltage ripple requirements. When the commanded reference voltage polarity changes ($v^*_{out} < 0$), the energy stored in the magnet is recovered to the battery by applying negative voltage (fourth quadrant operation). Transistors M_1 and M_2 are deactivated and the system operates without interleaving. All the M_r switches are simultaneously modulated with the complementary of the duty cycle provided by the voltage loop ($1 - \delta_1$). Current regulation loops are deactivated and current balancing relies on the impedance matching between cells (accordingly, hardware elements have been over-dimensioned considering the turn-off phase). An output voltage up to -10 V needs to be provided to increase the ramp-down rate and to shorten the duration of the discharge process.

III. RCP PLATFORM IMPLEMENTATION DETAILS

A. Controller requirements and physical platform selection

The requirements of the control and modulation algorithms (figure 2(b)) need to be taken into account to select an appropriate physical RCP digital platform:

(a) A high sampling frequency (f_s) is required for the voltage and current loops, specially to achieve a good current balancing throughout all the cells. Initially and considering the results obtained from a theoretical analysis and simulations, both controller and PWM frequencies have been set to 50 kHz. However, it is convenient to be able to operate at higher frequencies for future upgrades of the power converter prototype which are currently being investigated.

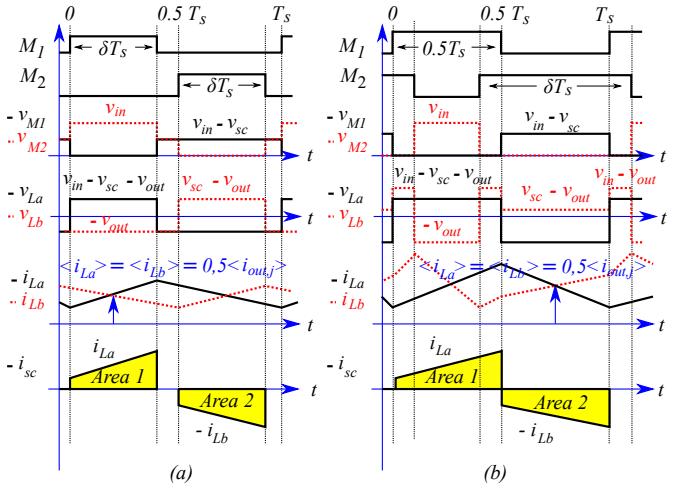


Fig. 3: Modulation algorithms for buck operation mode (adapted from [19]): (a) normal modulation pattern for $\delta \leq 0.5$; (b) extended modulation, providing current balancing for $\delta > 0.5$.

(b) The RCP platform should allow full customization of the modulation algorithm (section II), including interleaving, extended modulation features, programmable dead-times if synchronous diodes are incorporated, etc.

(c) The amount of switching events over a modulation period due to interleaving is high. Thus, it is important to sample the ADCs when no switching occurs to avoid the introduction of noise in the measurements. Thus, synchronization between the ADCs, control loops and modulation blocks is required.

(d) The integration of fast alarms that respond in the order of few μs is convenient to protect the power converter against fault situations that could produce more faults in cascade.

(e) Interleaved cell currents need to be oversampled at double PWM frequency to obtain their mean value over one period and provide a more precise current balancing.

(f) The high precision control requirements of the application (of around 1 ppm for the magnet current) are achieved by the high level controller by utilizing 24 bit ADCs and specialized current probes [20]. Any deviation produced within the power converter is compensated by this high level controller. Thus, it is sufficient to use conventional 16 bit ADCs in the physical controller of the power converter prototype.

All these control requirements make it convenient to use an RCP device with a programmable FPGA. In this context, three RCP platforms are available in the APERT Research Team that meet this criteria: a modular dSPACE, an OPAL-RT OP4510 and an OPAL-RT OP4200 device. The latter was selected for the application as, apart from having a programmable FPGA, it is lightweight and portable, and the number and type of I/Os can be configured through plug-and-play cassettes (figure 4). This way, the number of digital outputs can be tailored for future evolutions over the prototype that could incorporate a higher number of cells and/or synchronous diodes to improve efficiency. Table I summarizes the main hardware characteristics of the OP4200 device. It also provides

TABLE I Main characteristics of the OPAL-RT OP4200 based RCP platform and software used for the MBD implementation of the controller.

RCP platform			OPAL-RT OP4200, based on a XilinX Zynq XC7Z030	**Software tools**
Processor			Dual-core ARM Cortex A9 at 1 GHz	Matlab/Simulink 9.4 (R2018a) with toolboxes:
FPGA			XilinX Kintex 7, 125K LUT	• Stateflow 9.1. (to develop the main state machine)
I/Os	**Analog**	**Inputs**	*Cassette* OP4240-1 16 ch. (simultaneous), 16 bit ADCs, 500 KS/s, ±20 V	• MATLAB Coder 4.0. (for automatic code generation) • Simscape Power Systems 6.9 (system model exec. spec.)
		Outputs	*Cassette* OP4230-1 16 ch., 16 bits, 1 MS/s, ±16 V	XilinX Vivado 2019.1 for DSP • XilinX System Generator (XSG)
	Digital	**Inputs**	*Cassette* OP4250-1 32 ch., 4.5 V to 50 V, 40 ns typical propagation delay	RT-Lab v2019.2.3 • RT-Lab v2019.2.3.176 toolbox • RT-XSG v3.2.6.561 toolbox
		Outputs	*Cassette* OP4260-1 32 ch., 5 V to 30 V, 65 ns typical propagation delay	**Communication protocols**
Dimensions W x D x H (cm)			11,2 x 8,7 x 9,75	CAN bus interface, SFP, RS-232, optical synchro. link
Weight			4,54 kg	USB, JTAG, RJ45 Ethernet port

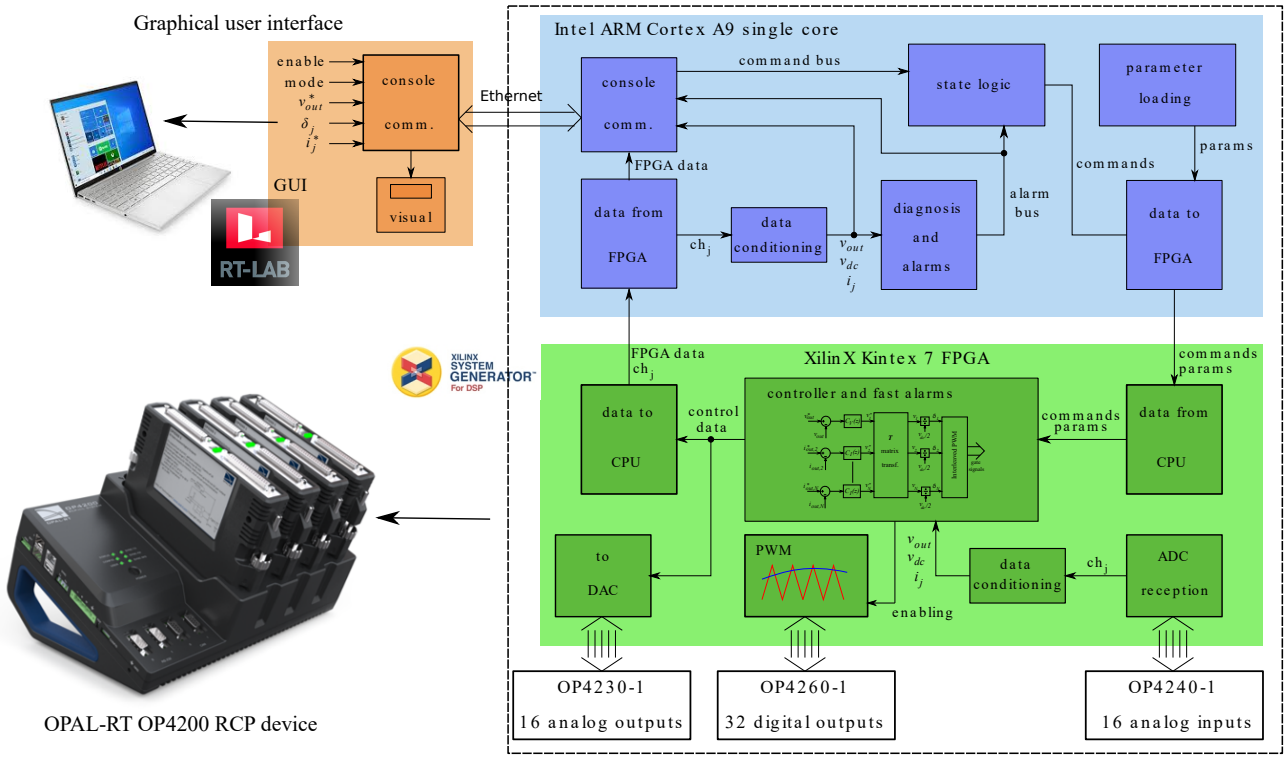


Fig. 4: General diagram of the digital implementation of the power converter controller, highlighting the distribution of the most relevant tasks/subroutines among the CPU core and the FPGA of the OPAL-RT OP4200 device.

details regarding the software used to implement the controller following the MBD approach.

B. Digital implementation details

In order to successfully carry out the digital implementation of the proposed control algorithm, as a first step the capabilities of the OP4200 device regarding the maximum execution frequencies need to be considered [15]:

- The maximum frequency of the control loop implemented in a CPU core is limited to 10 kS/s.
- The maximum frequency of the fast control loop implemented in the FPGA is limited to 1 MS/s.
- The PWM generation within the FPGA can be set to 200 kHz, with a resolution of 5 ns, which perfectly meets the system requirements.

Consequently, the control tasks/subroutines of the controller have been distributed throughout the OP4200 target (FPGA and CPU) and the user interface (remote console) considering the aforementioned frequency constraints (figure 4).

The console or Graphical User Interface (GUI) is executed in a Dell computer connected to the OP4200 device via Ethernet by using the RT-Lab Metacontroller (figure 4). This block sets the control references (v^*_{out} or, eventually i^*_j, $j = \{2, 3\}$, this last option to test the performance of the decoupled controller), the power converter enabling command and the control mode (open-loop or closed-loop operation). Alarm monitoring and resetting, and reception and registering of the most significant waveforms (v_{DC}, v_{out} and i_j, $j = \{1, 3 \dots 6\}$) is also done at the console.

The Intel ARM Cortex A9 includes two cores. The first core incorporates a real-time operative system (*Petalinux*) to manage the communication between the OP4200 and the user interface and synchronize the CPU with the FPGA. In particular, the hardware synchronized mode is used, where the

FPGA acts as a master and synchronizes its execution with the CPU. The second core incorporates the control functionalities that do not require fast execution frequencies (figure 4). This core, mainly implemented with standard Simulink blocks and proprietary OPAL-RT toolboxes, provides communication between the FPGA and the CPU, as well as data conditioning. It also includes the general state machine (developed with the Stateflow toolbox) that governs the high-level operation of the system. Slow frequency alarms are also incorporated for redundancy, and automatic sensor calibration functions are performed during the start-up phase.

The controller parts with high sampling frequency requirements implemented in the FPGA (figure 4) have been also created with MBD tools (XilinX System Generator and RT-XSG toolboxes): I/O management (OP4230-1, OP4260-1 and OP4240-1 boards), signal conditioning and current measurement averaging, fast alarms, DAC (for internal variable debugging), control loops, decoupling matrix and interleaved and reconfigurable PWM module. The synchronization between the constituting blocks (control, modulation, ADCs) can be triggered either from the sawtooth of the PWM modulator of the first cell or from an internal clocking signal generated within the FPGA. This part is fully reconfigurable through a set of parameters sent from the CPU. This way, it is possible to change the number of active cells, the number of active fast alarms and the closed-loop control parameters that set the dynamics. This is one of the main strengths of the implementation, as it avoids the regeneration of the bitstream each time a modification in the controller is required, speeding up the experimental validation of the prototype.

The MBD implementation has followed a previously defined Validation Test Plan (VTP), were each subsystem has been unitarily validated in Simulink prior its incorporation to the whole controller. Then, a system level verification has been carried out in simulation, using an accurate power converter model as system specification. These procedures guaranteed an error free implementation of the algorithm in early development stages. The integration of the whole control system, from the initial idea to its digital implementation, took estimatively four to six person-months. Once virtually validated, the controller was integrated in the experimental platform and was fully operative in a single laboratory session within hours, demonstrating the effectiveness of the approach.

IV. Experimental results

The developed RCP platform has been used during the whole experimental validation stages of the collaboration project. In particular, various physical prototype iterations have been manufactured, where the proof-of-concept versions v1 (June 2021) and v2 (June 2022) can be highlighted. As an example, table II summarizes the main parameters of the latest prototype (v2), while figure 5 shows its physical layout.

As a summary of the multiple results obtained during the project, figure 6 shows the performance of the controller when the power converter operates in buck mode at nominal conditions. The voltage regulation complies with the desired dynamics (no overshoot, settling time $ST_{2\%}$ = 200 ms for v_{out}). The $i_{out,j}$ currents circulating through the six cells that constitute the prototype are kept balanced both in steady state and in transient conditions, as the current regulator dynamics have been set with a faster settling time of 5 ms. Figure 7 provides greater detail regarding the power converter operation. In such test, four cells are active. The currents circulating through the series capacitors of three of the cells ($i_{SC,j}$) have been measured using Rogosky current proves, while the fourth oscilloscope channel shows the total output current of the converter. The output current waveform of each cell can be easily reconstructed from the capacitor currents (see $i_{out,1}$ represented with a dashed black line, figure 7). In particular, this result shows the correct implementation of the interleaved modulation throughout all the active cells.

Finally, it is important to remark that the performance of the power converter prototype has been tested and verified for all the relevant operation conditions, such as the maximum voltage limits and both positive and negative voltage application modes. An efficiency of 85 % has been achieved in buck mode, at nominal conditions. Efficiency was reduced when working within the regenerative mode, but it represents a small amount of operation time of the converter. Including synchronous diodes in future hardware iterations would improve such efficiency results.

TABLE II Main parameters of the experimental platform (proof-of-concept version v2, tested in June 2022).

Power system parameters			
Number of cells (N)	6	Switching freq. (f_{sw})	50 kHz
Controller frequency (f_c)	50 kS/s	Input voltage (V_{bat})	24 V
DC-link capacitor (C_{dc})	100 μF	Series capacitor (C_{sc})	400 μF
Output capacitor (C_{out})	4,7 mF	Per-cell induc. (L_a, L_b)	3,5 μH
Load inductor parameters		**Control parameters**	
Load inductance (L_{load})	50 μH	Voltage $ST_{2\%}{}^{(2)}$	200 ms
Load resistance (R_{load})	1 mΩ	Current $ST^{I}_{2\%}{}^{(2)}$	5 ms

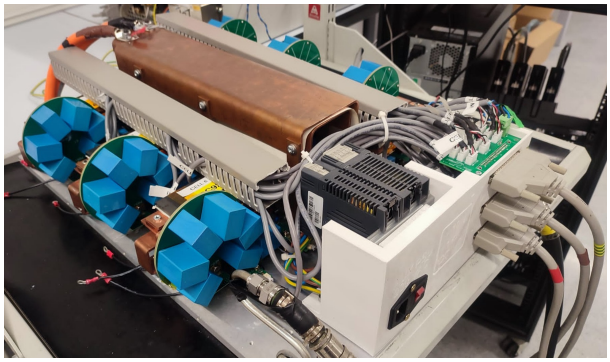
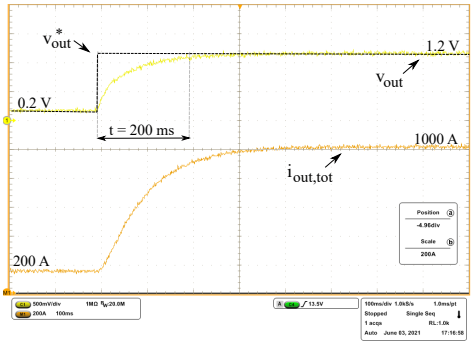


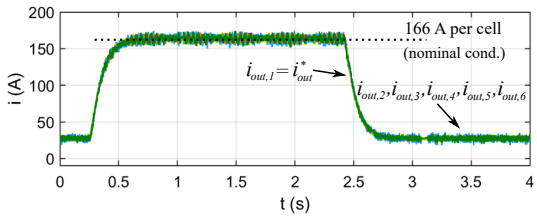
Fig. 5: Prototype proof-of-concept v2 (June 2022).

V. Conclusions

This paper shows the convenience of utilizing a RCP platform to test and develop a high performance power converter prototype during its initial development stages (before the industrialization process). In particular, an FPGA-based real-time device has been required considering the control requirements. Thanks to the automatic code and VHDL generation tools, a model based implementation of the FPGA design has been possible, and no hand coding has been required, simplifying the whole integration process.



(a) Output voltage vs reference voltage for step-up command.



(b) Detail of current balancing through six paralleled cells for both step-up and step-down voltage commands (registered in the OPAL-RT RPC device).

Fig. 6: Experimental results obtained in buck mode for the proof-of-concept v1 prototype of June 2021 at nominal conditions ($ST_{2\%}$ = 200 ms and ζ = 1 for voltage, $ST_{2\%}$ = 5 ms and ζ = 1 for currents), adapted from [10].

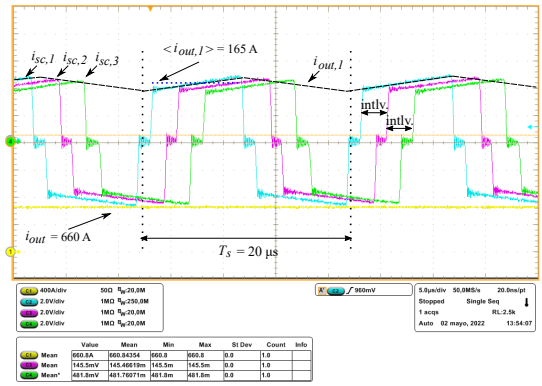


Fig. 7: Detail of the currents circulating through the series capacitors of 3 out of 4 active cells at nominal conditions, measured using Rogosky current proves in the proof-of-concept prototype v2 of June 2022.

The MBD approach and the conducted VTP allowed an in-deep verification of the implemented algorithms. Thanks to this procedure, an error free digital platform has been developed during early design stages, and the incorporation of the digital controller into the experimental platform has been done within hours, demonstrating the strengths of this working paradigm. The obtained experimental results during the whole project have served to validate the proposed control algorithm, the RCP platform and the developed hardware prototypes.

Acknowledgements

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