Loss and stress reduction in VSI devices for EVs using general discontinuous PWM

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***Abstract*—In this paper, a new carrier based discontinuous pulse width modulation (DPWM) strategy for voltage source inverter (VSI) is presented in order to use in electric vehicles (EV). The basic idea of DPWM techniques, is clampimg to upper or lower terminal of DC-link to avoid commutations. Clamping interval of this algorithm is controlled on-line by output current values, to avoid switching with highest current values. The triangular carrier signals are generated as well, depending on output currents to ensure minimum input current ripple. This reduces DC-link capacitor current, and so, reduce stress in capacitor. Switching losses and capacitor current are optimized for whole load angles.**

***Index Terms*—EV, VSI, DPWM, SLF, input current ripple, ICRM-DPWM.**

I. Introduction

The advent of electric vehicles (EV) is gaining research on electric propulsion systems in order to improve efficiency and reliability, being the battery capacity the main bottleneck [1]. Increasing the efficiency of the system, enhances vehicle range and lifetime, so reducing losses and stress of main devices are important issues [2]–[5]. The main power electronic converter, which converts energy from batteries to the three-phase alternating current motor, usually is a voltage source inverter (VSI, figure 1). This converter is well known, robust and simple to control [6]–[8].

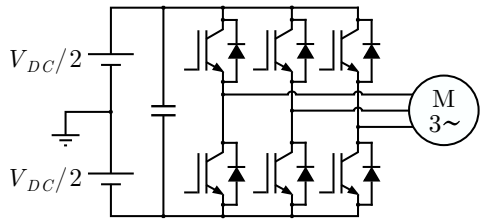
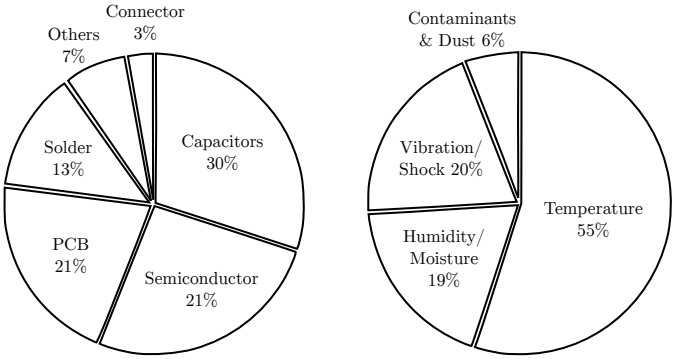


Figure 1. Basic scheme of VSI.

In the other hand, figure 2 shows that most vulnerable elements in a power converter are DC-link capacitor, main switches and pcb, being the main stress source the temperature, which is generated by losses [4], [5], [9]. So loss and stress reduction is a challenging target in converters.

Switches generate heat with conduction losses, leakage current losses and switching losses. Conduction losses and leakage current depend on device technology, but switching losses can be reduced by gate drivers, frequency switching or modulation techniques.



(a) Failure rates. (b) Stress sources.

Figure 2. Distribution of faults and stresses in power converters.

Focusing on modulation methods, discontinuous pulse width mmodulation (DPWM) have been developed. These modulation techniques inject a zero sequence value to all phases in order to clamp a leg to positive or negative link of the DC-bus during a defined interval [4], [8], [10], reducing the number of commutations by 33% in a three phase system [11], [12]. Switching losses depend on clamping intervals and load angle (ϕ), so to reduce for all load angles different methods have been developed, such as general DPWM (GDPWM) [10]. The GDPWM needs to calculate the load angle to modify the modulation indexes. Another method is the digital direct technique GDPWM (DDT-GDPWM) [13], which does not need load angle calculation. It obtains optimal switching loss reduction by clamping the leg which carries highest absolute current. The same method is used by unified dual carrier PWM (Uni-DCPWM) [14]. Other studies have concluded the same with different methods, such as finite control set model predictive control (FCS-MPC) [15], [16].

Mentioned DPWM methods generate modulation waves and are compared with a single triangular carrier wave to produce PWM signals. Using multicarrier waveforms (bicarrier, tricarrier) with DPWM techniques have been demonstrated to have lower DC-link capacitor rms current in certain load angles [11], [14], [17]–[19]. The capacitor rms current reduction with modulation techniques is desirable, because the DC-link capacitor is bulky and one of the weakest devices in an VSI (figure 2(a)) [3], [5], [9], [20], [21].

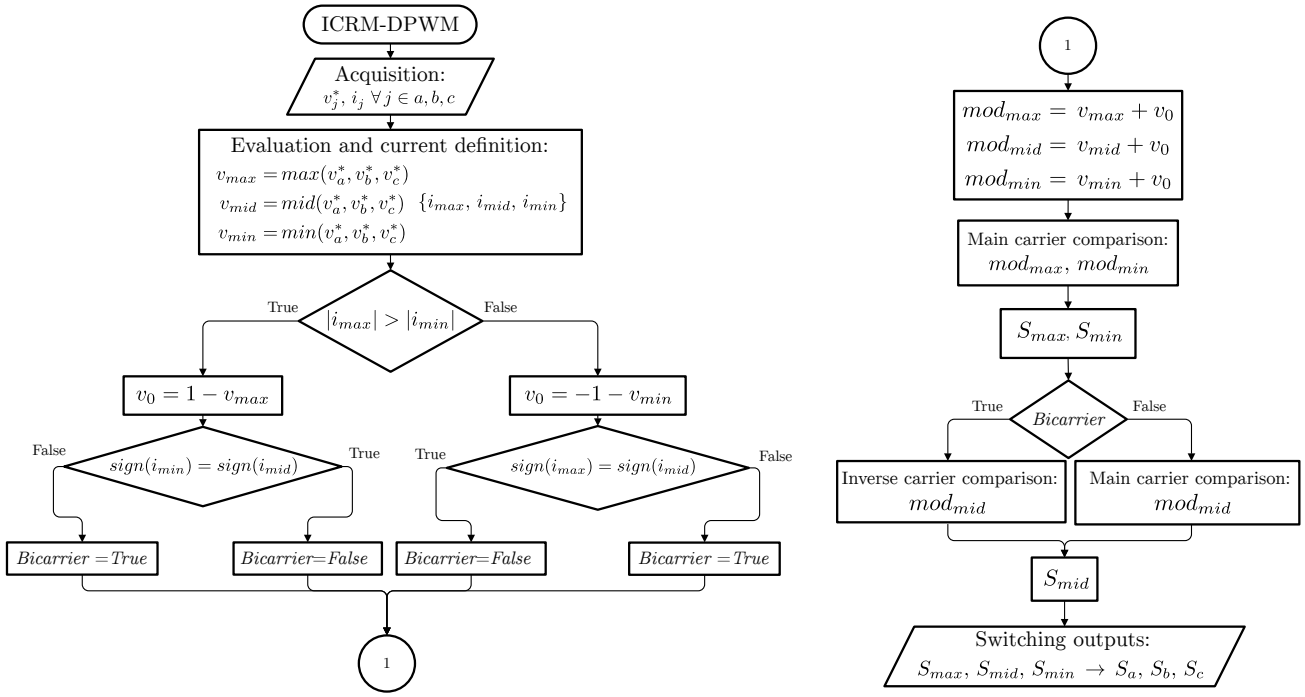


Figure 3. ICRM-DPWM flowchart.

The combination of general DPWM techniques with bicarrier waveform, switching losses still minimized for all load angles, and the DC-link capacitor rms current have been reduced but only for certain load angles. In this paper, an improvement in general DPWM techniques has been obtained: minimal switching losses and DC-link capacitor rms current reduction, both for all load angles. Section II shows the new input current ripple minimization DPWM (ICRM-DPWM) strategy. In Section III, main parameters of DPWM techniques are defined to compare them, and in Section IV experimental results are shown comparing this new technique to SVPWM and other general DPWM techniques.

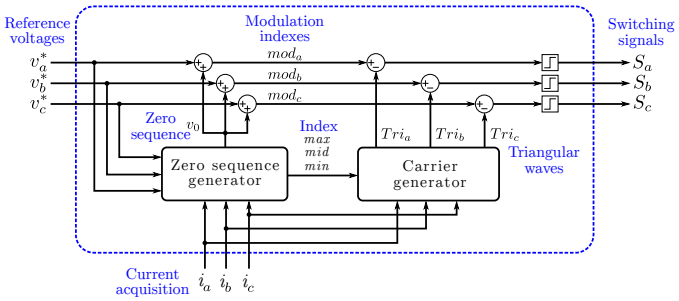


Figure 4. ICRM-DPWM scheme.

II. Input Current Ripple Minimization DPWM

The input current ripple minimization DPWM (ICRM-DPWM) algorithm is a general DPWM method for modulation index modification, combined by a multicarrier (single or bicarrier) selection wave to obtain PWM signals for switching devices. It still gets minimal switching loss, like newest general DPWM techniques, and minimal input current ripple of the inverter, which results in a reduction of DC-link capacitor's rms current. This algorithm operates on-line, analyzing every switching period which technique generates less input current ripple.

The v_0 calculation is determined by modulation indexes and currents of each phase. Firstly, the modulation indexes are sorted from maximum to minimum (v_{max}, v_{mid} and v_{min} in figure 3), and currents are measured and labeled: i.e. i_{max} corresponds to the same phase as v_{max} (i_{max}, i_{mid} and i_{min} in figure 3). If $|i_{max}| > |i_{min}|$, v_0 gets the value to clamp to upper link. Otherwise, it gets the value to clamp to lower link. This generates new modulation waveforms by adding v_0 to modulation indexes (mod_{max}, mod_{mid} and mod_{min} in figure 3). Adding the same value to all phases, the difference between them still sinusoidal.

The carrier wave determination is done by the input current ripple generated by single carrier and bicarrier wave comparison. The algorithm selects the one that gives the lowest ripple, by comparing not clamped phases current signs (figure 3).

The next step, is the generation of switching signals (S_{max}, S_{mid} and S_{min} in figure 3), comparing mod_{max} and mod_{min} with main triangular carrier wave and comparing mod_{min} with the selected carrier wave. Finally, the switching signals are transformed to phases to drive switches (S_a, S_b and S_c in figure 3).

The outcome of ICRM-DPWM is a minimized input current ripple for all load angles, reducing switching losses as other general DPWM techniques. Basically, it compares the ripple generated by the bicarrier wave and single carrier wave, and selects the lowest of both every switching period. So the basic scheme has two parts: a zero sequence generation (v_0 in

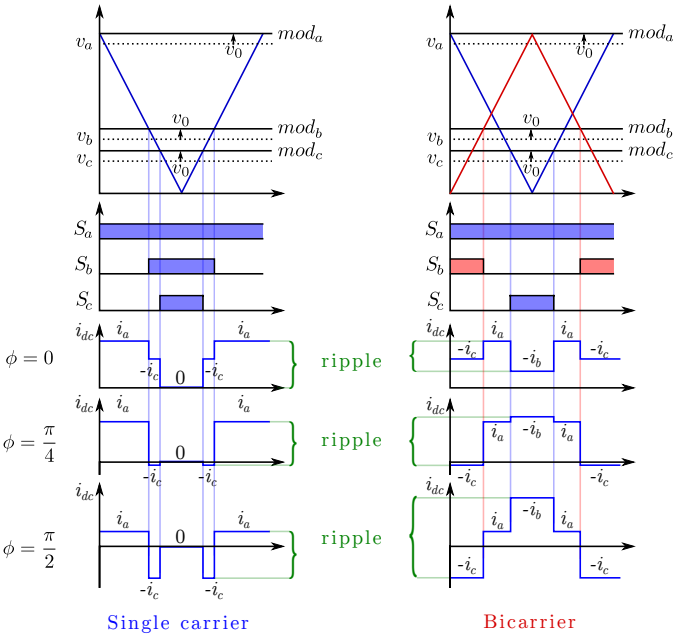


Figure 5. Input current ripple comparison between single carrier and bicarrier with different load angles ($\phi = 0$, $\phi = \pi/4$, $\phi = \pi/2$).

figure 4) and a carrier wave generation for each phase (Tri_a, Tri_b and Tri_c in figure 4).

The difference of input current ripples are shown in figure 5 as an example. Having the same modulation indexes in both techniques, with $\phi = 0$, the bicarrier technique obtains lower input current ripple, but with $\phi = \pi/2$, the single carrier technique gets a lower value.

In order to compare ICRM-DPWM with other modulation techniques, some parameters need to be defined, which are explained in the next section showing simulation results, in order to see differences between modulation techniques.

III. Comparison Parameters and Simulations

In this section, main comparison parameters are defined, and simulation results are shown in order to show differences between modulation techniques. These parameters are the switching losses, DC-link capacitor current rms value from input current waveform, and output current ripple rms value from output current waveform.

A. Switching loss factor

Switching losses depend on the voltage holding the switching device and the current across it during the switching interval. These losses generate heat, adding stress to devices. A comparison parameter of continuous and discontinuous PWM methods is the switching loss factor (SLF), which is defined as:

$$SLF(\%) = \frac{<P_{DPWM}>_T}{<P_{CPWM}>_T} \cdot 100\%, \tag{1}$$

where $<P_{DPWM}>_T$ and $<P_{CPWM}>_T$ are the mean values of switching power loss by DPWM and CPWM techniques in modulation wave's period T, respectively. The ratio depends

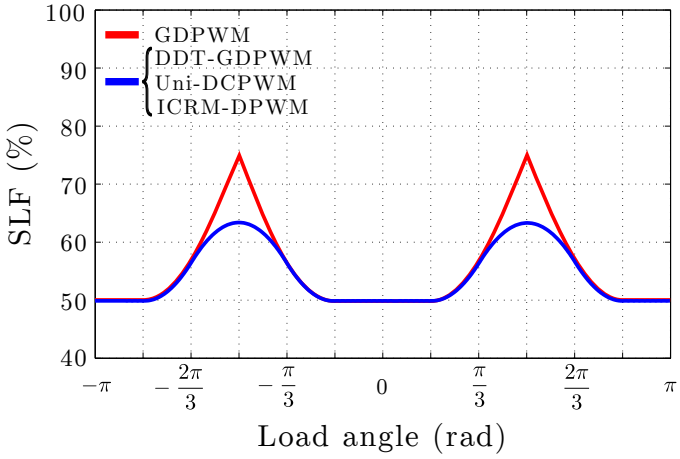


Figure 6. Calculated switching loss factors for different techniques.

basically on current absolute values, where the reduction of DPWM techniques comes from avoiding the switching action in one of the phases.

SLF is a switching power ratio between a DPWM and CPWM technique [10]. CPWM techniques commute in every switching period, and DPWM techniques avoid some switching intervals, so depending on clamping interval and load angle, the SLF has a variation. In general DPWM methods, the clamping interval is determined by the load angle, in order to minimize switching losses compared to continuous methods.

In figure 6, SLF is shown for different load angles. When load angle is $|\phi| < \pi/6$ or $5\pi/6 < |\phi| < \pi$, the SLF obtains the lowest value of 50%. When $|\phi| = \pi/2$, which is the worst case the SLF gets approximately 63% of the value, showing that even in the worst case, it saves losses.

B. DC-link capacitor rms current value

Some studies have analyzed the DC-link capacitor current in VSI topology [14], [20], [22]–[25], due to loss generation and heat defined as:

$$T_{Cap} = T_a + I^2_{Cap,rms} \cdot ESR \cdot R_{th,cap-a}, \tag{2}$$

where T_{Cap} is the capacitor temperature, T_a is the ambient temperature, $I_{Cap,rms}$ is the rms value of capacitor current, ESR is the equivalent series resistance, and $R_{th,cap-a}$ is the thermal resistance between capacitor and ambient.

A method used to analyze the capacitor rms current value is by calculating inverter input current. This is due to direct dependency of input current with switching vector and output current. Knowing the input current of the inverter (I_{Inv}), it is possible to calculate current rms value of the capacitor, by the input current rms value ($I_{Inv,rms}$) and the input current average value ($I_{Inv,dc}$) of the inverter (equation 3) [20]–[22]:

$$I^2_{Cap,rms} = I^2_{Inv,rms} - I^2_{Inv,dc}. \tag{3}$$

In figure 7, the capacitor's current rms value in $p.u.$ ($I_{Cap,rms}/\hat{I}$) is shown in some load conditions. When $\phi = 0$, the DDT-GDPWM gets highest value for all modulation range, and when $\phi = -\pi/2$, Uni-DCPWM gets the highest value.

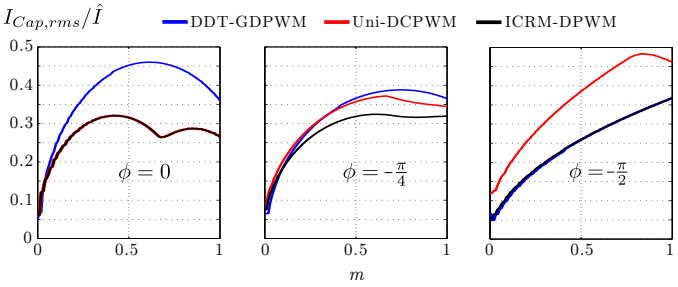


Figure 7. Calculated capacitor's current rms value ($I_{Cap,rms}$ in $p.u.$) depending on the modulation index for different load angles.

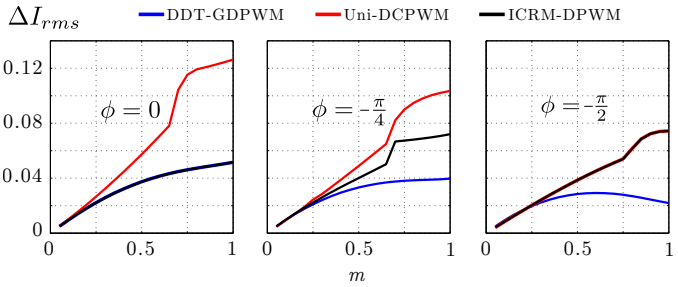


Figure 8. Calculated ΔI_{rms} $(p.u.)$ depending on modulation index for different load angles.

In those conditions, the ICRM-DPWM technique gets the minimal value. In an intermediate load angle ($\phi = -\pi/4$), the ICRM-DPWM takes advantage to both of techniques, lowering the rms value of both methods.

C. Waveform quality

Modulation techniques generate an output comprising the fundamental frequency and harmonics. In order to compare various modulation methods, output current ripple rms value is used, defined as:

$$\Delta I_a = I_a - I_{a,f}, \tag{4}$$

$$\Delta I_{a,rms} = \sqrt{\frac{1}{T}\int_0^T (\Delta I_a)^2 \cdot d\omega t}, \tag{5}$$

where ΔI_a is the current ripple, I_a is the measured data, $I_{a,f}$ is it's fundamental component and $\Delta I_{a,rms}$ is the rms value of the current ripple in phase a. In figure 8, the rms value (in $p.u.$) of the ripple current is shown, concluding that DDT-GDPWM has the lowest value for all load angles, so the highest output quality, and the highest value gets the Uni-DCPWM technique, getting the lowest output quality. The ICRM-DPWM quakity is in between, close to Uni-DCPWM in high power factor angles, and close to DDT-GDPWM in low power factor angles.

IV. Experimental Results

Experimental results have been measured by the system depicted in figure 9: a DC voltage source, a 6-IGBT inverter and R-L load with parameters listed in table I.

In figure 10, the capacitor current rms value is shown by the experimental results. The measured current has been I_{Inv}, as shown in figure 9, and processed with equation 3.

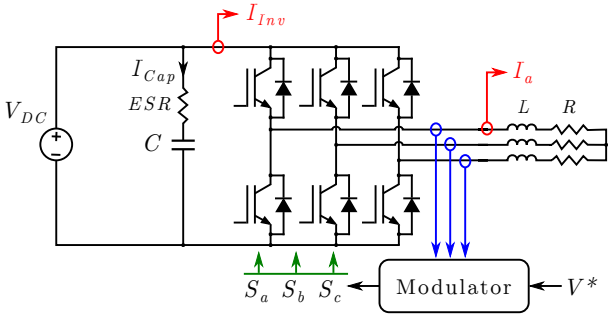


Figure 9. Source, inverter, control and load system.

Table I
Parameters of the system.

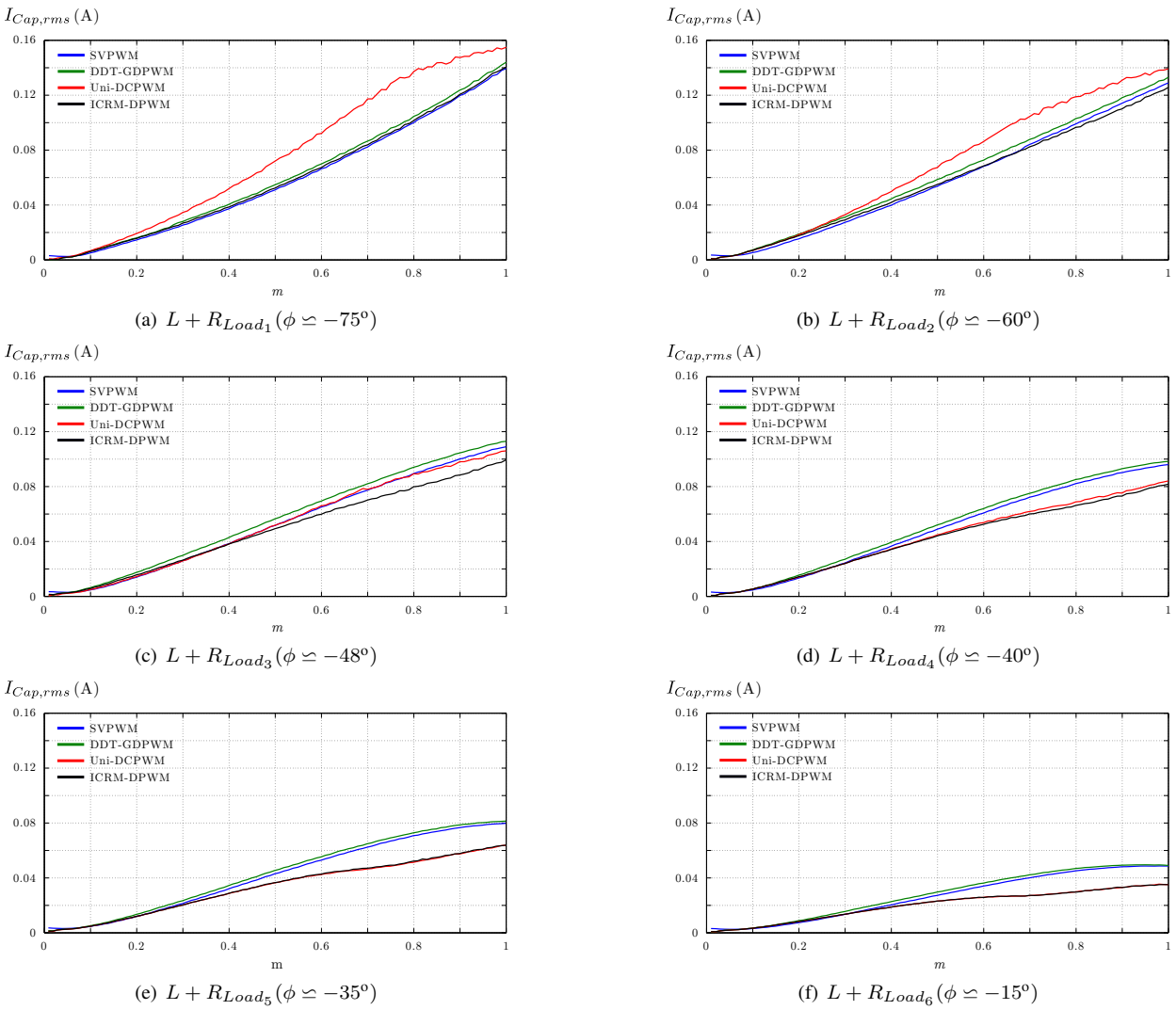
Parameter	Value
V_{DC}	$30\,V$
Inverter	SEMITOP® 3 SEMIKRON
Modulation frequency	$95\,Hz$
Switching frequency	$6\,kHz$
L_{Load}	$40\,mH$
R_{Load_1}	$2\,\Omega \rightarrow \phi_{Load1} = -75^o$
R_{Load_2}	$10\,\Omega \rightarrow \phi_{Load2} = -60^o$
R_{Load_3}	$22\,\Omega \rightarrow \phi_{Load3} = -48^o$
R_{Load_4}	$32\,\Omega \rightarrow \phi_{Load4} = -40^o$
R_{Load_5}	$47\,\Omega \rightarrow \phi_{Load5} = -35^o$
R_{Load_6}	$94\,\Omega \rightarrow \phi_{Load6} = -15^o$

Highest value of $I_{Cap,rms}$ is obtained in low power factors (figure 10(a)) and lowest values in high power factors (figure 10(f)). And it's visible that ICRM-DPWM gets the lowest value for all load angles, comparing to SVPWM, DDT-GDPWM and Uni-DCPWM. Comparing with the SVPWM, this method can achieve up to 33% of capacitor current rms reduction in best cases ($m = 0.75$, $\phi = -15^o$).

In the other hand, the output current quality is measured as the output current ripple rms value shown in figure 11. It shows that the worst quality is obtained by Uni-DCPWM, but DDT-GDPWM output quality is not as good as SVPWM. The ICRM-DPWM technique is between both general discontinuous techniques. The best case for input capacitor, is the worst case for output current quality, nearly doubling the output current ripple rms values comparing to classical SVPWM. But these values can be reduced by increasing the switching frequency, and in general DPWM techniques this is possible due to loss savings.

V. Conclusions

In this paper an optimized DPWM method is presented, oriented for switching devices and DC-link capacitor. The ICRM-DPWM technique reduces up to 50% of switching losses compared to continuous PWM methods, and reduces the input current ripple, obtaining a reduction in the capacitor current rms value up to 33% in best cases. So switching devices and DC-link capacitor's stress and losses have been reduced with this method. The output current quality is an intermediate between single carrier and bicarrier DPWM techniques. This suggests increasing the switching frequency to gain in quality, at expense of increase of SLF. It has



(a) $L + R_{Load_1}(\phi \backsimeq -75^{o})$

(b) $L + R_{Load_2}(\phi \backsimeq -60^{o})$

(c) $L + R_{Load_3}(\phi \backsimeq -48^{o})$

(d) $L + R_{Load_4}(\phi \backsimeq -40^{o})$

(e) $L + R_{Load_5}(\phi \backsimeq -35^{o})$

(f) $L + R_{Load_6}(\phi \backsimeq -15^{o})$

Figure 10. Capacitor rms current depending on the modulation index ($I_{Cap,rms}$ *vs.* m).

been simulated and implemented in hardware to obtain data, showing the feasibility of the technique.

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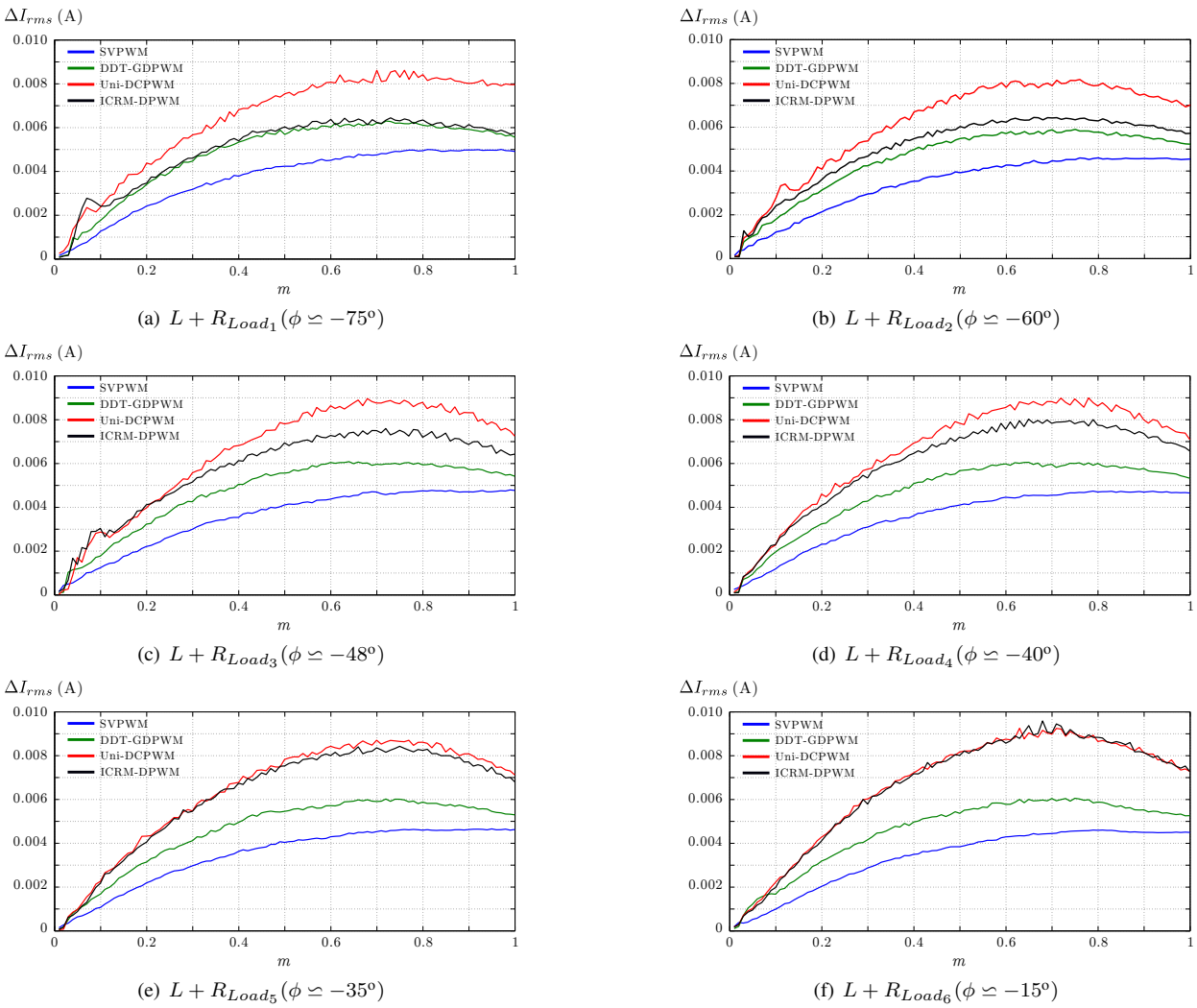

(a) $L + R_{Load_1} (\phi \backsimeq -75^{o})$ (b) $L + R_{Load_2} (\phi \backsimeq -60^{o})$

(c) $L + R_{Load_3} (\phi \backsimeq -48^{o})$ (d) $L + R_{Load_4} (\phi \backsimeq -40^{o})$

(e) $L + R_{Load_5} (\phi \backsimeq -35^{o})$ (f) $L + R_{Load_6} (\phi \backsimeq -15^{o})$

Figure 11. Rms value of output current of phase a depending on modulation index (ΔI_{rms} $vs.$ m).

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