

# Advanced power inverter topologies and modulation techniques for common-mode voltage elimination in electric motor drive systems

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## ABSTRACT

The demand for more reliable and efficient electric machines and drives is constantly growing in the renewable energy and transport electrification sectors. Such drive systems are usually fed by semiconductor switch-based inverters, which, unlike balanced pure sine-wave AC sources, produce large-amplitude, high-frequency common-mode voltage (CMV) waveforms, as a result of the application of pulse-width modulation (PWM). This can lead to a number of issues, such as high electromagnetic interference, deterioration of stator winding insulation, and leakage current flow through motor bearings, which dramatically reduce the life-cycle of machines and drives. Thus, this topic has been extensively investigated in the scientific literature, where either corrective or preventive mitigation approaches have been proposed. The former attempt to relieve the damage produced, whereas the latter tackle the problem at its root, by minimizing or eliminating the CMV produced by the inverter. This work provides a comprehensive review of the major CMV mitigation/elimination solutions, with emphasis on preventive actions, in the form of inverter topology variants and/or advanced modulation techniques. A wide picture of this subject is provided to researchers and field engineers, with valuable information and practical hints for the design and development of high-performance electric drive systems. Indeed, an in-depth analysis of the most recent literature clearly shows that best results are obtained by conveniently combining alternative topologies and modulation techniques, which, in some cases, make it possible to completely suppress the CMV component.

## 1. Introduction

Electric motor driven systems (EMDSs) have long been used for a variety of general industrial applications, such as heating [1,2], ventilation and air conditioning [3,4], elevators/lifts [5,6] and liquid pumping [7,8]. While EMDSs are still used for these purposes, another market field is gaining relevance outside industrial facilities: transport electrification [9,10]. Indeed, because of the growing concern and societal awareness over the global warming and the need to protect the environment, considerable resources are being directed to R+i into hybrid and fully electric vehicles (HEV/EVs) for road transit [11,12] as well as into electrically propelled air transport [13,14], e.g. to develop the “more electric aircraft” (MEA) concept [15–17].

In 2011, the International Energy Agency (IEA) conducted the first study<sup>1</sup> analyzing the impact of EMDSs on the global energy consumption [12]. EMDSs took around 43% of the global electricity supply, whose 70% belonged to industrial applications; see Fig. 1(a). Subsequent IEA reports confirm this picture [19,20], and predict that

the energy consumption of electric machines will grow steadily; see Fig. 1(b). More recently, the 2019 IEA ‘World Energy Outlook’ [21] forecasts a surge in the global electricity demand, in both ‘Stated Policies’ and ‘Sustainable Development’ scenarios; see Fig. 1(c). Here, the highest relative increment is experienced by the transport sector, whose electricity demand is estimated to double between 2030 and 2040 in both scenarios. Although the respective 2- and 4-PWh totals for 2040 may not seem large sums, observe that the transport sector has barely reached the 1 PWh mark in 2018–2020.

Along the same lines, the global electric motor market is likely to continue growing in the years to come. As a matter of fact, market reports estimate that the compound annual growth rate (CAGR) of electric motor manufacturing will range from 3.7% to 7.4% for different periods between 2016 and 2025 [22]. Given that the 2017 global electric motor market was worth US\$ 96,968 M, an expected CAGR of e.g. 4.5% would yield a US\$ 136,496 M market for 2025 [23]. As

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<sup>1</sup> This IEA study was a meta-analysis that considered data of third-party large regional studies, such as the European Union’s Lot 11 studies for the Eco-design Directive, the US Department of Energy-sponsored investigations, Japanese and Chinese studies and other regional data sources.

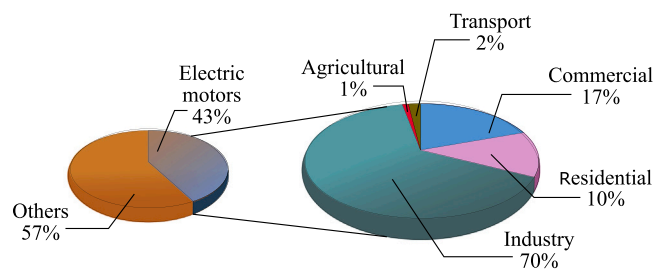
Nomenclature	
$B$	Boost factor
$C_x$	$x^{th}$ corrective solution
$C_b$	Parasitic bearing capacitance (F)
$C_{rf}$	Parasitic rotor-to-frame capacitance (F)
$C_{wf}$	Parasitic winding-to-frame capacitance (F)
$C_{wr}$	Parasitic winding-to-rotor capacitance (F)
$C_x$	x capacitor
$D_x$	x diode
$f_{sw}$	Switching frequency (Hz)
$M_a$	Amplitude modulation index
$N_L$	Number of different CMV steps per $T_{sw}$
$N_T$	Number of CMV transitions per $T_{sw}$
$P_x$	$x^{th}$ preventive solution
$SW_x$	Main switch with number of branch x
$SW'_x$	Complementary switch with number of branch x
$THD_c$	Total harmonic distortion of output current (%)
$T_{SW}$	Switching period or modulation period (s)
$v_b$	Bearing voltage of the electric machine (V)
$v_{CE}$	Collector-emitter voltage of the semiconductor (V)
$v_{CM}$	Common-mode voltage (V)
$V_{DC}$	DC-link voltage (V)
$v_{DS}$	Drain-source voltage of the semiconductor (V)
$v_{N0}$	Neutral-to-ground voltage (V)
$\mathbf{V}_{ref}$	Reference vector (V)
$v_{sh}$	Shaft voltage of the electric machine (V)
$\mathbf{V}_x$	x vector (V)
$v_{x0}$	x phase-to-ground voltage (V)
$Z_{N0}$	Capacitive neutral-to-ground parasitic imped. (F)
$Z_{xN}$	x phase impedance ( $\Omega$ )
$\Delta_p$	Peak-to-peak relative value of CMV waveform
$\Delta_S$	Height of largest relative value of CMV step
Abbreviations	
AC	Alternating current
AZS-PWM	Active zero-state PWM
BEV	Battery electric vehicle
CAGR	Compound annual growth rate
CB	Carrier-based
CCMV-PWM	Constant common-mode voltage PWM
CMC	Common-mode current
CMV	Common-mode voltage
DC	Direct current
D-PWM	Discontinuous PWM
EDM	Electric discharge machining
EMDS	Electric motor driven systems
EMI	Electromagnetic interference
EV	Electric vehicle

Fig. 2 shows, this progression is led by the vehicle motor manufacturing sector, which would hit a 50% market share in 2022. This prediction agrees with the expected growth of the electric vehicle stock shown in

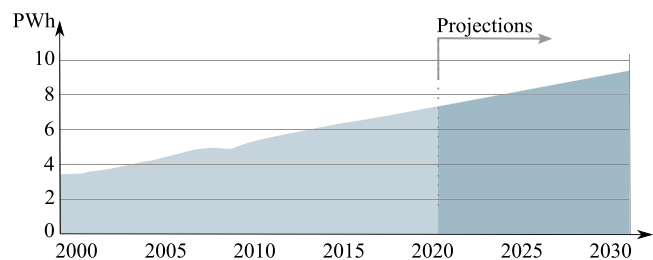
H7	VSI with additional DC-decoupling switch
H7D1	VSI with additional DC-decoupling switch and clamping diode
H7z	VSI with additional DC-decoupling switch and Zener diode
H8	VSI with two additional DC-decoupling switches
H8D2	VSI with two additional DC-decoupling switches and clamping diodes
H8z	VSI with two additional DC-decoupling switches and two Zener diodes
HBZVR	H-bridge zero-voltage rectifier
HERIC	High efficient and reliable inverter concept
HEV	Hybrid electric vehicle
IEA	International Energy Agency
IGBT	Insulated gate bipolar transistor
LCV	Light commercial vehicle
MD-PWM	Modified discontinuous PWM
MEA	More electric aircraft
MOSFET	Metal oxide semiconductor field effect transistor
MRS-PWM	Modified RS-PWM
NS-PWM	Near-state PWM
NST	Non-shoot-through
oH7	VSI with additional DC-decoupling switch and clamping switch
PHEV	Plug-in hybrid electric vehicle
PLDV	Passenger light duty vehicle
PV	Photovoltaic
PWM	Pulse-width modulation
Q-ZSI	Quasi-Z-source inverter
RCMV-PWM	Reduced common-mode voltage PWM
RS-PWM	Remote-state PWM
$R + i$	Research and innovation
SGR	Shaft grounding ring
ST	Shoot-through
SV	Space-vector
SV-PWM	Space-vector PWM
VSI	Voltage source inverter
VSIZVR	VSI zero voltage rectifier
VSIZVR-D1	VSI zero voltage rectifier with one clamping diode
VSIZVR-D2	VSI zero voltage rectifier with two clamping diodes
WBG	Wide-bandgap
ZSI	Z-Source inverter

Fig. 3, which would reach not only a remarkable hit of 250 M units in 2030, but even eight times as much, up to the 2000 M figure, in 2050 [10].

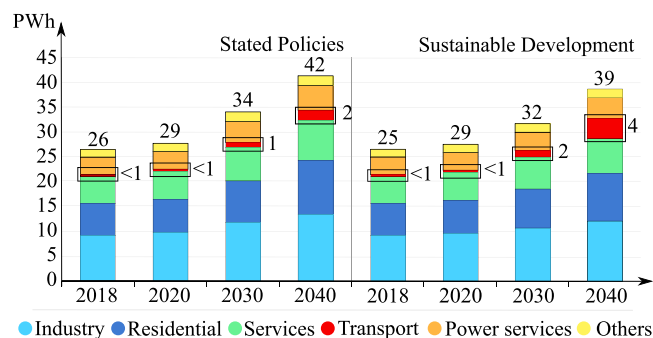
All these data point in the same direction: mechanical energy needs will increasingly be satisfied by electrical energy sources, particularly in the transport sector. Therefore, intensive research is already going on to keep up with this demand, in quest of more efficient [24–26], cost-effective [27,28], as well as reliable and durable [29,30] electric drives and motors. Here, the recurring issue of bearing failures is still one of the main concerns, because they account for 40% to 70% of electric machine breakdowns [31–33], as Fig. 4 illustrates. Indeed, bearings are critical for proper operation of electric machines because, among other duties, they must keep the rotor centered within the stator, so that



(a) Relative electricity demand in 2011 by end use [12, 18].



(b) Gross electric machine consumption trend (adapted from [19, 20]).



(c) Gross electricity demand by sector and scenario (adapted from [21]).

Fig. 1. Global energy consumption: impact of EMDs ([12,18–21]).

the rotor can turn with the least possible resistance [34]. Therefore, a bearing failure may cause not only a steady efficiency drop, but also motor malfunction and therefore high repair costs, and, ultimately, lead to a destructive fault of the whole system [31,33].

The use of pulse-width modulation (PWM) to synthesize AC sine waves represented a major breakthrough in EMDS technology. Before that, most bearing malfunctions resulted from mechanical and/or thermal issues, e.g. corrosion, vibrations, misalignment, etc. [34–36]. In PWM-based inverter-driven motors, however, bearing failures typically originate in the electrical domain, and more precisely as a consequence of the common-mode voltage (CMV) waveforms resulting from PWM modulation [37–40].<sup>2</sup>

Fig. 5 summarizes how high-frequency PWM sinewave generation can end up in bearing damage [34,36,45]: the PWM algorithm driving the power devices (Fig. 5, ①) produces rather unbalanced phase voltages (Fig. 5, ②), which yield CMV profiles having abrupt edges (Fig. 5, ③). These high  $|dv/dt|$  values excite some parasitic capacitances, and

<sup>2</sup> Analogously, and although it is not the objective of this work, CMV induces capacitive leakage currents in photovoltaic applications that flow in a resonant circuit between the converter, the AC filter and the grid [41–43]. As in motors, these stray currents can degrade and even produce breakages in critical mechanical elements such as the photovoltaic panels.

therefore a replica of the CMV attempts to develop in the shaft, which may easily exceed the dielectric breakdown voltage of the lubrication film inside the bearing (Fig. 5, ④). In that event, arcing discharge sparks will be produced between the races of the bearing, in the form of ringing current pulses (Fig. 5, ⑤), so that the charge built up in the shaft can flow back to earth potential or vehicle chassis, depending on the application [34,46]. This leaves the shaft at zero potential until the next CMV edge arrives, but at the expense of bearing damages, such as pitting and fluting (Fig. 5, ⑥) [36,45,47,48]. Last but not least, to make things worse, these fast-switching CMV shapes also deteriorate the stator windings (Fig. 5, ⑦) [49], and may create significant electromagnetic interference (EMI) [28,50–54].

In this scenario, CMV-related issues are increasingly drawing attention from the scientific community and the industrial world alike [47, 48,50,51,55]. Two main research lines can be distinguished, depending on where the focus is put: either caring for the bearings or acting on the electric supply — the inverter. The former includes such measures as replacing the classic rolling bearings with more robust ceramic bearings, or providing the drive-motor setup with a grounding ring, among others [39,45,56,57]. The latter, which tackles the issue right at the origin, can in turn be divided into three ‘sublines’: those which call for (i) leveraging classic filtering approaches [34,58], (ii) the use of advanced power conversion topologies [41,42,59], and (iii) modulation techniques for CMV reduction, particularly for such topologies [41,60–62].

In general, filters at the inverter output reduce high-frequency components and therefore electromagnetic noise [58,63,64]. Conventional CMV-specific filters are not an exception. Targeted to weaken the CMV before it enters the stator region [56,65,66], they have proved to lower the shaft-to-ground currents in up to 85% [34]. Cheaper and less bulky are the so-called ‘ $dv/dt$  filters’ or reactors [56,67], but they are useful only for some sorts of bearing currents [56,65]. A kind of advanced low-pass filter has also been proposed [67], referred to as ‘sine filter’, which pushes high-frequency currents away and, in addition, avoids the overvoltage effect, thus helping reduce EMI, and therefore making it a good complement to conventional CMV filters.

However, filtering is palliative rather than curative — filters do not remove the CMV, but prevent or make it more difficult for the CMV to get to the terminals of the motor [68]. Also, there is no universal filter to solve every CMV issue, so case-by-case approaches must be followed, which is time- and resource-consuming. In contrast, the other two source-focused preventive research sublines are currently gathering momentum, with publication of multiple recent, innovative contributions [41,42,69–71]. All these works present relevant CMV mitigation solutions but, up to date, there is virtually no work providing a complete, up-to-date picture on this topic. Therefore, the purpose of this work is to conduct a comprehensive review of the state of the art related to CMV issues and their mitigation, focusing on how advanced conversion topologies and modulation techniques can help PWM-based power converters to produce as balanced as possible phase voltages, in order to eliminate the CMV delivered to the motor. Indeed, acting on one of the primary causes of fatal breakdowns of electric machines is key to their successful operation in a wide variety of applications — transport and beyond.

This article is organized as follows: Section 2 explains why PWM-based sinewave synthesis results in such far-from-ideal CMV waveforms. Moreover, CMV-derived issues and their damaging consequences are also detailed, along with the corrective actions available to alleviate them. Then, Section 3 reviews the advanced converter topologies proposed in the literature that bring about CMV minimization, and Section 4 discusses the most significant modulation techniques, which provide additional CMV reduction. Finally, Section 5 draws the conclusions of this work, highlighting the fact that it is possible to completely suppress the CMV delivered to the motor.

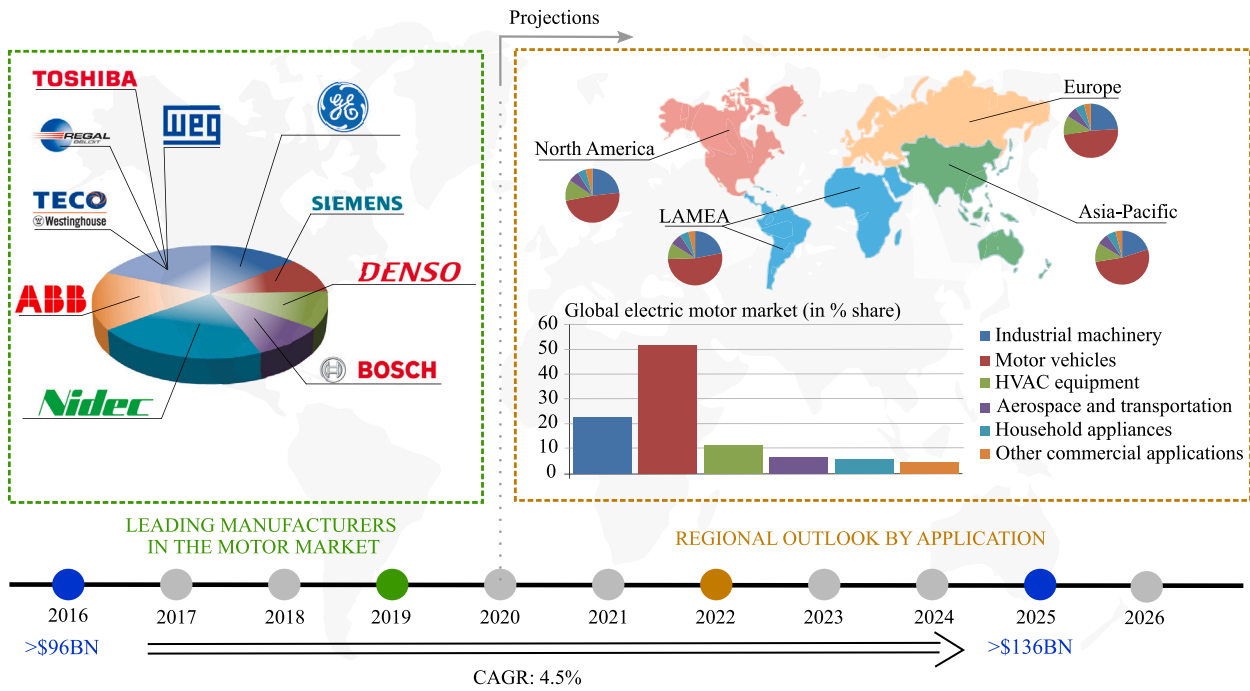


Fig. 2. Global electric motor market growth, in US\$ billions, by application, players and regions [23,44].

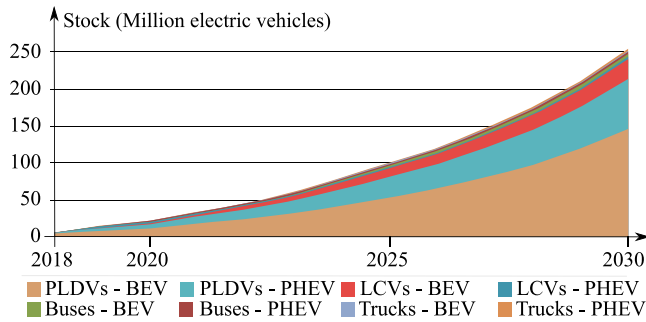


Fig. 3. Electric vehicle stock in the “EV30@30” scenario [72].

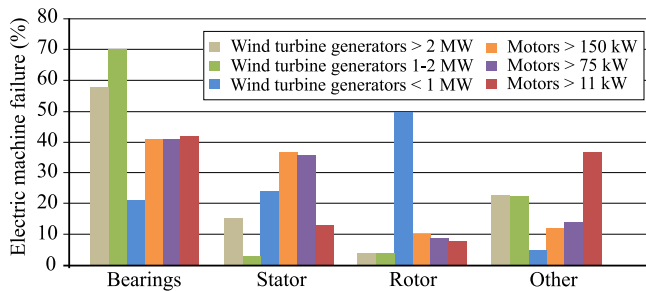


Fig. 4. Failure sources in electric machines by power range [73].

## 2. PWM-generated common-mode voltage and its effects

### 2.1. Common-mode behavior and equivalent circuit

Fig. 6 shows the most common power converter architecture used in variable speed drives: a two-level three-phase voltage source inverter (VSI). The VSI is grounded at half the DC-link voltage value ( $V_{dc}/2$ ) and is powering a star-connected motor, characterized by phase

impedances  $Z_{AN}$ ,  $Z_{BN}$  and  $Z_{CN}$ , and a capacitive neutral-to-ground parasitic impedance  $Z_{N0}$ .

Charge conservation at the neutral point requires that

$$\frac{v_{N0}}{Z_{N0}} = \frac{v_{A0} - v_{N0}}{Z_{AN}} + \frac{v_{B0} - v_{N0}}{Z_{BN}} + \frac{v_{C0} - v_{N0}}{Z_{CN}}, \quad (1)$$

which, for a balanced motor having equal phase impedances  $Z_{AN} = Z_{BN} = Z_{CN}$ , allows expressing the neutral voltage<sup>3</sup> as

$$v_{N0}(t) = \frac{3Z_{N0}}{3Z_{N0} + Z_{AN}} v_{CM}(t), \quad (2)$$

where  $v_{CM}(t)$  is the common-mode voltage (CMV) at the source, defined as

$$v_{CM} \triangleq \frac{v_{A0} + v_{B0} + v_{C0}}{3}. \quad (3)$$

Therefore, no CMV arises in AC line-operated motors, where  $v_{A0} + v_{B0} + v_{C0} = 0$ , but it does arise in motors powered from PWM-based VSIs. In this case, a CMV results whose amplitude is proportional to the DC-link voltage  $V_{DC}$ , and its frequency is related to the switching frequency  $f_{sw}$  of the VSI [47,75]. These facts are patent in Fig. 6, which shows the CMV waveform that arises in a typical two-level three-phase VSI making use of a conventional PWM modulation technique, such as Space-vector PWM (SV-PWM) [76].

Fig. 7 summarizes how the SV-PWM technique works, in the belief that its space-vector representation (hence the name) helps understand the influence of the modulation on the CMV. Every switching period  $T_{sw} = 1/f_{sw}$ , this technique uses (depending on the sector in which the reference voltage  $V_{ref}$  is located on the  $\alpha\beta$ -frame) two out of the six available active vectors ( $V_1$ – $V_6$ ), as well as two zero vectors ( $V_0$  and  $V_7$ ). So, Fig. 7(a) shows the space-vector distribution in the first sector, where  $V_1$  and  $V_2$  are used, as well as the two zero vectors. In this way,  $V_{ref}$  is synthesized by a linear combination of the selected

<sup>3</sup> Some authors reserve the term ‘common-mode voltage’ and its abbreviation CMV to denote the voltage at the neutral point,  $v_{N0}$ , whose shape resembles  $v_{CM}$  at the frequencies where the impedance ratio of (2) approaches unity [36,74].

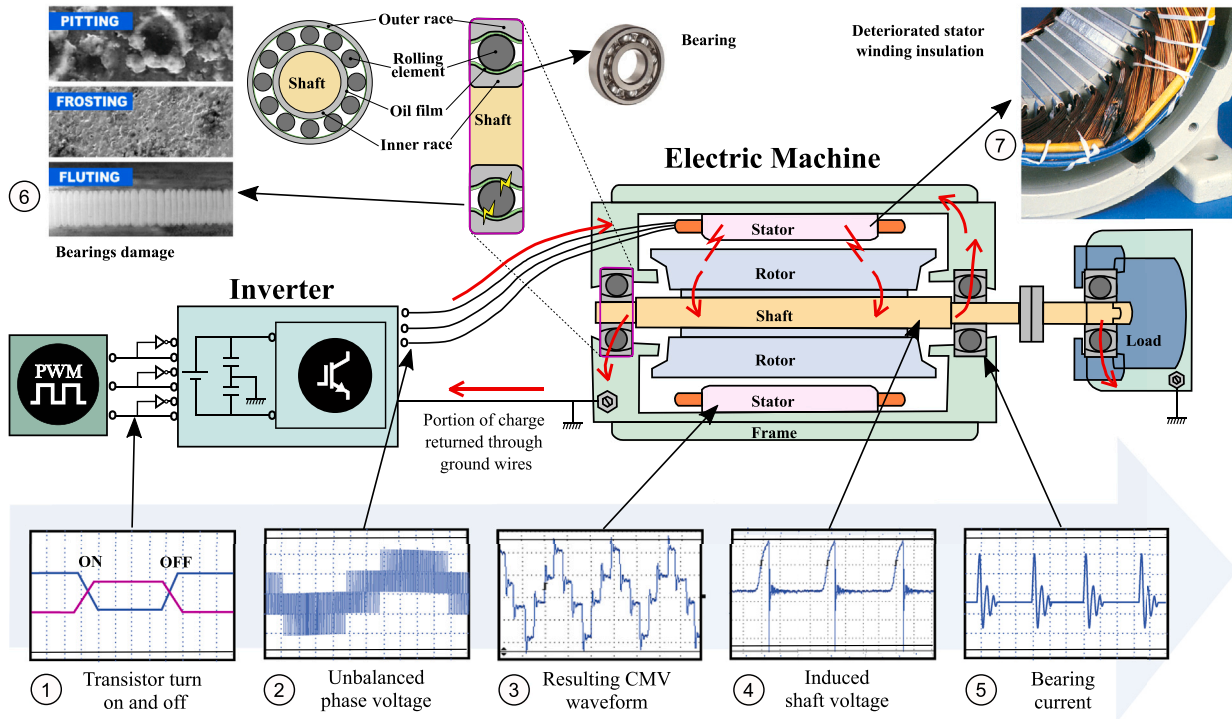


Fig. 5. A replica of the CMV attempts to develop in the shaft, which causes charge build-up and eventual spark discharging through the bearing(s).

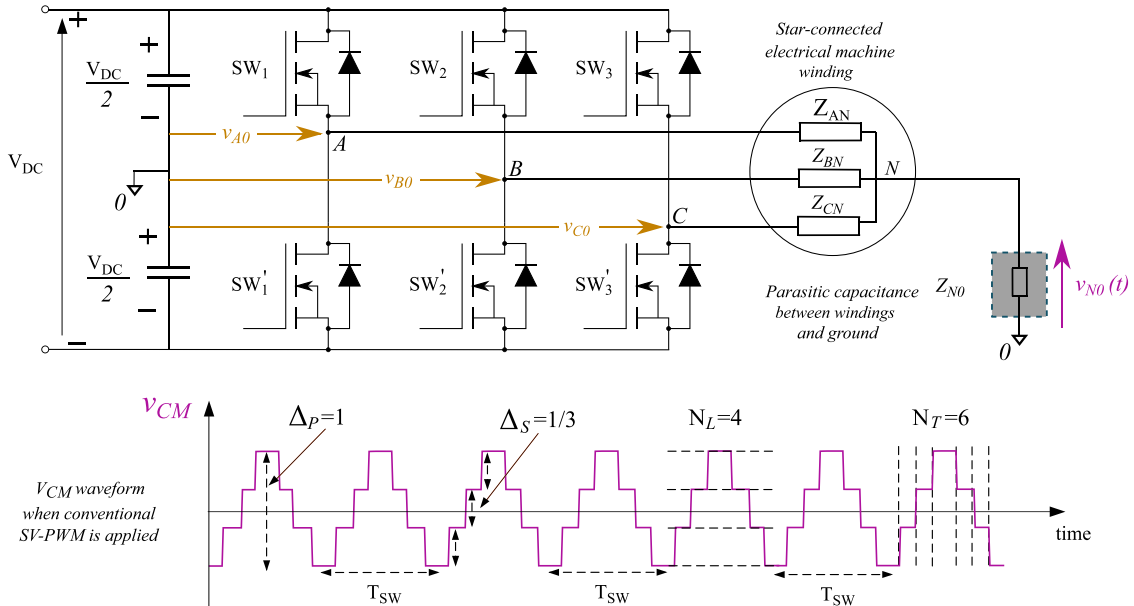


Fig. 6. Top: two-level three-phase voltage source inverter (VSI) with star-connected load. Bottom: CMV waveform synthesized by a conventional PWM, such as SV-PWM.

vectors. Moreover, for SV-PWM to operate in the linear range without overmodulation, the amplitude modulation index

$$M_a = \frac{|V_{ref}|}{V_{DC}/2} \quad (4)$$

must satisfy  $M_a \in [0, 2/\sqrt{3}]$ ; namely,  $|V_{ref}|_{max} = V_{DC}/\sqrt{3}$ . Thus, the SV-PWM technique allows synthesizing voltages with its highest harmonic quality and maximum linear range (Fig. 7(b)). Furthermore, it is possible to minimize the number of commutations (one per phase and modulation period) by appropriately selecting the modulation sequence (Fig. 7(c)). However, this modulation technique employs all available switching states or vectors (Fig. 7(d)), resulting in large CMV

variations, since the application of zero vectors produces the largest levels of CMV — as high/low as  $\pm V_{DC}/2$ .

These and other CMV-related particularities are best captured by the following ‘the lower the better’ figures-of-merit, which will be helpful in understanding and comparing the alternatives of CMV waveform to be presented in this work.

1.  $\Delta_p \in [0, 1]$  — Peak-to-peak value of waveform, relative to  $V_{DC}$ .
2.  $\Delta_s \in [0, \Delta_p]$  — Height of largest CMV step, also relative to  $V_{DC}$ .
3.  $N_L$  — Number of different levels per  $T_{sw}$ .
4.  $N_T$  — Number of transitions (step shifts) per  $T_{sw}$ .

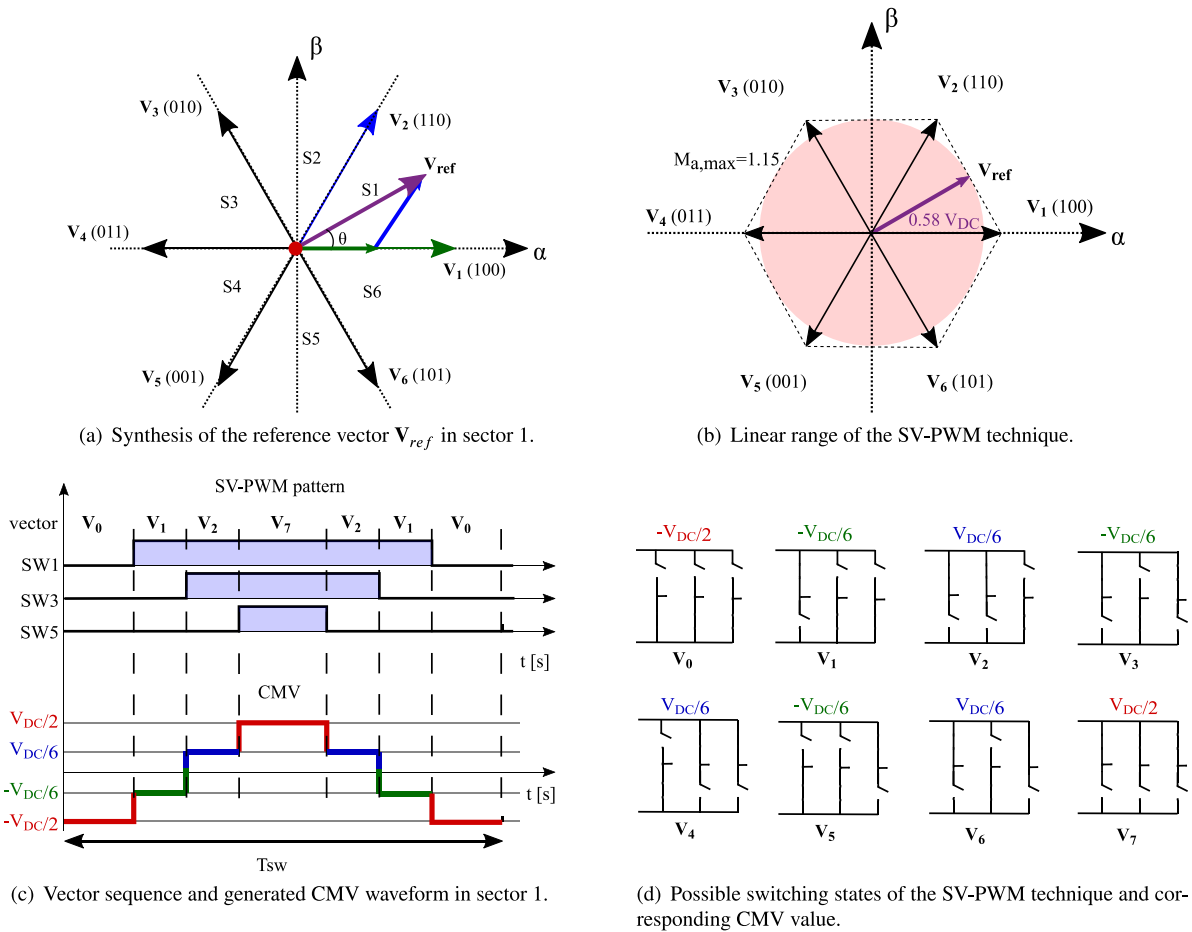


Fig. 7. Vector representation of the SV-PWM technique along with switching states and associated common-mode voltage levels.

In these terms, SV-PWM is characterized by  $\Delta_p = 1$ ,  $\Delta_S = 1/3$ ,  $N_L = 4$ , and  $N_T = 6$ , which are rather poor values from the CMV perspective, as will soon be shown. Indeed, these indicators can be improved (lowered) by using alternative VSI topologies, as well as appropriate CMV reduction modulation strategies. Essentially, this means modifying the turn-on and turn-off sequences of the power switches. These topics will be covered in Sections 3 and 4, respectively.

## 2.2. Parameters affecting the common-mode voltage waveform

The following parameters also affect the CMV waveform; see also Fig. 8:

(a) *DC-bus voltage ( $V_{DC}$ )*. It refers to the instantaneous voltage of the electric drive input (recall Fig. 6). This value depends on the system specifications and the peak-to-peak value of the CMV is proportional to  $V_{DC}$ , resulting in  $\Delta_p \in [0, 1]$  (Fig. 8(a)). Thus, from the CMV perspective, and in those cases where an adequate preventive action against the CMV is not used, it could be desirable to reduce the  $V_{DC}$  value as long as the operating requirements of the electric drive are met.

(b) *Switching frequency ( $f_{sw}$ )*. In a VSI, this frequency is the rate at which the power semiconductor is turned on and off. Among others,  $f_{sw}$  is directly related with power losses, which become higher at higher frequencies. On the other hand,  $f_{sw}$  greatly affects the CMV since increasing it increases the number of CMV level shifts in some fixed time interval (Fig. 8(b)) [47]. In addition, as the number of CMV variations increases, the induced voltage amplitude on the machine shaft also increases. In fact, depending on the common-mode impedance ( $Z_{N0}$ , Fig. 6) characteristics, the shaft voltage varies with

$f_{sw}$  [47]. If the impedance is capacitive for a given  $f_{sw}$ , the amplitude of the motor shaft voltage will increase as the switching frequency increases. However, if it is inductive, the amplitude will decrease with increasing frequency. For this reason, shock filters, which include inductive elements to compensate the common-mode impedance, are sometimes used [47].

(c) *Switching speed of semiconductor devices ( $dv_{DS}/dt$  or  $dv_{CE}/dt$ )*. The switching time ( $t_r$  and  $t_f$  for rise and fall times, respectively), which are specific to each semiconductor device, determines the  $dv/dt$  of the phase voltages (Fig. 8(c)). This speed affects power losses, among other issues, and to a lesser extent, the CMV. Although the high-frequency CMV noise increases as the switching time decreases, the influence of this CMV noise is limited, both for the CMV and for the voltage induced on the machine shaft [47]. Therefore, and since  $t_r$  and  $t_f$  (usually several ns) are small compared to  $T_{sw}$  (usually several  $\mu$ s), the CMV can be considered almost unaffected by the switching speed [47].

(d) *Modulation index ( $M_a$ )*. This parameter, already introduced in (4) for SV-PWM, represents the ratio between the modulating and the carrier wave amplitudes.  $M_a$  allows scaling the modulus of the voltage reference vector from 0 to 1.15 (considering SV-PWM). Likewise, this parameter facilitates the estimation of the CMV waveform, because such waveform depends on the modulus of the reference vector. Although the relationship between the application times and the modulation index is discussed in more detail in Section 4, it can be seen that low  $M_a$  values produce large zero vector application times ( $t_0$ ) and short active vector application times ( $t_i$ ) (Fig. 8(d)), whereas high  $M_a$  values have the opposite effect. This relationship between vector application times and  $M_a$  result in CMV mean value variations, and becomes particularly marked for large  $M_a$  values, as Fig. 8(d) shows.

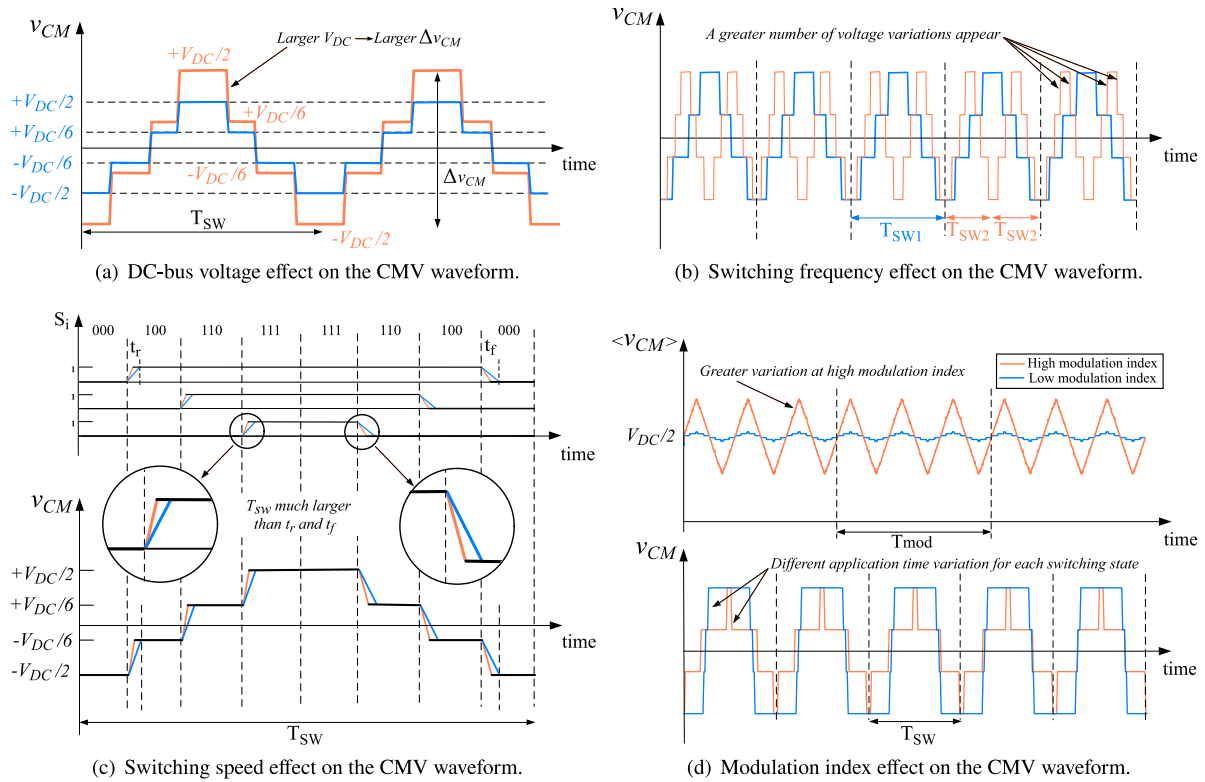


Fig. 8. Variation of the CMV waveform due to the main parameters that affect it.

### 2.3. Unwanted effects of common-mode voltage

As a consequence of CMV, there are some unwanted effects on the electric drive system. Among them:

**(a) Electromagnetic interference (EMI).** The switching patterns and resulting voltage waveforms produced by the converters that feed electric motors, combined with the intrinsic parasitic impedances between the different parts of these motors, cause several types of conducted and radiated EMI [77,78]. In particular, this EMI source may affect other subsystems of the electric drive, because of the paths of the common-mode impedances highlighted in Fig. 9. Besides, such subsystems can in turn introduce radiated or conducted EMI back to either the converter or the motor or both, which could further increase the overall EMI levels.

CMV-related EMI issues can also be addressed following either corrective or preventive actions. Although the most salient corrective actions for CMV problems are discussed in the next Section, common corrective actions against EMI problems include: (i) low impedance power cables, such as laminated cables or special alloys made cables; (ii) same length twisted pair connection cables and; (iii) different types of mechanical shielding in the architecture most sensitive areas and in key connection wires [79–82]. Nonetheless, preventive actions are usually preferable since they avoid or reduce the CMV generation, tackling the problem at the origin (Sections 3–4).

**(b) Winding insulation damage.** CMV causes significant stress on the stator winding insulation (Fig. 10) due to the large  $|dv/dt|$  values at the input terminals of the machine produced by the PWM technique [83–85]. This is especially harmful in motor drives with long cables between the motor and the drive, which can lead to premature failure of the electric machine [28]. To protect against these damages, Polyimide nano-composite film-based insulators (such as Kapton 100CR) are typically used [86], so the issue could be addressed by seeking alternative insulation solutions that allow extending the service lifecycle of the

electric machine. However, it could also be minimized by using corrective solutions (Section 2.4) such as, for example, short cables or any preventive action that reduces CMV from the source (Sections 3–4).

**(c) Induced shaft voltage.** The CMV also induces high-frequency voltage on the electric machine shaft ( $v_{sh}$ , Fig. 11) [87–89], again due to the PWM applied to the inverter, as well as to the existence of a parasitic capacitance in the machine [47].<sup>4</sup> This problem is directly related to the motor bearing failure. When the voltage induced on the motor shaft exceeds the insulating capability of the bearing grease, it causes a circulating bearing current, resulting in pitting and fluting of the bearing races. Bearing failure is an expensive problem both in terms of motor repair and downtime, so helping to prevent this by measuring shaft voltage is an important diagnostic step [33]. However, if this is not sufficient, as counter-measures or techniques to protect the bearings against induced shaft voltage, bearing insulation and shaft grounding brushes are widely used solutions [33].

**(d) Bearing currents.** Although shaft voltage is directly related to a type of bearing current, fast CMV variations generate more leakage currents that flow through the motor bearings as a result of the presence of several parasitic capacitances (Fig. 12).<sup>5</sup> Four sources of bearing

<sup>4</sup> In addition to high-frequency voltage, low-frequency effects mainly produced by the asymmetry of the motor windings also occur [90]. In traditional drive systems, these effects can be categorized into (i) alternating voltages induced in the shaft, (ii) homopolar magnetic flux, (iii) friction-derived electrostatic effects, and (iv) external potentials [33].

<sup>5</sup> The visual impact of bearing damages can be classified into five types: fluting, frosting, pitting, spark tracks, and welding [33]. Fluting is characterized by transverse evenly distributed flutes burnt into the bearing race. Frosting is characterized by small “craters”, which are formed during electrical discharges. Pitting, which consists in much larger “craters”, is a more serious form of frosting. Spark tracks are irregulars and often askew to the direction of the rotation. Welding is linked to a large amount of current passing through a bearing and can easily be seen to the naked eye.

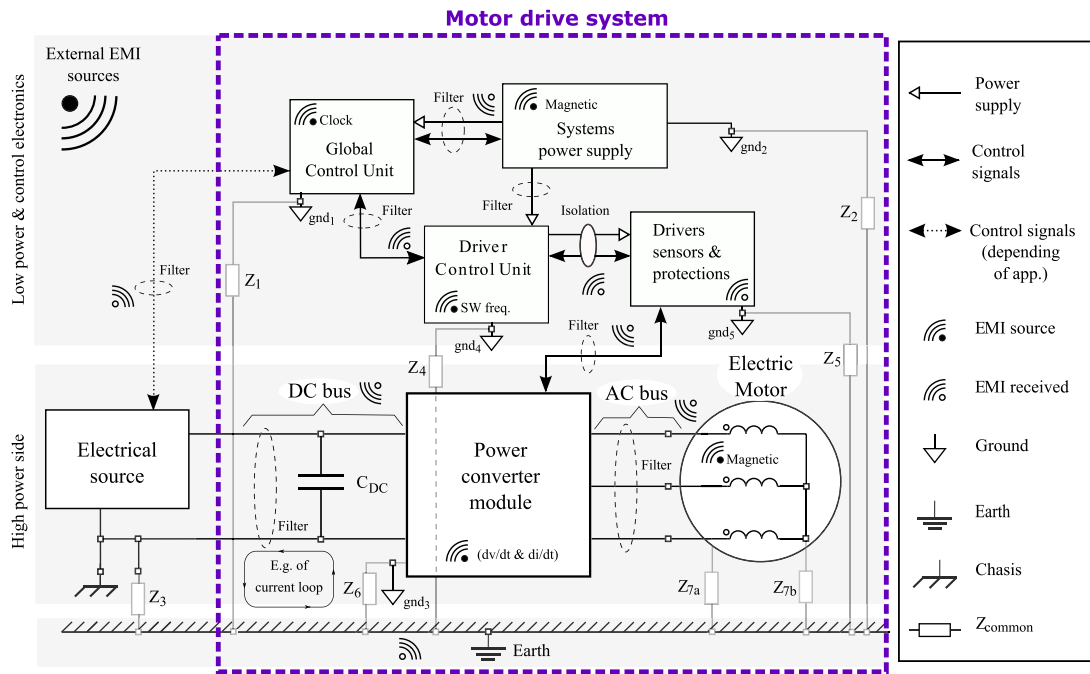


Fig. 9. Identification of EMI sources in electric drive systems. Source: Adapted from [9].

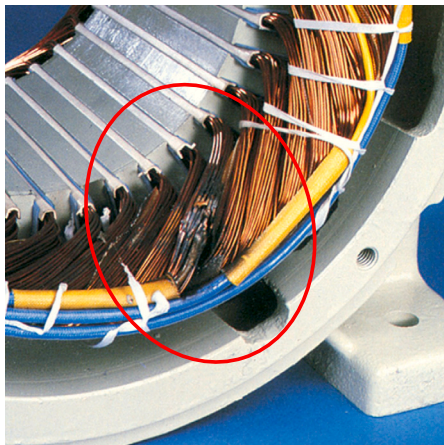


Fig. 10. Typical winding insulation damage by voltage surge leading to a short circuit between the stator windings in a three-phase induction motor [91].

currents can be distinguished, which are described below along with their approximate amplitude ranges:

1. Capacitive currents (5 mA–0.2 A). When the rotor lubricant film is undamaged it behaves like an insulator, forming a stray capacitance ( $C_b$ ) in the bearing (Fig. 11). As a result of the capacitive divider formed by the parasitic capacitance between the stator winding and the rotor ( $C_{ur}$ ), the capacitance between the rotor and the stator frame ( $C_{rf}$ ), and the capacitance formed in the bearing ( $C_b$ ), high frequency CMV produces  $v_b(t)$  voltage on the bearing (Fig. 11). Consequently, a capacitive bearing current

$$i_b(t) = C_b \frac{dv_b(t)}{dt} \tag{5}$$

appears, but its amplitude is small [33], and therefore is not considered relevant, compared to the currents presented in the following items [56,92].

2. Electric discharge machining currents (0.5–3 A). Also called EDM currents, they arise as a result of  $v_b(t)$  exceeding the dielectric strength of the bearing lubricant, because a shaft-to-motor frame electric discharge then occurs through the bearings (Fig. 12, in green) [33,93,94]. This results in pitting, grinding and spline on bearings [37,95]. In addition, EDM currents can cause serious breakdowns, and their effects are especially harmful in motors of less than 110 kW [56,95].
3. Circulating currents (0.5–20 A).<sup>6</sup> Voltage variations at the motor terminals generate a common-mode current (CMC) that flows into the parasitic capacities of the stator through the motor frame (Fig. 12, in blue). This current creates a time-varying magnetic field around the motor shaft, which in turn induces a voltage drop along the shaft. If this voltage is large enough, it drills the bearing lubricating film, destroys its insulating properties, and generates circulating currents [93,96]. The maximum amplitude of these currents depends on the size of the motor [33, 56,92].
4. Rotor-to-ground current (1–35 A). If the motor is grounded through the load, part of the total ground current can pass through the rotor to ground (Fig. 12, in red). Depending on high frequency impedances of the stator and rotor frame-ground connection, as the motor size increases, this current can reach considerable magnitudes [33]. When this current passes through the bearings, they can be damaged quickly [56,92,95], so special care must be taken with this current.

Although each one of the currents described above has its particularities, they all have in common that depend on certain parameters such as motor size, motor speed, and bearing temperature [56,92]. The literature states that motor speed and bearing temperature mainly affect the magnitude of the bearing currents. The severity of the affection depends on the power rating of the motor: in small motors

<sup>6</sup> In addition to currents produced by the CMV, low-frequency circulating currents might arise due to the existence of a magnetic field asymmetry between the rotor terminals (due to manufacturing tolerances or generation of unbalanced voltages) [34,36].



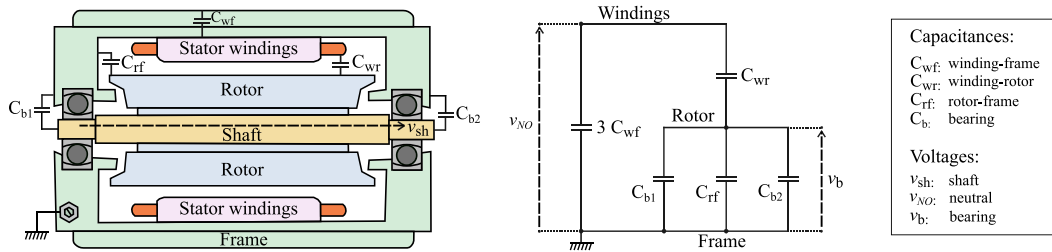


Fig. 11. Voltages produced in the electrical machine by the existing parasitic capacitances and the equivalent electrical circuit.

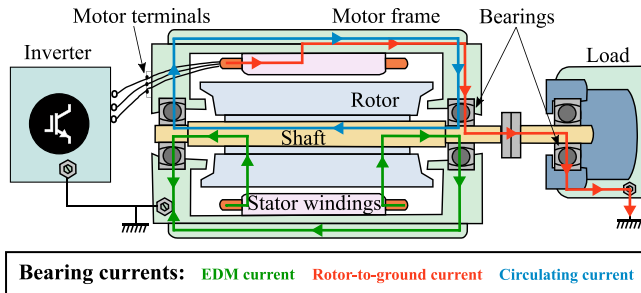


Fig. 12. Bearing currents' paths. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

with EDM currents, as bearing temperature increases, bearing current is reduced and shifted to higher motor speed (Fig. 13). Conversely, for large motors, the circulating bearing currents reach maximum values at low motor speed and at higher bearing temperature [56]. Furthermore, motor size has a significant influence on the nature of the bearing currents and on the magnitude of the bearing and ground currents (see Table 1). In small motors, only EDM currents occur, whereas in large motors distinctive circulating bearing currents are observed [56].

2.4. Corrective techniques to mitigate the common-mode voltage effects

Fig. 14 shows the consequences of CMV in electric drive systems. In particular, Fig. 14(a) summarizes the effect chain triggered by the CMV in the inverter-motor assembly, including the possible solutions to each problem and consequences derived. Fig. 14(b) shows the physical location of each solution, and a summary of the possible corrective approaches. Broadly speaking, there are two families of solutions [56, 68]:

- Corrective actions ('Cx' tags) are techniques aimed at mitigating other undesired effects produced by the CMV after CMV occurs, such as counter-measures against bearing currents within or at the motor, or against EMI in electric drive system. In general, these encompass assembly procedures and additional external elements that may be required to diminish, or further minimized the CMV-derived problems.
- Preventive actions ('Px' tags) are the group of solutions which comprises the mitigation techniques on the inverter side, aimed at directly reducing the CMV before it leads to further problems. In general, these are mainly those that involve the control, layout and architecture of the inverter.

A brief review on corrective actions follows, leaving the more in-depth study of preventive actions to Sections 3 and 4. In this sense, corrective solutions can be further classified into two categories: either

those solutions blocking the current path (leakage current insulation solutions, Fig. 14(c)); or those providing a more appealing current path (ground leakage current discharge solutions in Fig. 14(d)). Among the former stand out:

(C1) Faraday shielding. This solution consists on a conductive shield between the rotor and the stator, which blocks the current from the inverter, thus preventing it from being induced in the shaft [97]. This solution is extremely difficult to implement and very expensive, so it is seldom used in practice [45]. Moreover, it is only effective for EDM currents, since using this technique can be harmful for other types of undesired currents, such as circulating currents [56].

(C2) Insulated bearings. The use of insulated bearings prevents the shaft current from being discharged into the stator frame through them [45,98]. Generally, a non-conductive resin or ceramic layer is used as insulator material. However, due to the capacitive effect of the insulator, EDM currents can still pass through the insulated bearings [45]. This technique requires a special modification of the electric machine, which increments the implementation cost. In addition, this solution can transfer the problem to other motor areas, so it is not considered a fully effective technique [35].

(C3) Ceramic or hybrid bearings. This type of bearing has either a ceramic rolling element and a steel track or both ceramic elements. This prevents the shaft current from flowing through the bearings, which makes this solution particularly effective in small motors [56,65]. However, these bearings are significantly more expensive than conventional steel bearings and may shift the problem to other parts of the inverter-motor assembly, as occurs with insulated bearings, which may make their adoption cost-inefficient [45,57].

(C4) Conductive grease. This grease contains conductive particles that provide a continuous electric path through the bearings, thus reducing harmful discharges produced by shaft voltage [34,45]. On the downside, these particles can increase the mechanical wear of the bearings, which would render the lubricants ineffective and cause premature failures. This solution is therefore not currently considered as viable [45].

(C5) Insulated mechanical load coupling. This technique avoids possible damage in the driven load by isolating the leakage currents that could flow towards it. This is an effective solution against rotor-to-ground currents, but not against other types of bearing currents [35,56].

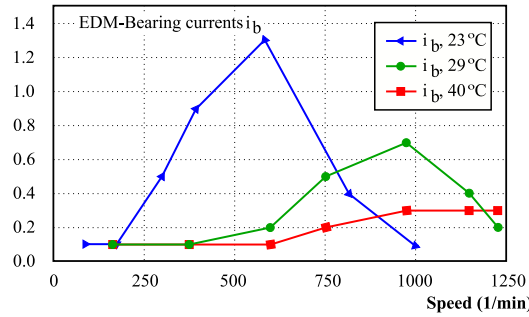
The following techniques stand out among those providing a more attractive alternative path to earth ground; see also Fig. 14(d):

**Table 1**  
Impact of leakage currents on electric machines according to machine size [56].

Motor size (shaft height in mm)	Capacitive currents	EDM currents	Circulating currents	Ground rotor currents
Very small (63)	↓	↑	–	↑
Small (160)	↓	↑	–	↑
Large (280)	–	↑	↑	↑↑
Very large (400)	–	–	↑↑	↑↑↑

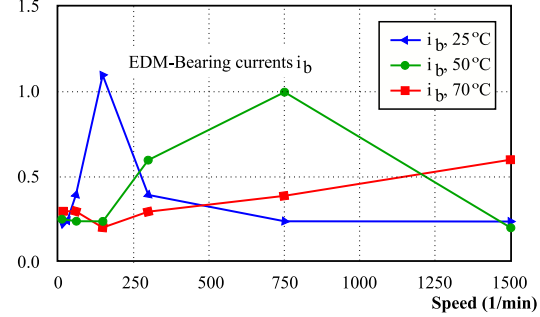
Table notes: – Not affect; ↓ Negligible impact; ↑ High impact; ↑↑ Very high impact; ↑↑↑ Extremely high impact.

**Bearing current pk-pk (A)**



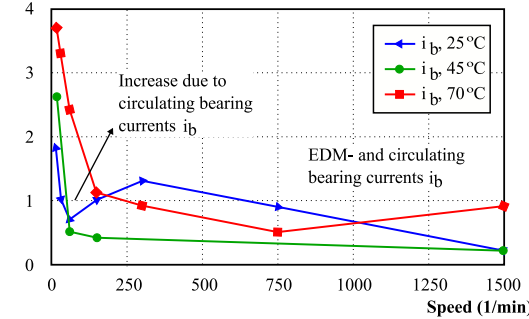
(a) 1 kW power with permanent magnet motor (4 poles and 63 mm of shaft height) and inverter with asynchronous PWM ( $f_{sw} = 9 \text{ kHz}$ ).

**Bearing current pk-pk (A)**



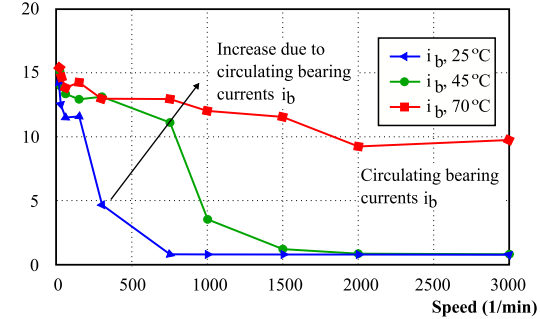
(b) 11 kW power with induction motor (4 poles and 160 mm of shaft height) and inverter with asynchronous PWM ( $f_{sw} = 3\text{--}14 \text{ kHz}$ ).

**Bearing current pk-pk (A)**



(c) 110 kW power with induction motor (4 poles and 280 mm of shaft height) and inverter with direct torque control (hysteresis control,  $f_{sw} = 2\text{--}3 \text{ kHz}$ ).

**Bearing current pk-pk (A)**



(d) 500 kW power with induction motor (2 poles and 400 mm of shaft height) and inverter with asynchronous PWM ( $f_{sw} = 1.7\text{--}2.5 \text{ kHz}$ ).

**Fig. 13.** Influence of motor speed and bearing temperature on bearing currents according to the measurements carried out in [56].

(C6) *Shielded cable.* This solution provides an alternative low-impedance electric path to the currents generated by the CMV to return to the inverter via symmetrical ground protection cables [34,35]. This significantly reduces EMI and eliminates, almost completely, rotor-to-ground currents. However, stator-to-ground currents are increased up to 40% and, in large motors, the same applies to circulating currents [65]. In addition, the length of these cables, together with the high switching speed of the semiconductor devices, causes overvoltage at the motor terminals, thus creating partial discharges and premature ageing of the winding insulation [67].

(C7) *Grounding cables.* It is critical to provide adequate grounding points so that the currents can easily flow through them [34,92]. For this purpose, thin-film cables are usually used, either on the motor, on the inverter, or on the load, so high-frequency currents are derived to ground [99]. Within these solutions, a high-frequency grounding strap stands out that consists in a twisted cable which decreases the impedance between the motor frame and the ground [100].<sup>7</sup>

<sup>7</sup> This solution together with the shaft grounding ring (SGR) have been patented by the AEGIS company.

(C8) *Brushes.* Metal or carbon brushes provide the bearing with a parallel electrical connection between the shaft and the motor frame. This solution is better than the insulation, because it offers an alternative discharge path and avoids bearing currents. However, depending on the brush type chosen, they can easily wear out or become contaminated. In addition, the cost of the brushes is variable, and they can only be applied selectively according to the size of the motor and its particular use [45,57,95]. This solution is effective against EDM currents, but not against circulating currents [56].

(C9) *Shaft grounding ring (SGR).* Like brushes, this solution provides a very low-impedance path between the shaft and the motor frame, thus preventing leakage current circulation through the motor bearings [45,57]. The solution consists on a micro-conductor fiber-based ring specially designed to redirect the shaft current [101,102]. Unlike brushes, its wear is negligible, and it is very resistant to contamination. In addition, it is a low-cost action, which can be applied to virtually any motor regardless of size and application. However, this technique does not eliminate completely the bearing currents due to the low impedance between the balls and the bearing races [45]. Nevertheless, it is one of the best existing corrective actions [34] incorporated by several motor manufacturers such as ABB, Regal Beloit, WEG Electric, TECO-Westinghouse, GE and Nidec [67,92,95].

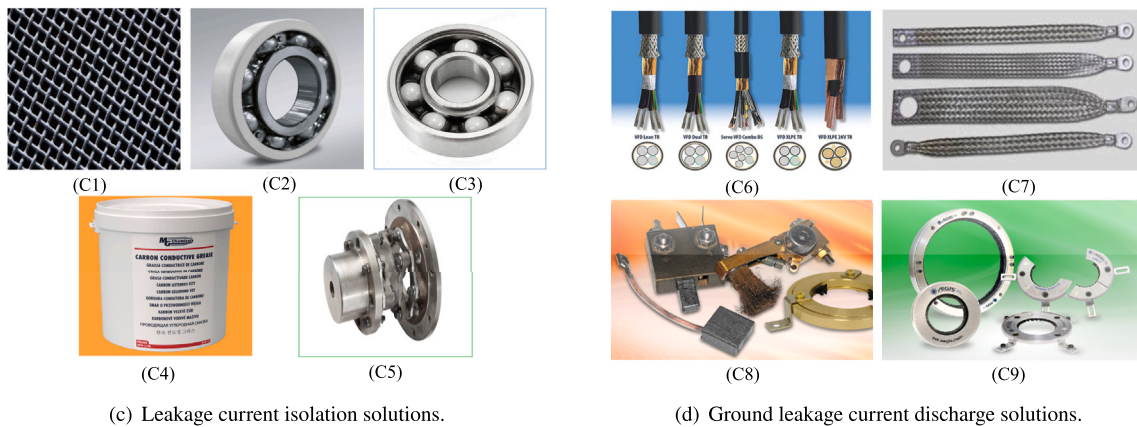
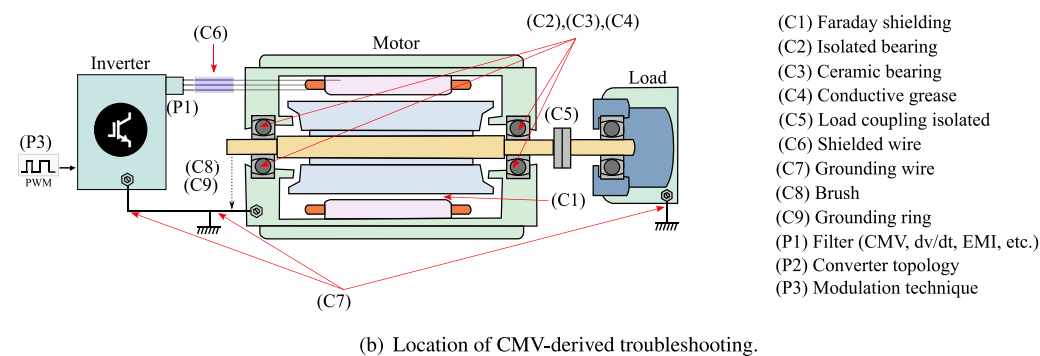
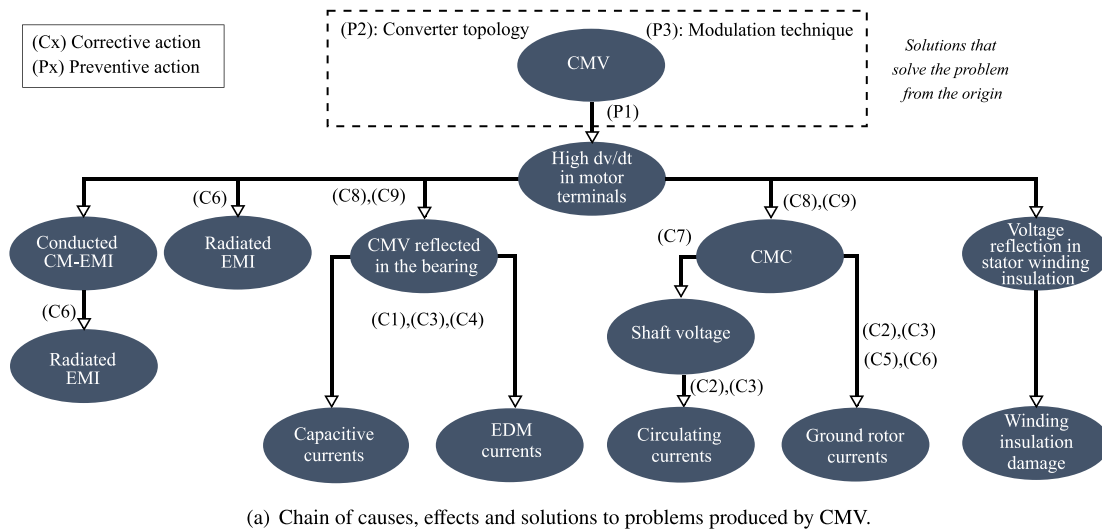


Fig. 14. Problems caused by CMV in an electric drive system and its main solutions, emphasizing corrective actions.

To summarize, in each particular case and as long as the CMV represents a considerable threat to the integrity of the motor, it is necessary to assess the situation to determine whether it is worth tackling the problem at its source, or one had better mitigate its effects [103]. In some cases, the required solution or solutions will exceed what can be addressed at the design stage. In other cases, it may be necessary to combine several of the existing solutions to achieve high reliability in the electric motor-driven system assembly [103].

As stated before, corrective actions can be leveraged to mitigate the effects of CMV, but they do not prevent the CMV generation. Preventive actions, for their part, reduce or even eliminate the CMV effects from the electrical/electronic point of view. Among these preventive actions, inverter output filters (P1) are commonly used to reduce the effects generated by the CMV. However, they do not completely reduce

them and, basically, they confine the CMV in the VSI, preventing it to travel to the motor terminals [68]. In contrast, alternative power converter topologies (P2) allow to reduce or eliminate CMV. For example, there are single-phase or three-phase topologies for photovoltaic applications [42,104,105] that reduce CMV, and are also some two-level three-phase solutions for applications with electric drives [48,106,107], even multiphase topologies [51,69,70] or topologies with a greater number of levels [108,109]. Moreover, several modulation techniques (P3) have been proposed [39,40,61], which allow to reduce or eliminate CMV. This last is a cheap solution since, as soon as the digital controller can deal with the technique, no additional hardware elements are required (it is not necessary a modification of the motor structure or the converter hardware). Thus, these advanced converter

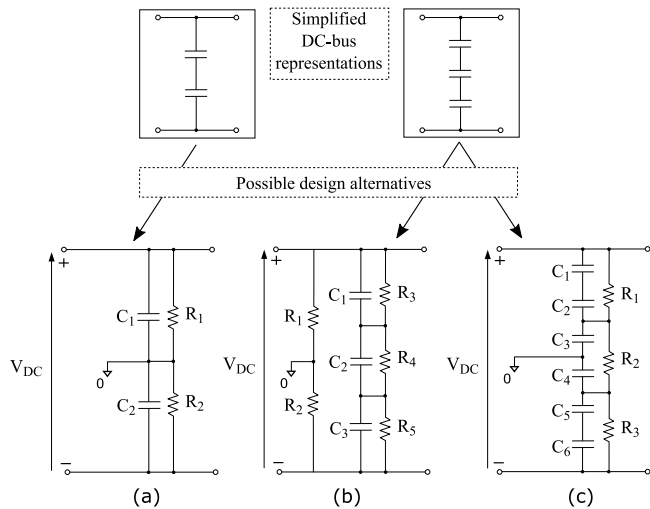


Fig. 15. Possible construction alternatives for the DC-bus depending on the number of capacitors: (a) two balanced capacitors; (b) three balanced capacitors and a resistive divider; (c) three balanced capacitances consisting of six capacitors.

topologies and modern modulation techniques are covered by the following two sections in greater detail.

### 3. Alternative converter architectures for common-mode voltage mitigation

There are various approaches when reducing CMV through converter topologies. On the one hand, it is possible to use multilevel or multiphase converter topologies instead of the conventional VSI, since they provide additional degrees of freedom. Indeed, they make it possible to obtain improved CMV waveforms or even a complete elimination of CMV variations through specific modulation techniques [40,110–112]. On the other hand, it is possible to add extra hardware components to the conventional three-phase converter (recall Fig. 6) that provide new functionalities. This paper focuses on the latter approach, where there are two options to reduce the CMV on a conventional two-level three-phase inverters: (i) adding passive reactances together with modified PWM techniques [113,114]; or (ii) adding more switches, providing the inverter with more degrees-of-freedom [106,115]. However, these last solutions may also require special DC-bus designs.

Sometimes, different DC-bus access points may be necessary to distribute the total voltage among several capacitors: for example, it is usual to have to split the DC-bus in two halves, setting the voltage reference point in the middle of the bus. This fact is modeled by means of two equal capacitors that are generally balanced with two equal resistors (Fig. 15(a)). Another possible scenario is a DC-bus with three balanced capacitors, requiring access to their midpoint. There, a two-resistor divider can be implemented beside a three-capacitor set (Fig. 15(b)), or also six-capacitor string, which gives access to all the required voltage levels (Fig. 15(c)). These ideas must be kept in mind when designing the converter, although in all the topologies discussed below the representation of the bus has been simplified for the sake of clarity (Fig. 15, top).

Particularly, in what follows the DC-bus middle point will be regarded to be the voltage reference ground. Moreover, Fig. 16 summarizes the two-level three-phase inverter architectures resulting from all these modifications, where three main families can be distinguished: (1) impedance source inverters, with the Z- and Quasi-Z-source structures (ZSI and QZSI, respectively); (2) DC-decoupled inverters, with the so-called H7 and H8 subfamilies; and (3) AC-decoupled inverters, with the so-called VSIVZR subfamily, and the ‘High Efficient and Reliable Inverter Concept’ (HERIC) structure.

### 3.1. Impedance-source inverters

Impedance-source architectures have interesting features for reducing CMV variations. The use of these topologies has been proposed in the scientific literature for both photovoltaic [116–118] and drive systems [107,119,120]. As Fig. 17 shows, the Z-Source Inverter (ZSI) and Quasi-Z-Source Inverter (Q-ZSI) are the two most employed architectures. They have two operation modes: non-shoot-through (NST) and shoot-through (ST). In the former, six active states and two zero states are applied as in the traditional VSI; whereas in the latter both switches of the same branch can conduct simultaneously, in at least one phase [117]. In more detail:

(a) **ZSI.** Fig. 17(a) shows this architecture, which incorporates an X-shaped impedance source network coupled between the DC-voltage source and the inverter. The inverter is then no longer called ‘voltage-source’ but ‘impedance-source’. This impedance typically comprises two identical capacitors and inductors [116,121,122]. In addition, to guarantee the DC-link isolation from the inverter switches during the ST states, a fast recovery diode ( $D_1$ ) is added.

Its main advantage is that two semiconductors of the same leg can be switched on together without the voltage-source having a short-circuit. Therefore, there is no need to introduce deadtimes, which improves the output current distortion and system reliability [121]. In addition, the Z-network intrinsically allows stepping down or up the DC-source voltage (buck/boost), so additional DC-DC converters could be avoided [122]. This is especially interesting in applications where the source voltage has large variations [48], because it reduces costs and increases the overall efficiency [118].

One of the main disadvantages of the ZSI architecture is that the voltage across the Z-source capacitors equals the voltage of the DC source. Thus, high-voltage capacitors must be used which may result in larger volume and, consequently, increased system cost [121]. Moreover, with regard to the modulation techniques, there is an interdependence between the boost factor ( $B$ ) and the modulation index, which are considered the control parameters of the Z-source gain of the ZSI architecture. This interdependence causes a conflict on the output power quality and on the system boost capability [122].

In any case, the existence of these ST states within the switching periods causes the high-frequency harmonics to shift to higher frequencies than in conventional voltage-source inverters, which worsens the CMV waveform. Voltage levels also are different; see Table 2 [113]. In other words, ZSI architecture-based inverters do not reduce CMV levels by themselves; instead, specific modulation techniques are required for this, which, on the other hand, are able to not only reduce but also completely eliminate the CMV variations [116,118].

(b) **Q-ZSI.** Fig. 17(b) shows this variation of the ZSI architecture, which provides some extra advantages. First, the new arrangement of diode  $D_1$  allows the energy to flow in both directions [107]. Second, the buck/boost function is carried out more reliably than by the ZSI [117]. Third, it provides a wider voltage gain range [123], with the advantage that the boost control methods developed for the ZSI can all be used by the Q-ZSI too [117]. Fourth, Q-ZSI components suffer less stress than ZSI components [48,114]. Fifth, the Q-ZSI draws a continuous constant DC current from the source, whereas the ZSI draws a discontinuous current [117,123], thus greatly reducing the voltage on  $C_2$  (Fig. 17(b)).

The disadvantages of the Q-ZSI are similar to those of the ZSI. In particular, the interdependence between the boost factor and the modulation index remains the same as for the ZSI. Thus, in order to maximize the voltage gain and minimize the voltage stress of the inverter,  $B$  should be decreased and  $M_a$  should be increased as much as possible [117].

Finally, like the ZSI, the Q-ZSI allows reducing the CMV by applying modifications to the SV-PWM technique [48,114]. Moreover, the CMV levels produced in each switching state are different from those produced by the ZSI (see Table 2). So again, the Q-ZSI requires a special modulation technique to reduce the CMV.

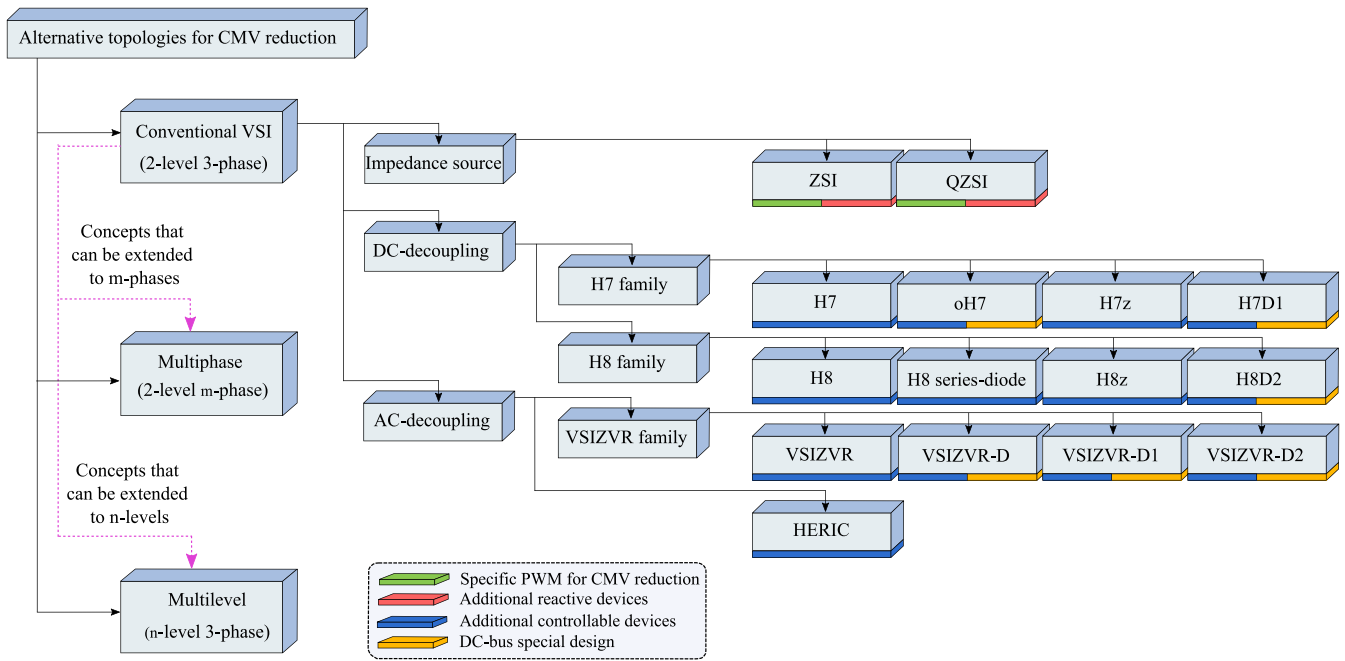


Fig. 16. Applicable inverter topologies to drive systems for CMV reduction discussed in this section.

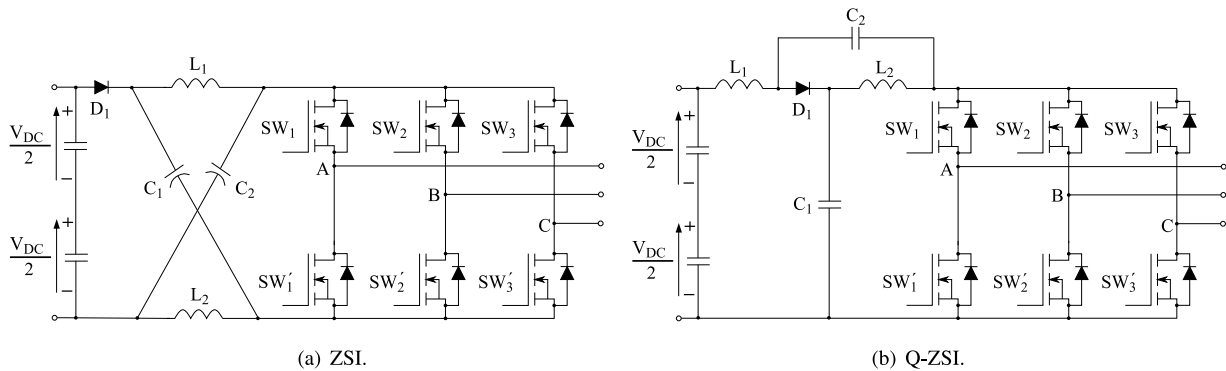


Fig. 17. Two-level three-phase impedance-source topologies.

### 3.2. DC-decoupling inverters

Decoupling strategies are more attractive than impedance-source strategies for CMV reduction due to its simplicity of implementation, among other benefits. Since according to (3) zero vectors are the ones that produce the highest CMV levels, the objective of these topologies is to decouple the power circuit during the application of such vectors. For DC decoupling architectures, these decouple the voltage source from the load when the modulation algorithm applies the zero vectors [42,124]. Among these converters, the most relevant are:

(a) *H7 family*. CMV reduction is one of the most important issues for transformerless PV grid-connected inverters, where a large number of single-phase topologies have been proposed to reduce this voltage [43]. Inspired by the existing single-phase topologies, such as the H5 or oH5 [43,125], their three-phase equivalents have been proposed for this applications: H7 (Fig. 18(a)) and oH7 topologies (Fig. 18(b)) [42, 124,126]. However, the use of these topologies is not limited to photovoltaic systems — they have also been proposed as alternatives for applications with electric machines [84,85,106]. One of these H7 topology variant incorporates a Zener diode connected in antiparallel with the DC side additional switch (Fig. 18(c), H7z) to reduce CMV to a greater extend [84]. Furthermore, the H7D1 topology (Fig. 18(d))

has been proposed, which achieves the same CMV reduction by just replacing the additional active device of the oH7 topology with a diode [106].

Table 2 summarizes the main features of this family of converters. Overall, its major advantage is that the additional  $SW_{DC1}$  device (Fig. 18) provides an additional degree-of-freedom which can be leveraged to reduce the CMV. Apart from this, each variant has its own particularities: for example, the oH7 and the H7D1 eliminate an extra level of CMV thanks to a clamping device [106]. In turn, the H7z can achieve the same if a suitable Zener diode is used for this purpose. Thus, when the additional switch is turned off, the DC-link voltage is blocked by the breakdown voltage of the Zener diode [84].

The main disadvantage of this family of converters is the increased conduction losses incurred by the additional active device, which is connected in series with the DC-source. In addition, the oH7 makes the control more complex due to the addition of an extra active device, when the same results can be achieved with just a clamping diode. Finally, the Zener diode of the H7z must be carefully selected.

(b) *H8 family*. As with the H7 family, the extension of the H6 single-phase inverter [43,127] for photovoltaic applications gave rise to the H8 family. Its main feature is the incorporation of two active DC-decoupling switches (Fig. 18,  $SW_{DC1}$  and  $SW_{DC2}$ ) that are used during

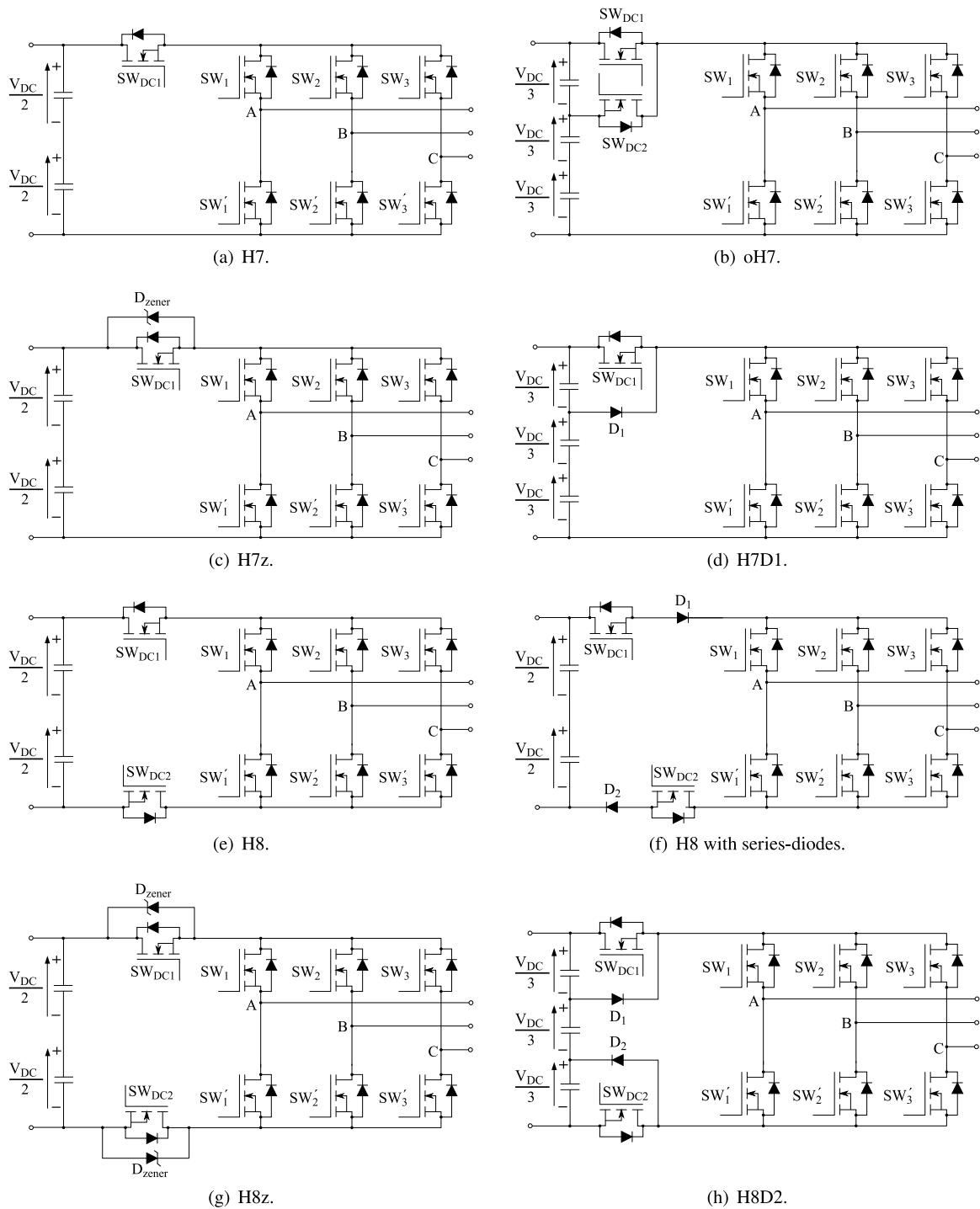


Fig. 18. Two-level three-phase DC-decoupling topologies.

the application of zero vectors [41,124,126,128], but not all of the H8 family topologies reduce the CMV to the same extent; see Table 2.

The baseline architecture is the H8 (Fig. 18(e)) [41,124], after which the family is named. However, there are other variants such as the H8 with series-diodes [152], the H8z [129], and the H8D2 [130]; see Figs. 18(e)–18(h). This latter H8D2 has been proposed for applications beyond photovoltaics, such as industrial drives [48], HEV/EVs [115] and MEA [131].

Again, each family member has its particularities. The H8z and the H8D2 allow a greater CMV reduction. In the H8z the magnitude of CMV during the zero vectors can be adjusted by selecting the appropriate

breakdown voltage of Zener diodes, i.e. by turning off the series-connected switch, thus blocking the DC-bus voltage [129]. The H8D2 has a voltage divider consisting of three balanced capacitors and two clamping diodes, which allow the desired voltage to be set on the load terminals over the zero vector application interval [48,126]. In this way, the clamping diodes are activated only for a short time, thus charging and discharging the stray capacitance of the semiconductor devices, and ensuring that the  $+V_{DC}/3$  or  $-V_{DC}/3$  voltage levels (Fig. 18(h)) are applied in  $v_{CM}$  (3) during the application of zero vectors [48].

On the downside, the H8 and H8 with series-diodes do not allow controlling the CMV level during zero vectors. One possible solution

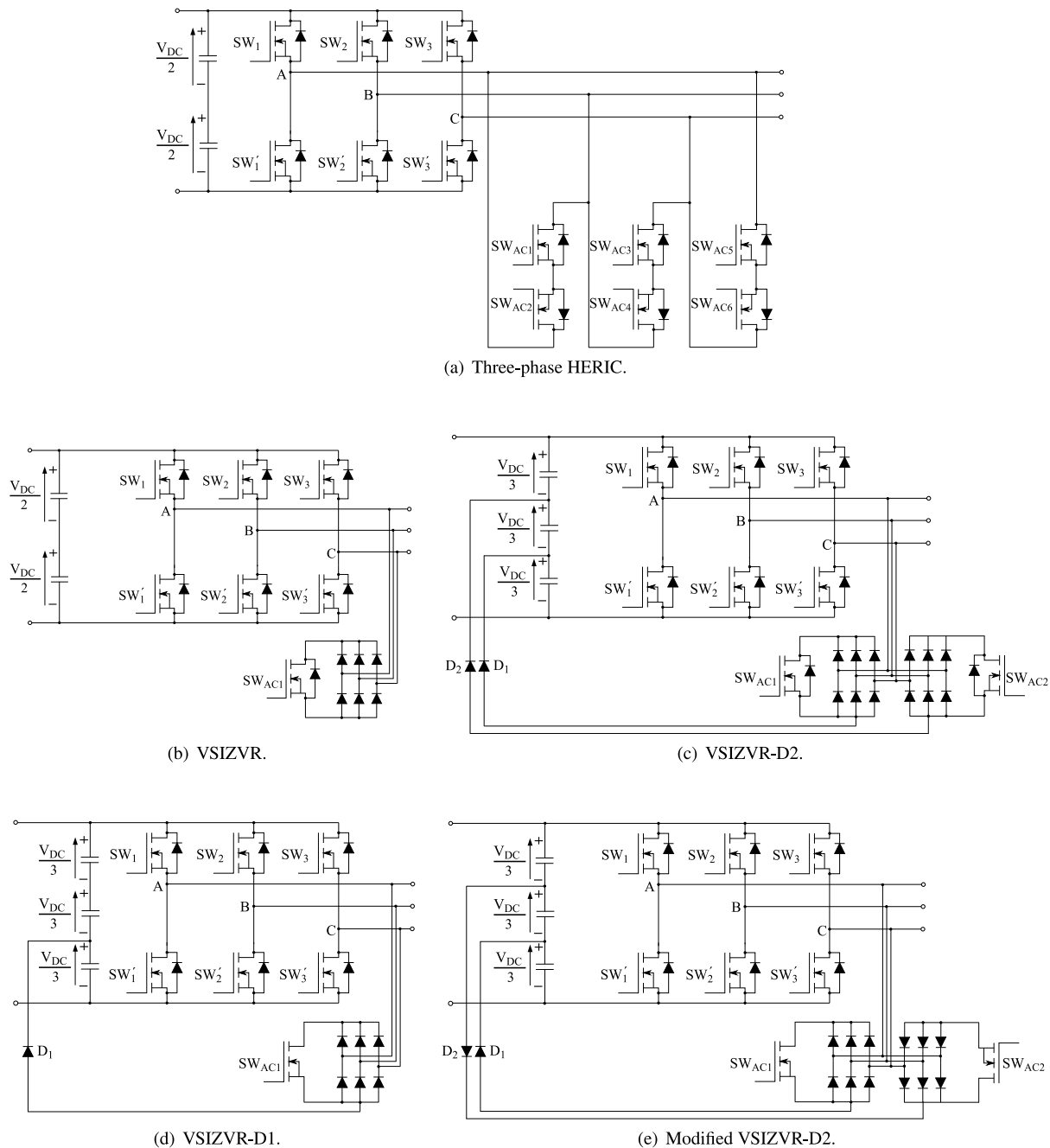


Fig. 19. Two-level three-phase AC-decoupling topologies.

is to use either of the other two alternatives (H8z or H8D2). However, blocking the corresponding DC-bus voltage can be easier with clamping diodes than with Zener diodes. Furthermore, all these topologies have a general additional drawback: the increased conduction losses. By incorporating additional devices connected in series with the DC-source, conduction losses are considerably increased. So these topologies should be selected for those applications with motor drives where CMV reduction, even at the cost of lowering the efficiency, is the main purpose.

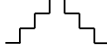
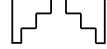


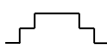

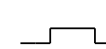

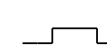
3.3. AC-decoupling topologies

Fig. 19 shows the most common AC-decoupling architectures, which use additional hardware to disconnect the inverter from the load when

the modulation algorithm applies a zero vector. As a result, as in DC-decoupling strategies, the CMV levels produced by the zero vectors are eliminated. Among these strategies, the following can be highlighted:

(a) *HERIC converter.* This is by far the most commonly referenced single-phase AC-decoupling architecture [43,132,133]. It stands for ‘High Efficient and Reliable Inverter Concept’, a well-known converter for transformerless systems. It consists of a full bridge inverter with an AC-bypass leg parallel to the output [134]. This design is able to produce constant CMV, and therefore, very low ground leakage current and EMI.

**Table 2**  
Characteristics of the main three-phase topologies for CMV reduction.

		Impedance source			DC-decoupling				AC-decoupling	
		VSI Fig. 6	ZSI <sup>c</sup> Fig. 17(a)	QZSI Fig. 17(b)	H7 Fig. 18(a)	H7z <sup>d</sup>   H7D1 Figs. 18(c)–18(d)	H8 <sup>d</sup> Fig. 18(e)	H8z <sup>d</sup>   H8D2 Figs. 18(g)–18(h)	VSIZVR-D1 <sup>f</sup> Fig. 19(d)	VSIZVR-D2 <sup>f</sup> Fig. 19(e)
Hardware	• Switches	6	6	6	7	7	8	8	7	8
	• Diodes	0	1	1	0	1	0   2 <sup>e</sup>	2	7	14
	• Capacitors	0	2	2	0	0	0	0	0	0
	• Inductors	0	2	2	0	0	0	0	0	0
	• Voltage sources	0	0	0	0	0	0	0	0	0
CMV-related data	$V_0$	$-V_{DC}/2$	$(1-2B)V_{DC}/2$	$-V_{DC}/2$	$V_{DC}/6$	$-V_{DC}/2$	$V_{DC}/4$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$
	$V_{Odd}$	$-V_{DC}/6$	$(1-2B)V_{DC}/6$	$(2B-3)V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$
	$V_{Even}$	$V_{DC}/6$	$(2B-1)V_{DC}/6$	$(4B-3)V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$
	$V_7$	$V_{DC}/2$	$(2B-1)V_{DC}/2$	$(2B-1)V_{DC}/2$	$-V_{DC}/4$	$V_{DC}/6$	$-V_{DC}/4$	$V_{DC}/6$	$-V_{DC}/6$	$V_{DC}/6$
	$V_{ST}$ <sup>a</sup>	$\times$	$(2B-1)V_{DC}/2$	$-V_{DC}/2$	$\times$	$\times$	$\times$	$\times$	$\times$	$\times$
	$\Delta_p$	1	$2B-1$	$2B-1$	2/3	2/3	1/2	1/3	1/3	1/3
	$\Delta_S$	1/3	$(2B-1)/3$	$(2B-1)/3$	1/3	1/3	1/3	1/3	1/3	1/3
	$N_L$	4	4	4	3	3	4	2	2	2
	$N_T$	6	8	8	6	4	6	2	4	2
	• CMV waveform with SV-PWM									
Required changes	• Clamping included	No	No	No	No	No   Yes	No	No   Yes	Yes	Yes
	• Modified DC-bus	No	No	No	No	No   Yes	No	No   Yes	Yes	Yes
	• Buck-boost function	No	Yes	Yes	No	No	No	No	No	No
	• Bidirectional energy flow	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	• Special PWM for CMV reduction	No	Yes	Yes	No	No	No	No	No	No
	• Simultaneous switching per phase	No	Yes	Yes	No	No	No	No	No	No
Performance	• Efficiency		≈	≈	↓	↓	↓↓	↓↓	↓↓	↓↓
	• Conduction losses		≈	≈	↓	↓	↓↓	↓↓	≈	≈
	• Switching losses	Performance	≈	≈	≈	≈	≈	≈	↓↓	↓↓
	• CMV	regarding	≈	≈	↑	↑↑	↑	↑↑↑	↑	↑↑↑
	• Power density	the VSI (using:	↓↓↓	↓↓↓	≈	≈	≈	≈	↓	↓
• Robustness against $V_{DC}$ drop	≈, ↓ and ↑ <sup>b</sup>	↑	↓	≈	≈	≈	≈	≈	≈	
References		[116,122]	[117,123]	[42,85]	[84,106]	[41,124]	[106,115]	[106]	[106]	

<sup>a</sup> $V_{ST}$  is the vector associated with the shoot-through states.  $\times$  means that the switching combination is not allowed in that converter.

<sup>b</sup>The performance of each topology is valued qualitatively regarding the VSI: ≈ means similar to the VSI; ↑ means better than the VSI; and ↓ means worse than the VSI. For all the cases, the number of ↑ and ↓ means to a greater or lesser extent.

<sup>c</sup>B is the boost factor of the impedance network of the inverter.

<sup>d</sup>When the value is different for one or the other it is differentiated separated by “|”.

<sup>e</sup>Only on H8 with series-diodes.

<sup>f</sup>This topology has the possibility of obtaining the same performance as the VSI, if it is operated as VSI without using the additional elements.



Fig. 19(a) shows the three-phase extension of the HERIC [106]. However, in terms of CMV mitigation, the HERIC is far from being a good candidate: a great number of additional active devices would be required to effectively eliminate the CMV. To operate it would be very complicated: to eliminate the highest levels of CMV, all the devices of the inverter stage must be turned off and all the devices of the AC-bypass must be turned on, thereby increasing the switching losses significantly.

(b) *VSIZVR family.* Despite many transformerless single-phase converters for photovoltaic applications have been proposed to reduce CMV, three-phase PV AC-decoupling inverter architectures with reduced CMV have not been deeply explored. Figs. 19(b)–19(c) show the solutions proposed to fill this gap, namely, the so-called VSIZVR and VSIZVRD designs [135,136]. The idea of both inverters comes from the single-phase H-bridge Zero-voltage Rectifier (HBZVR). In this sense, the VSIZVR incorporates a rectifier circuit connected to the converter output phases, which allows the load to be decoupled during the application of zero vectors [135]. Similarly, the VSIZVR-D2 incorporates two rectifier circuits connected to the DC-bus by means of two clamping diodes [136].

Because these two designs turn out to have certain limitations for CMV reduction, other two additional three-phase alternatives for electric traction applications are presented: VSIZVR-D1 and modified VSIZVR-D2 (Figs. 19(d)–19(e), respectively) [106]. These converter designs incorporate a capacitive divider on the DC-bus, with one or two diode rectifiers and one or two clamping diodes ( $D_1$  and  $D_2$ ). Observe that both VSIZVR-D1 and VSIZVR-D2 prevent the current from passing through the antiparallel diode of the switch of the rectifier-bridge; as a result, this diode can be dispensed with, depending on the device chosen.<sup>8</sup>

The main advantage of the VSIZVR family is that the CMV can be reduced without hindering the efficiency of the converter, since, unlike DC-decoupling topologies, these converters do not incorporate active devices in series that increase the conduction losses. Besides, if necessary, additional hardware can be dispensed with, and the converter works exactly the same as the conventional VSI.

Regarding the disadvantages, in general for the VSIZVR family, CMV reduction PWM techniques need more than one commutation per phase and per  $T_{SW}$ , which increases switching losses. Besides, these topologies can increase in size, due to the large number of devices they incorporate.

Finally, although each of the topologies in this family has its particular advantages and disadvantages, the VSIZVR does not reduce the CMV as much as the rest, since it does not incorporate clamping diodes. The VSIZVR-D2 cannot control the CMV level when the right side rectifier is activated. Therefore, to achieve a correct performance of this converter, it is necessary to employ the modified VSIZVR-D2 design; otherwise, the same results as in VSIZVR-D1 design would be obtained.

Table 2 summarizes the characteristics, the advantages and disadvantages, the CMV levels generated by the main topologies studied, as well as the resulting waveform for each switching period when SV-PWM is applied. Note that the CMV waveforms shown in the table could be further reduced by replacing SV-PWM with some specific CMV reduction modulation techniques [48]. For that purpose, Section 4 reviews CMV reduction modulation techniques that can be applied on these three-phase converters.

<sup>8</sup> MOSFETs have a silicon-integrated body diode that allows current to flow in the opposite direction. However, although most IGBTs currently also have an antiparallel diode, they might not have such a diode intrinsic in the device.

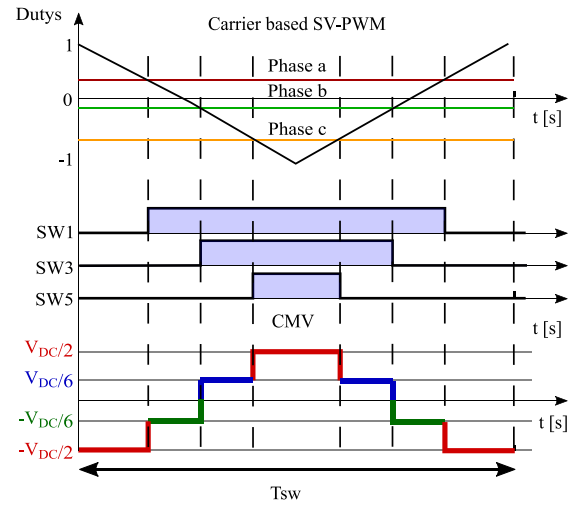


Fig. 20. CMV generated by min–max injection modulation.

## 4. Advanced modulation techniques for common-mode voltage reduction

### 4.1. Carrier-based vs space-vector approaches





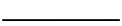
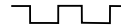

PWM can be synthesized by following either carrier-based (CB) or space-vector (SV) approaches [137]. The former are relatively simple to implement: may use sinusoidal as well as nonsinusoidal modulating waves, together with triangle- or sawtooth-shaped carriers, and inject zero-sequence signals. The latter are more resource intensive, so they started becoming popular in the beginning of this century, along with the introduction of digital signal processing (DSP) devices [138]. Anyway, because any SV-PWM-based modulation technique can also be implemented by following the CB approach,<sup>9</sup> the CMV waveform produced by a given modulation scheme does not depend on whether it was originally devised as CB or SV. Indeed, Fig. 20 shows how the CB approach, which is called ‘min–max injection’ modulation, can give rise to the SV-PWM pattern [76]. Note that the resulting CMV waveform is the same appearing in Fig. 7. The same rationale applies to other well-known modulations originally conceived as CB, such as third-harmonic-injection PWM (THI-PWM) [139,140]. However, when compared to pure sinusoidal PWM, in min–max injection and THI-PWM algorithm the CMV levels produced are considerably increased by the zero-sequence signals added to the modulator signal. This occurs because the frequency of the zero-sequence signal results three times as high as that of the reference sinusoid, which makes the third harmonic of the CMV waveform increase accordingly [111].

CB-PWM variants exist that do reduce the CMV [112]; some of these techniques are: (i) carrier phase shift PWM (CPS-PWM), which uses one carrier for each modulator signal [141]; (ii) carrier peak position modulation (CPPM), which varies the position of the peak of the carrier signal to avoid zero-voltage states [142]; (iii) rotation reverse carriers scheme, where carrier frequency modulation is leveraged [143]; and (iv) third harmonic injection sinusoidal pulsewidth modulation (THISPWM), which alternates the polarity of the carrier wave [144].

Another fruitful CB-PWM way to decrease the CMV is to do it through the reduction of the switching losses, which ultimately lowers  $N_T$ . The so-called ‘discontinuous’ (D-PWM) techniques come into play here, several of which are well known, such as D-PWMMIN [139], D-PWMMAX [140], D-PWM1 [145], D-PWM2 [145], D-PWM0 [140] and D-PWM3 [140].

<sup>9</sup> An in-depth study has been made about the relationship between CB and SV techniques in [111].

**Table 3**  
 Characteristics of the main SV-based PWM techniques for CMV reduction compared to conventional SV-PWM.

	SV-PWM Fig. 7	Discontinuous-PWM techniques			RCMV-PWM techniques			Other techniques
		D-PWM Fig. 21	MD-PWM Fig. 21	AZS-PWM Fig. 22	RS-PWM Fig. 24	NS-PWM Fig. 25	CCMV-PWM Fig. 26	
Linear range	$0 \leq M_a \leq 1.15$	$0 \leq M_a \leq 1.15$	$0 \leq M_a \leq 1.15$	$0 \leq M_a \leq 1.15$	$0 \leq M_a \leq 0.66$	$0.77 \leq M_a \leq 1.15$	$0 \leq M_a \leq 0.66$	
Voltage vectors used	All vectors	All vectors	All except $V_0$	Active vectors	Even/Odd vectors	Active vectors	Even/Odd and zero vectors	
Vector sequences	• Sector 1	0127210	72127	72127	6123216	31513	21612	10301
	• Sector 2	0327230	23032	23732	4321234	31513	32123	30103
	• Sector 3	0347430	74347	74347	2345432	31513	43234	30503
	• Sector 4	0547450	45054	45754	6543456	31513	54345	50305
	• Sector 5	0567652	76567	76567	4561654	31513	65456	50105
	• Sector 6	0167610	61016	61716	2165612	31513	16561	10501
CMV-related data	• CMV figures-of-merit							
	$\Delta_p$	1	2/3	2/3	1/3	0	1/3	1/3
	$\Delta_s$	1/3	1/3	1/3	1/3	0	1/3	1/3
	$N_L$	4	21/6 <sup>b</sup>	3	2	1	2	2
	$N_T$	6	4	4	6	0	4	4
	• CMV waveform in the conventional VSI							
Performance	• Efficiency		↑	↑	≈	↓	↑	↑
	• Conduction losses	Performance regarding	≈	≈	≈	≈	≈	≈
	• Switching losses	SV-PWM (using:	↑	↑	≈	↓	↑	↑
	• CMV	≈, ↓ and ↑) <sup>a</sup>	↑	↑	↑	↑↑↑	↑↑	↑↑
	• $THD_c$		↓	↓	↓↓↓	↓↓↓	↓↓↓	↓↓
	• Linear range		≈	≈	≈	↓	↓↓	↓
References	[48]	[42,124,128]	[42,124,128]	[42,124,146]	[60,124,147]	[42,60,124]	[48,115,131]	

<sup>a</sup>The performance of each topology is evaluated qualitatively using SV-PWM technique as a reference: ≈ means similar to SV-PWM; ↑ means better than SV-PWM; and ↓ means worse than SV-PWM. For all the cases, the number of ↑ and ↓ means a greater improvement/worsening.

<sup>b</sup>As the amplitude of the CMV changes depending on the sector in which it is applied, the average of  $N_L$  is provided to notice the difference with MD-PWM.

However, when the goal is to modify a given PWM pattern to reduce its CMV output, it is advantageous to work by following the SV-PWM approach. Indeed, the Space Vector frame provides a higher abstraction level, which makes it easier to relate the CMV figures-of-merit with the design parameters of the modulation algorithm. For example, it is straightforward to avoid using zero-voltage vectors, which are known to cause the largest CMV levels [148,149]. Three main contenders stand out here: (i) active zero-state PWM (AZS-PWM) [146,150,151]; (ii) remote-state PWM (RS-PWM) [147]; and (iii) near-state PWM (NS-PWM) [152]. Together, these three constitute the family of ‘reduced CMV’ PWM (RCMV-PWM) techniques, which deserves a closer look. But before that, a brief review of D-PWM variants follows, highlighting the ‘baseline’ D-PWM and the modified discontinuous (MD-PWM). In addition, the relationship between modulations and alternative converter topologies is explained at the end of the section, highlighting the ‘constant CMV’ (CCMV-PWM) technique at this point.

Table 3 summarizes all the features of these techniques and compares them with the SV-PWM technique, to highlight their strengths and weaknesses.

#### 4.2. Discontinuous PWM techniques

Unlike SV-PWM, D-PWM and MD-PWM techniques only use one zero vector in addition to two adjacent active vectors per modulation period (Fig. 21(a)). As a consequence, these techniques have the advantage of keeping the same linear range as SV-PWM, while reducing power losses. Fig. 21(b) illustrates the largest synthesizable reference vector that can be achieved by applying discontinuous modulation techniques, which results in  $|V_{ref}|_{max} = 0.58V_{DC}$  and  $M_a \in [0, 1.15]$ .

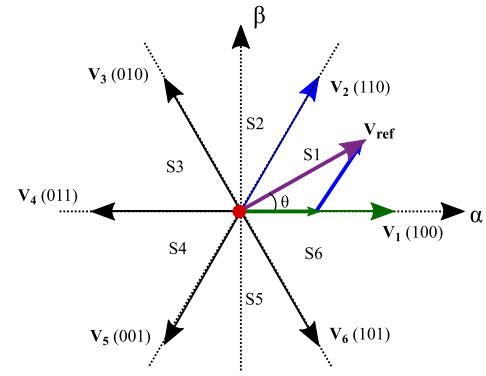
Likewise and regarding CMV,  $N_T$  is reduced due to the less number of vector transitions (Fig. 21(c)). Furthermore, although  $\Delta_p$  is the same for D-PWM and MD-PWM techniques, depending on the modulation sequence, CMV levels may vary between  $-V_{DC}/6$  and  $+V_{DC}/2$  or between  $-V_{DC}/2$  and  $+V_{DC}/6$ . Fig. 21(c) shows the latter case, where there are fewer vector transitions, since vector  $V_0$  is not used. In D-PWM different zero vectors are used for each sector ( $V_0$  or  $V_7$ ) and therefore there will be different CMV waveforms (see Table 3). In contrast, smaller CMV levels result in MD-PWM, since it always uses the same zero vector. In exchange, MD-PWM increases the switching losses when compared with D-PWM.

Although these techniques do not reduce CMV as much as the RCMV-PWM family, they are of great importance since they are multi-objective techniques. That is, they reduce CMV and, at the same time, they do not penalize efficiency as much as RCMV-PWM strategies do. Anyway, NS-PWM could also be classified within this type of techniques, and the same goes for CCMV, which are explained below.

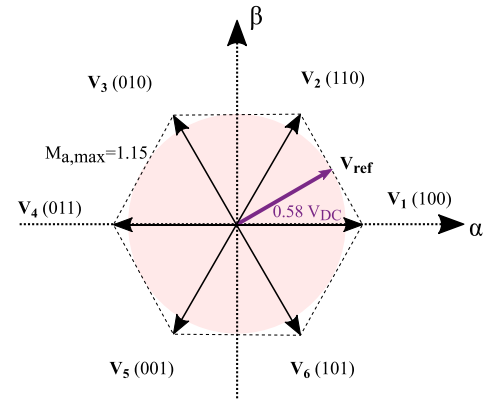
#### 4.3. RCMV-PWM techniques

##### 4.3.1. AZS-PWM

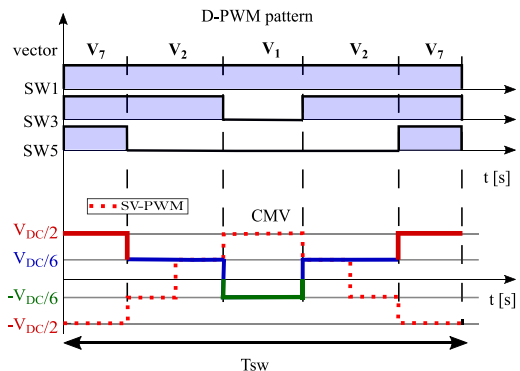
In place of zero vectors, AZS-PWM uses phase-opposite active vectors, each applied during  $t_0/2$  (where  $t_0$  is the application time of a zero vector). However, active vector application time to generate  $V_{ref}$  is calculated as in SV-PWM [148]. To illustrate this, Fig. 22(a) shows how  $V_{ref}$  is synthesized when it lies in sector 1. In this case, phase-opposite vectors  $V_3$  and  $V_6$  are used to fulfill  $t_0$ , instead of the corresponding zero vectors. However, there is no single solution to choose the active vectors that replace the zero vectors (Fig. 23). For example, variants AZS-PWM1 and AZS-PWM2 reuse one of the active vectors used to synthesize  $V_{ref}$  (Figs. 23(a)–23(b)), whereas the AZS-PWM3 variant uses two additional active vectors (Fig. 23(c)). When switching between non-consecutive vectors, two switches must change their state, as occurs in AZS-PWM1 and AZS-PWM2. Nevertheless, all three alternatives have the same number of commutations per period. This happens because both AZS-PWM1 and AZS-PWM2 require two fewer vector transitions than AZS-PWM3 to fulfill the vector sequence.



(a) Synthesis of the reference vector  $V_{ref}$  in sector 1 by using a single zero vector.



(b) Linear range and maximum achievable voltage vector at the inverter output for D-PWM and MD-PWM techniques.



(c) Vector sequence and generated CMV waveform in sector 1.

Fig. 21. Vector representation of the D-PWM and MD-PWM techniques along with switching states and associated common-mode voltage levels.

Since any of the AZS-PWM variants use all the available active vectors, the linear range of this modulation is the same as in SV-PWM (Fig. 22(b) vs Fig. 7(b)). This provides this modulation with a significant advantage over the other RCMV-PWM algorithms [42,60, 128].

The CMV figures-of merit of this technique are  $\Delta_p = 1/3$  and  $N_L = 2$ , meaning that the CMV is reduced to values between  $-V_{DC}/6$  and  $+V_{DC}/6$  (Fig. 22(c)). However,  $N_T$  value varies from one AZS-PWM variant to another. For example, there is no improvement in AZS-PWM3 over SV-PWM. Likewise, in addition to increasing the commutations, the implementation of any AZS-PWM technique increases the voltage ripple

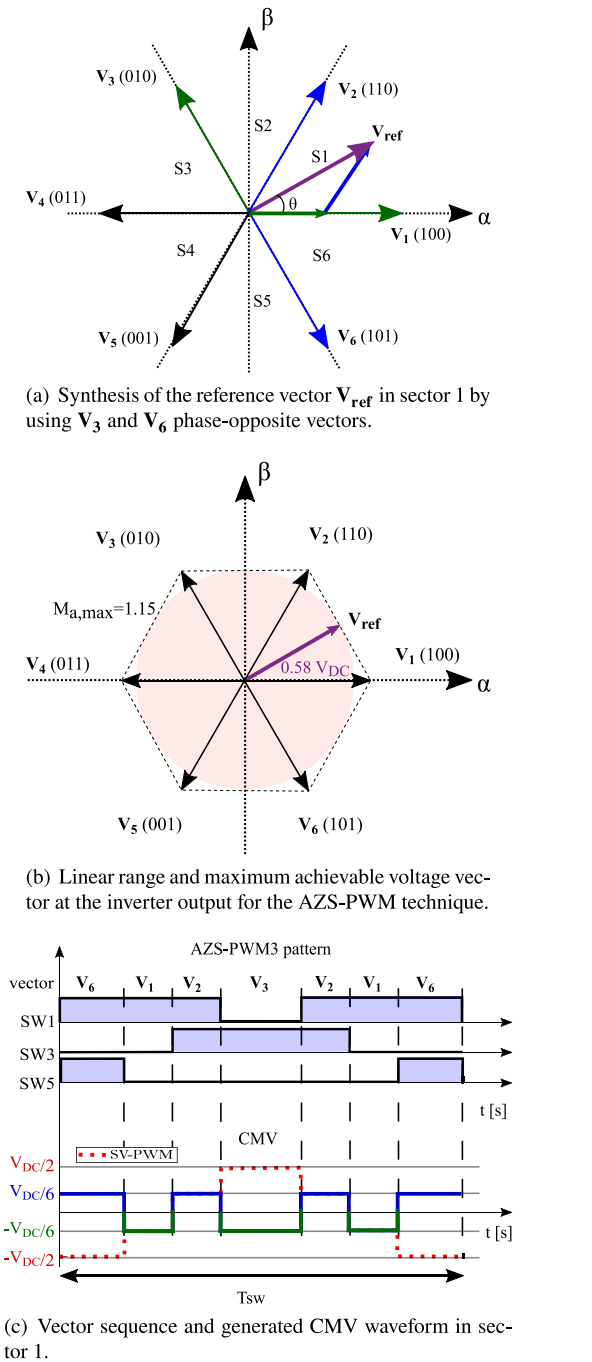


Fig. 22. Vector representation of the AZS-PWM technique along with switching states and associated common-mode voltage levels.

in the DC-bus capacitor and the total harmonic distortion of the output current ( $THD_c$ ) [112].

#### 4.3.2. RS-PWM

RS-PWM uses only even ( $V_2, V_4, V_6$ ) or odd ( $V_1, V_3, V_5$ ) active vectors. As a result, not only the use of zero vectors is avoided, but also vectors that generate the same CMV level are employed. In this technique, the  $\alpha\beta$ -plane is divided into three sectors, and all available vectors are used every modulation period ( $T_{SW}$ ) to synthesize  $V_{ref}$  (Fig. 24(a)) [149]. Therefore, and from the point of view of CMV reduction, in this particular case there is no need to propose modifications to the vector sequence.

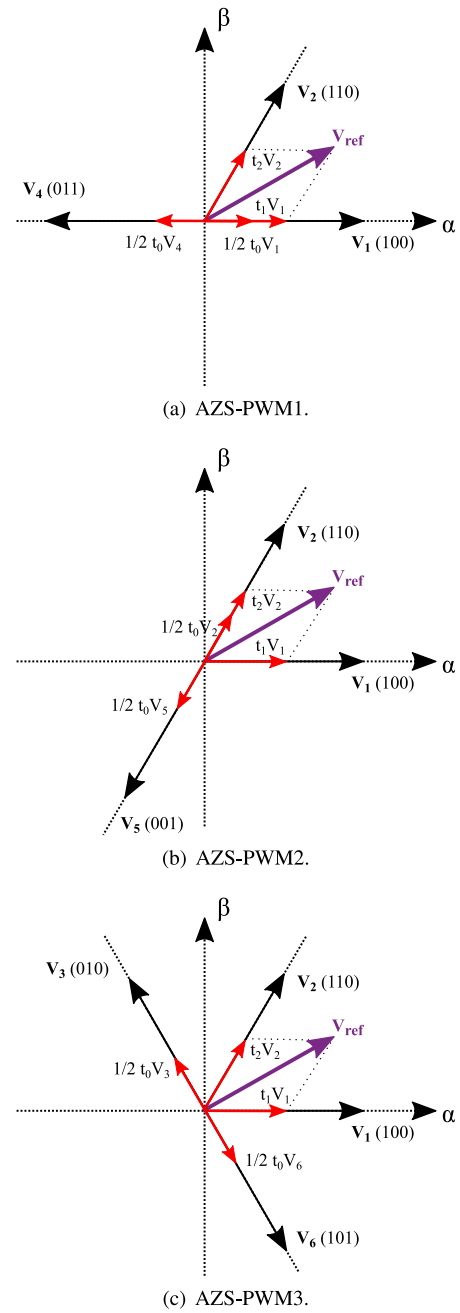
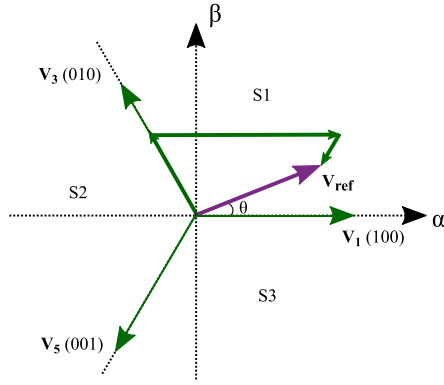


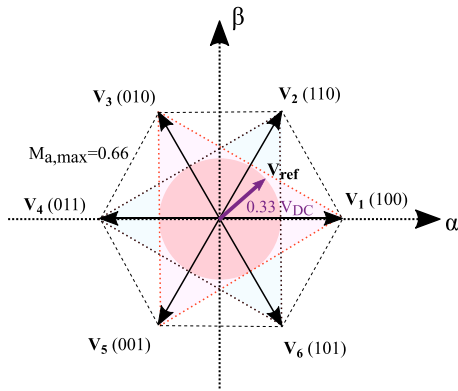
Fig. 23. AZS-PWM variants incorporating the different active vector combinations that can be used to avoid the application of zero vectors.

On the other hand, this technique has certain drawbacks (see Table 3). First, by switching only between odd or even vectors, the number of switchings per  $T_{SW}$  increases, thus reducing the efficiency of the converter. Second,  $THD_c$  worsens at the cost of a total elimination of the CMV variations. Third, the linear range of RS-PWM is greatly reduced, since  $|V_{ref}|_{max} = 0.33V_{DC}$  and, consequently,  $M_{a,max} = 0.66$ .

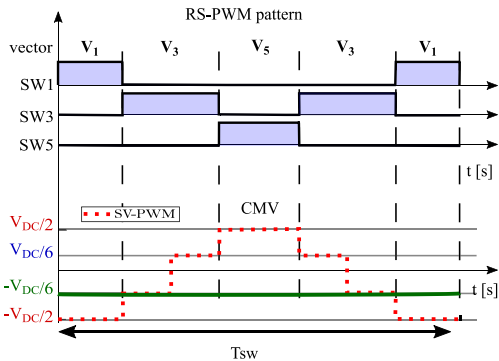
Fig. 24(b) shows the linear range (pink circle) obtained when using the RS-PWM technique, which lies inside the pink and green triangles created by odd and even vectors, respectively. A reduced linear range is an important drawback for various applications with drives, as in the case of electric vehicles where such a small linear range is not enough, since the entire linear range is required. To solve this problem, a variant of RS-PWM, named Modified RS-PWM has been proposed [149], which allows increasing the linear range up to 16 %.



(a) Synthesis of the reference vector  $V_{ref}$  in sector 1 by using all available odd vectors.



(b) Linear range and maximum achievable voltage vector at the inverter output for the RS-PWM technique.

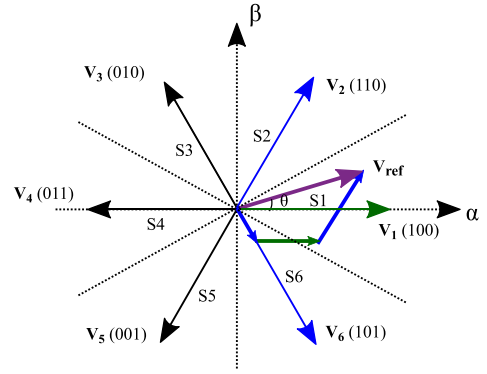


(c) Vector sequence and generated CMV waveform in sector 1 vs the one generated by SV-PWM (in red dashed).

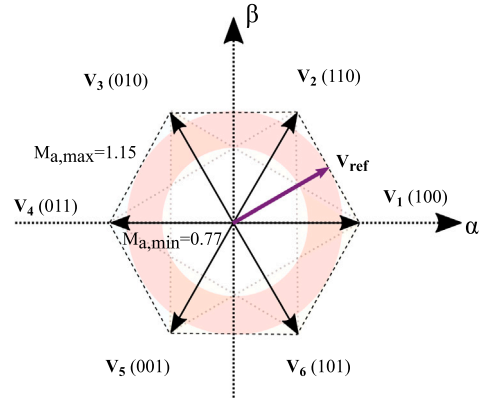
**Fig. 24.** Vector representation of the RS-PWM technique along with witching states and associated common-mode voltage levels. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

This technique divides the vector space into six sectors, and the use of odd and even vectors is alternated in each sector. Along this line too, a hybrid modulation, called MRS-SV-PWM, which combines MRS-PWM and SV-PWM has also been proposed [153]. As a result, the linear range can be maximized while leveraging the MRS-PWM technique under low modulation indexes.

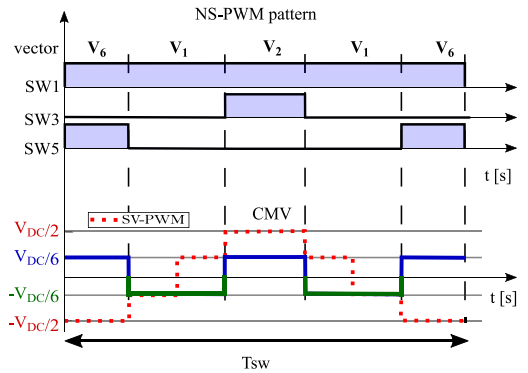
Regarding the CMV, as only vectors that produce the same CMV level are used, best results are achieved. Therefore,  $\Delta_p = 0$  and  $N_T = 0$ , which results in a constant CMV level (3) that equals  $+V_{DC}/6$  or  $-V_{DC}/6$ , depending on whether odd or even vectors are chosen (Fig. 24(c)).



(a) Synthesis of the reference vector in sector 1 using the closest vector and the adjacent two active vectors.



(b) Linear range and maximum achievable voltage vector at the inverter output for the NS-PWM technique.



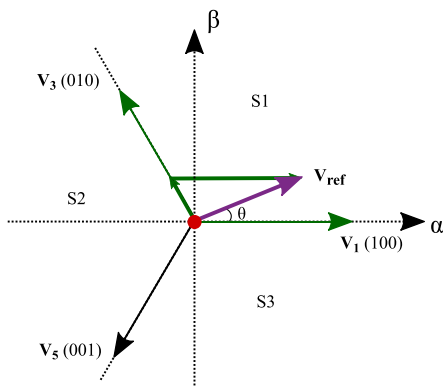
(c) Vector sequence and generated CMV waveform in sector 1 vs the one generated by SV-PWM (in red dashed).

**Fig. 25.** Vector representation of the NS-PWM technique along with witching states and associated common-mode voltage levels.

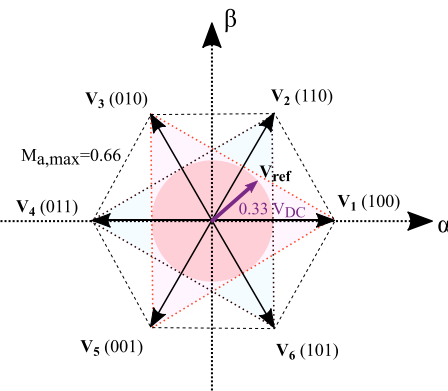
### 4.3.3. NS-PWM

When NS-PWM is implemented, the  $\alpha\beta$ -plane is divided into six sectors shifted  $30^\circ$  with respect to the SV-PWM space. Here, to synthesize  $V_{ref}$ , the closest vector and the adjacent two active vectors are used [154]; for example, when  $V_{ref}$  is in the first sector, the chosen vectors are  $V_6$ ,  $V_1$  and  $V_2$ . For illustration purposes, Fig. 25(a) shows how the reference vector is synthesized when using the NS-PWM technique.

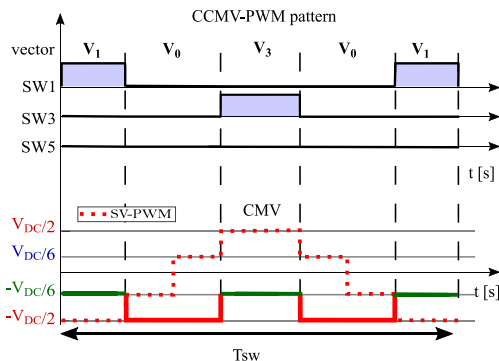
One of the main advantages of NS-PWM is that, in addition to reducing the CMV, it also reduces the switching losses [154]. This is because one of the branches of the converter does not change its state over a given switching period. That is, this technique can be



(a) Synthesis of the reference vector  $V_{ref}$  in sector 1 by using all odd vectors and a zero vector.



(b) Linear range and maximum achievable voltage vector at the inverter output for the CCMV-PWM technique.



(c) Vector sequence and generated CMV waveform in sector 1 vs the one generated by SV-PWM (in red dashed).

Fig. 26. Vector representation of the CCMV-PWM technique along with witching states and associated common-mode voltage levels.

also classified within the group of D-PWM algorithms [148,154]. On the downside, it is important to note that the linear range is reduced (see Table 3), the maximum achievable modulation index resulting  $M_a \in [0.77, 1.15]$  (Fig. 25(b)) [42,60]. Therefore, this technique must be combined with others, creating hybrid modulations, if it is to be applied in certain drive applications, such as traction, where the full linear range is required.

Finally, unlike AZS-PWM modulation, the variation of the order in which the vectors are applied does not represent a significant change in NS-PWM. Still, it is possible to apply a number of criteria. For example, when  $V_{ref}$  is in an odd-numbered sector, one can first apply the two even vectors to end with the odd one, and vice versa. In this way, it is

possible to further reduce  $N_T$ , at the cost of increasing the switching losses, since following these sequences two branches must change state to switch between two vectors. Conversely, if it is preferable to improve the efficiency, the CMV would be as shown in Fig. 25(c), with levels limited between  $-V_{DC}/6$  and  $+V_{DC}/6$  ( $\Delta_p = 1/3$ ).

#### 4.4. Combining converter topology and modulation

Different preventive actions can be combined to reduce the CMV, in fact, using special modulation techniques with modified two-level three-phase converter architectures is a common approach in the literature. For example, the CCMV-PWM technique has been proposed to obtain a constant CMV using the H8D2 converter topology [115].

The CCMV-PWM technique is similar to RS-PWM since it uses only odd or even vectors. As in RS-PWM, the  $\alpha\beta$ -frame is split into three sectors, depending on whether the odd or even vectors are used to form  $V_{ref}$  (Fig. 26(a)). Likewise, the linear range is also reduced ( $M_{a,max} = 0.66$ , Fig. 26(b)), as in RS-PWM [48]. On the other hand, and unlike RS-PWM (see Table 3), zero vectors are also used ( $V_0$  when using odd active vectors and  $V_7$  when even vectors are used, Fig. 26(a)).

Besides, Fig. 26(c) represents the time-domain CMV when applying the CCMV-PWM technique in a conventional two-level three-phase inverter. Here, CMV figures-of-merit are as follows:  $N_T = 4$  and  $\Delta_p = 1/3$ ; and CMV levels are limited to  $-V_{DC}/6$  and  $-V_{DC}/2$  using odd vectors, and to  $+V_{DC}/6$  and  $+V_{DC}/2$  when using even vectors. However, the results obtained when this technique is combined with other converter topologies such as the H8D2 or VSIZVR-D2 can be very beneficial in terms of CMV. For example, the H8D2 topology can be combined with CCMV-PWM and SV-PWM, depending on the modulation index [115]. Thanks to this, CMV variations can be eliminated when using CCMV-PWM and CMV can be reduced to low levels when SV-PWM is used. Another example is the combination of different modulation techniques in the VSIZVR-D2 topology to the extent of completely eliminating the CMV variations, by appropriately mixing it with CCMV-PWM [106].

In short, the combination of modulation techniques with converter topologies is not only limited to CCMV modulation, other combinations have been proposed too, such as the H7 topology with MD-PWM, which reduces the CMV and therefore the leakage currents [42], or using only odd or even vectors and the ST vector to reduce CMV and leakage currents with the Q-ZSI converter [123]. Therefore it can be affirmed that the combination of converter topology and modulation is an effective solution against the CMV problem, solving its possible derived-problems from the origin.

## 5. Conclusions

According to the reviewed literature, the utilization of electric machines and drives is continuously growing worldwide, particularly in the automotive sector. Due to the ongoing global push for e-mobility, a large number of hybrid and fully electric vehicles is expected in the coming years. In these vehicles, and in practically any modern electric drive system, PWM-driven voltage-source inverters provide the electric machine with the required AC power. However, unlike 'traditional' grid-connected machines, such inverters inherently produce high-frequency, large-amplitude common-mode voltage waveforms, unless specific design measures are taken. This can cause harmful consequences, such as high electromagnetic interference levels, damage to the machine stator windings, or even pitting of the bearings, which may ultimately lead to system breakdowns. Reviewed reports indicate that the latter is an important source of failures in electric drives. Thus, the search for solutions to either alleviate these consequences (corrective actions) or to reduce or even completely eliminate the CMV before it produces further issues (preventive actions) is receiving great attention.

This work has conducted a comprehensive review of the corrective and preventive actions that can be considered for CMV induced issue mitigation in electric drives. As a summary, the following general and particular conclusions can be derived from the conducted analysis:

1. Although it is possible to consider well-established corrective solutions such as Faraday shielding or the application of conductive grease, neither these or other reviewed corrective actions such as insulated bearings, ceramic bearings, grounding cable, brushes, etc. provide a definitive solution. The selection of the most suitable corrective solution will depend on the particularities of each electric drive and application, and it will be necessary to consider, in each case, the advantages and disadvantages of each approach.
2. In general, it can be concluded that preventive actions are more advantageous from the CMV perspective than the aforementioned corrective actions, since they allow solving the CMV problem from the origin.
3. With respect to preventive solutions, it has been verified that the interest of the scientific community and the industry on adopting alternative converter topologies that reduce CMV variations has increased. Among them, multilevel and/or multiphase configurations are being investigated, as they provide additional degrees of freedom when compared to conventional two-level three-phase inverters. A convenient exploitation of such degrees of freedom permits to synthesize the commanded output voltages while simultaneously reducing CMV.
4. Other alternative topologies to the conventional two-level three-phase VSI incorporating additional hardware elements that can be effectively used for CMV reduction have been widely researched in the literature. A variety of solutions have been proposed, from industrial drives, wind power or traction drives to applications that do not necessarily include electric machines, such as photovoltaic systems. Among them, this work has reviewed impedance-source topologies, as well as DC- and AC-decoupling topologies. Although each converter architecture has its own advantages and disadvantages, the AC-decoupling topologies stand out from the rest, because they can operate as a conventional VSI when efficiency takes precedence over CMV reduction. All these solutions imply the use of more hardware elements, increasing the size, complexity and cost of the drive.
5. PWM techniques oriented to the CMV reduction are another widely studied preventive solutions. These modulation algorithms can be implemented by following carrier-based or space-vector approaches. Although the former have certain implementation advantages due to their relative simplicity and low computational burden, the latter allow better representation of the switching states of the converter through the use of vectors and, therefore, a more understandable control of the CMV levels produced. Furthermore, since the control of electric machines is usually carried out vector-wise, calculating the inverter duty cycles also in vector coordinates is an easy, intuitive and straightforward approach. However, it is important to remark that fast digital devices such as FPGAs would be required for the practical implementation of space-vector modulation approaches. If, as usual, the electric machine control is programmed in a microcontroller, an additional digital device should be incorporated, increasing the cost of the control unit.
6. The RCMV-PWM family stands out among the space-vector modulation techniques. Their main purpose is to avoid the application of zero vectors, thus eliminating the switching states that generate the highest CMV levels. Moreover, there are other modulation techniques that, although their main goal is not the CMV reduction, they also exhibit remarkable performance. In this last group, discontinuous techniques stand out, which can

be considered multi-objective modulation techniques since they manage to reduce power losses while also reducing the CMV levels.

7. All in all, it should be noted that some of the reviewed alternative converter topologies and CMV-reducing PWM techniques can be combined to achieve better CMV reduction oriented results. With some particular topology/modulation combinations, as H8D2 and VSIZVR-D2 with CCMV-PWM, it is possible to completely eliminate this problem from the origin, and prevent it from spreading to other points of the electric drive system.

Thus, it can be finally concluded that the scientific literature provides a great variety of corrective (hardware) and preventive (hardware and software) approaches. Each solution has its own advantages and disadvantages in terms of performance (CMV mitigation, efficiency, THD, etc.), complexity and cost. Thus, the most suitable solution, or the combination of different solutions, must be carefully selected by engineers considering the requirements of the application and the obtained figures-of-merit.

### Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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