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Analysis of Interleaved Series Capacitor Tapped Buck topologies for adjustable output voltage range

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Abstract

During the last decade, high step-down applications have become an emerging topic in power electronics. From delivering power to modern embedded systems, to improving efficiency in high current and low voltage appliances, such as welding machines or superconducting magnets. In this work, an analysis of the series capacitor buck, one of the novel topologies in this field, is presented with two different configurations of tapped-inductors, in order to allow for a more flexible output voltage range.

1 Introduction

The series capacitor buck converter (SCB) (Fig. 1) was presented to improve the limitations of the traditional buck [1], [2] in Point-of-load (POL) applications, which were precise regulation and low output ripple. In general, buck converters allow for good regulation and efficiency [3]. However, obtaining very low output voltages imposes a lot of stress on power switches and overall efficiency in higher frequencies decreases. In this sense, the SCB was introduced to tackle these issues. It is built similarly to a conventional two-phase Buck converter and consists of two half-bridge branches and an LC filter in the output. The main difference is that it introduces a series capacitor between the two switches of the first branch, which effectively divides the input voltage by two. This makes all the switches of the converter operate with a drain-source voltage of $V_g/2$. Consequently, inductor current and switching losses are reduced, the duty ratio is doubled and automatic balance of phase currents is achieved.

The main advantages of this topology can be summarized as follows:

- For a given output voltage reference, the duty cycle (D) is doubled, as the output changes with $D \cdot V_g/2$. Thus, the performance of the converter under high step down operation is improved.
- Switching losses are reduced by a factor of two, as the voltage applied to the terminals of the semiconductors is also half the input voltage.

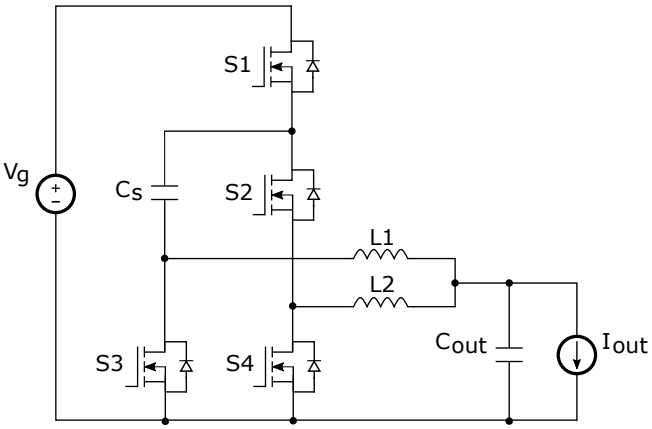
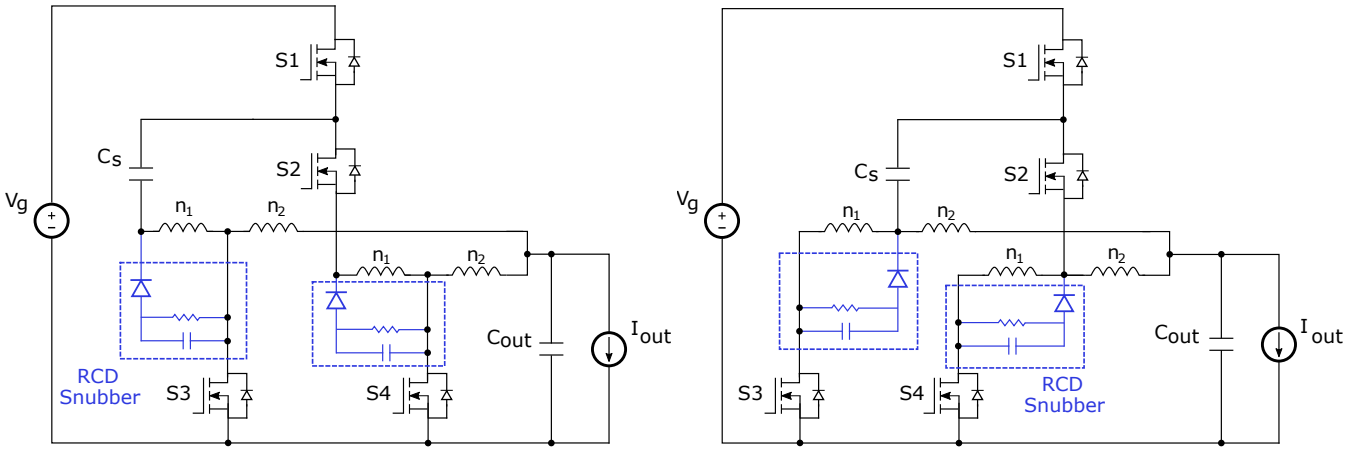


Fig. 1: Series Capacitor Buck converter.

- The current in both phases of the converter is automatically balanced whereas interleaved Buck converters require additional control logic and sensors.

However, it presents disadvantages, as well, such as a reduced maximum output voltage of $V_g/4$ due to a limited duty cycle of 50 $\%$ in order to maintain automatic current balance. In this context, several studies on tapped-inductor series capacitor buck converters have been conducted [4]–[7]. Nevertheless, these alternative topologies use additional switches that increase the overall cost of the converter. Therefore, in this work, two tapped-inductor topologies derived from the original SCB are presented (Figs. 2a and 2b), that maintains the same number of switching devices and make use of snubbers to get rid of voltage spikes.

The paper is organized as follows: in section 2,



(a) Lower switch tapped configuration (SCB-TSW). (b) Series capacitor tapped configuration (SCB-TCS).

Fig. 2: Schematics of two different Interleaved series capacitor tapped buck configurations.

the two tapped-inductor derived topologies are presented and analysed, as well as design considerations being discussed. Section 3, explains the experimental results obtained from the prototype built to test the converters, and summarises the components used for this purpose. Finally, in section 4, conclusions are discussed, besides the future work that will follow this paper.

2 Tapped-inductor configurations in the series capacitor buck

Two tapped-inductor configurations have been derived from the series capacitor buck converter (Fig. 2). The first one, is the lower switch-tapped SCB (SCB-TSW), which connects the lower switches S3 and S4 to the common terminal of the inductor (Fig. 2a). Whereas, in the second one, the series capacitor-tapped SCB (SCB-TCS) connects the lower legs of the series capacitor C_s and S2, to this terminal (Fig. 2b). The main advantage of tapped-inductors is that, with the same switch configuration as the SCB, the conversion ratio of both topologies is adjusted according to the turns ratio (N) between the primary (n_1) and the secondary (n_2) windings of the tapped-inductor:

$$N = \frac{n_1}{n_2}. \tag{1}$$

2.1 Tapped-inductor applications

In some applications, a wide output voltage range is required. The power supply for the Large Hadron Collider magnets, where an SCB is being used, has to provide a higher voltage during power up to guarantee a controlled current slope. Then, when the nominal current is reached, voltage is reduced

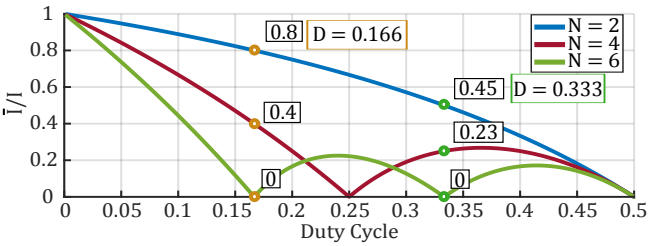


Fig. 3: Normalized ripple cancellation factor as a function of duty cycle for different N values.

to a lower level just to maintain this current [8]. Tapped configurations with adjusted values of (n_1) and (n_2) can be designed to meet this requirement. Advantages could be summarized as follows:

- Increased control over very low output voltages, improving overall regulation.
- Inductor current ripple amplitude depends on the turns ratio of the tapped inductor. According to the desired output voltage, the turns ratio could be adjusted to work with a desirable inductor current ripple.
- Tapped configurations with output voltages higher than $V_{DC}/4$ could be achieved, close to $V_{DC}/2$.
- In high current and ripple constrained applications, it is common to interleave multiple converters in order to meet these requirements. In such power converters, current ripple is reduced according to the number of interleaved phases and the applied duty cycle [9], [10]. For a given number of phases, with the use of tapped-inductors and adjusting the turns ratio, further reduction in current ripple could be achieved (Fig. 3).

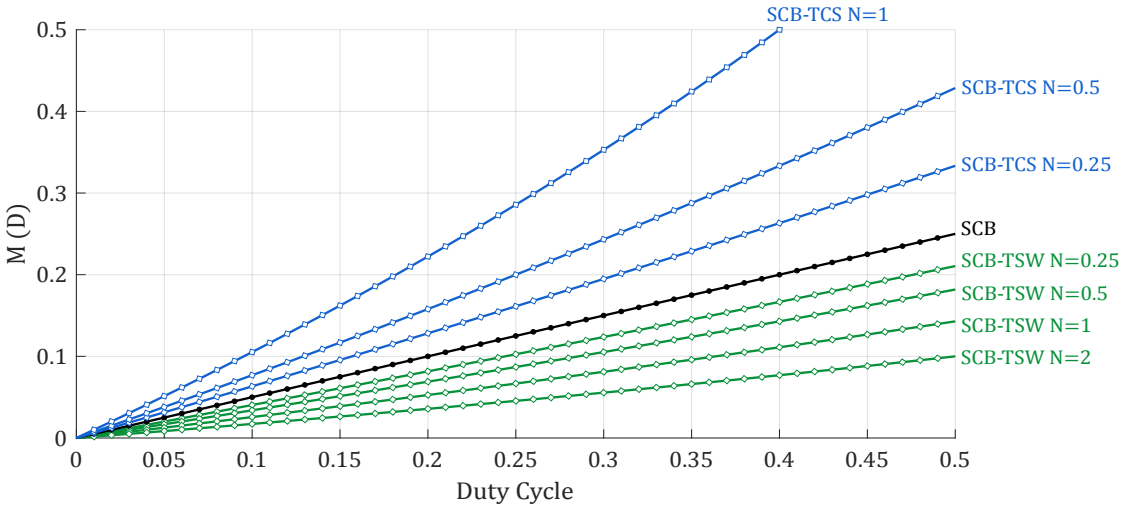
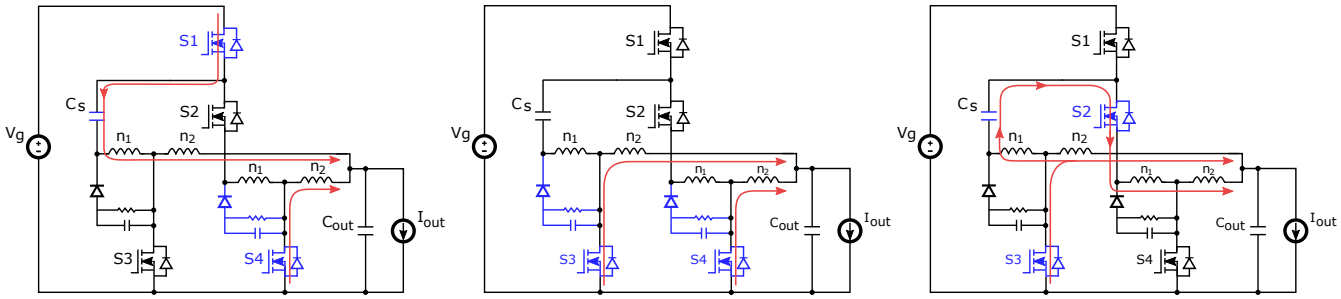
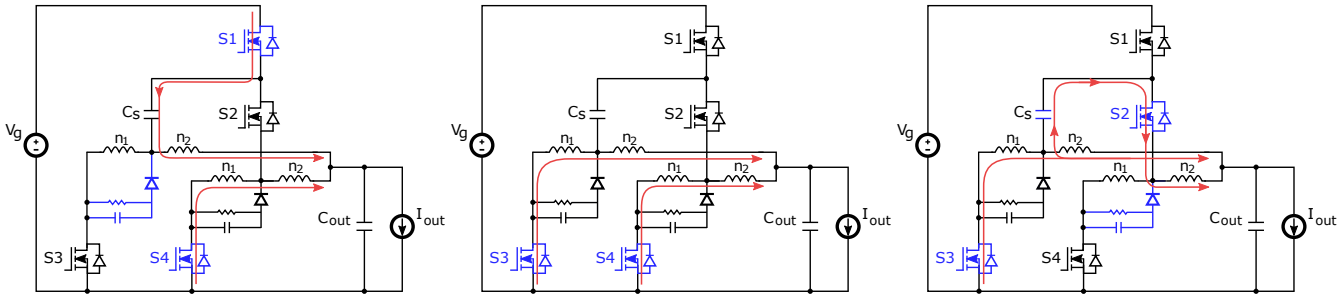


Fig. 4: Conversion ratio of the SCB-TSW and SCB-TCS converters.



(a) Stage 1 - SCB-TSW. (b) Stages 2 and 4 - SCB-TSW. (c) Stage 3 - SCB-TSW.

Fig. 5: Operation stages in SCB-TSW.



(a) Stage 1 - SCB-TCS. (b) Stages 2 and 4 - SCB-TCS. (c) Stage 3 - SCB-TCS.

Fig. 6: Operation stages in SCB-TCS.

2.2 Operation principles of proposed topologies

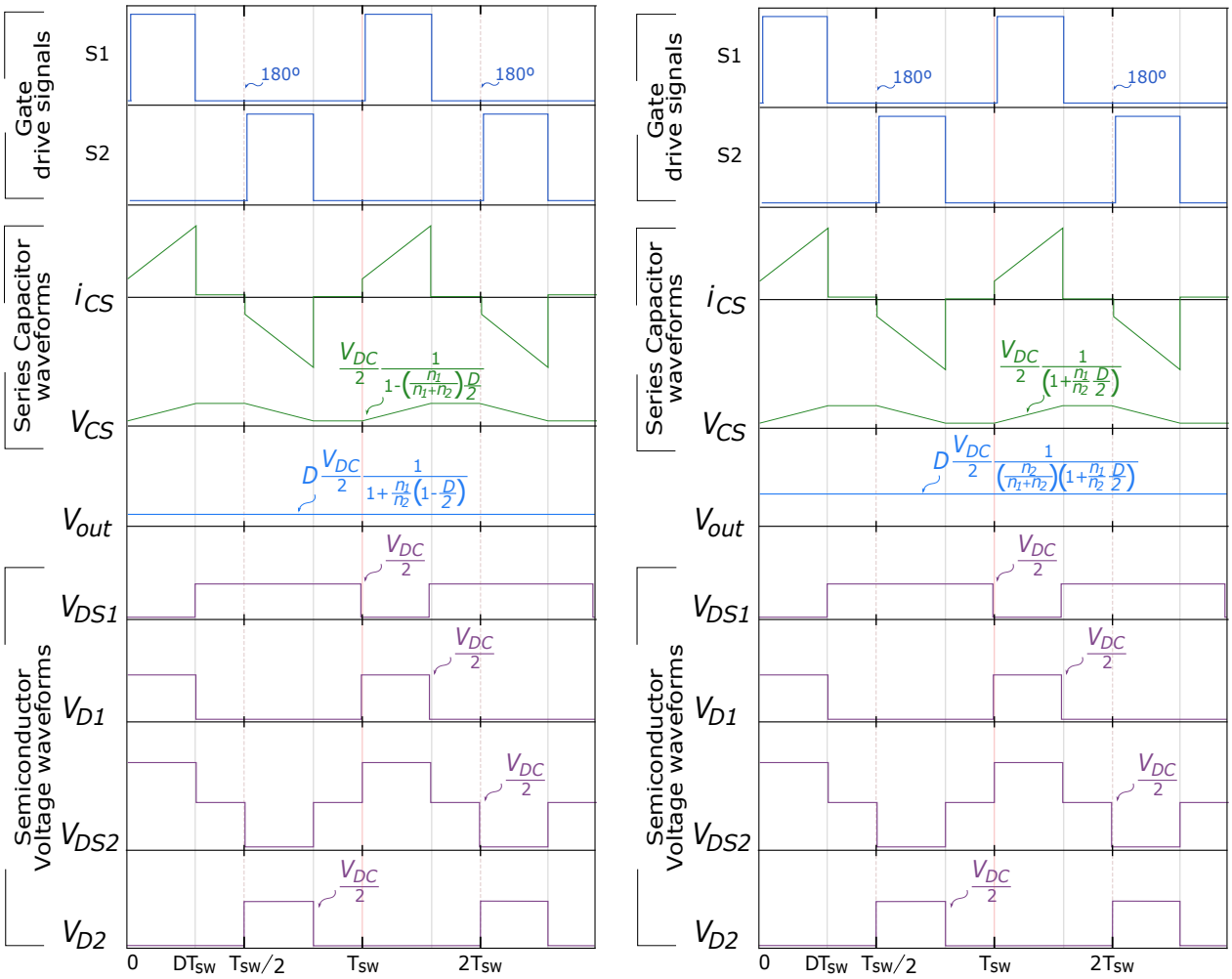
The SCB works in the same way as a conventional buck. In the case of the latter, the output voltage varies proportionally to the duty cycle:

$$M(Buck) = D\,V_g. \tag{2}$$

However, in the SCB, as soon as the intermediate capacitor reaches balance around $V_g/2$, conversion ratio is limited by this voltage level:

$$M(SCB) = \frac{V_g D}{2}. \tag{3}$$

In the case of the tapped configurations of the SCB, the turns ratio of the inductors modifies the way the converters operate (Figs. 5 and 6) which affects to their conversion ratio (M), extending or reducing the maximum output voltage (Fig. 4):



(a) SCB-TSW Waveforms. (b) SCB-TCS Waveforms.

Fig. 7: Waveforms of the proposed Tapped SCBs.

$$M_{(SCB-TSW)} = \frac{V_g D}{2}\frac{1}{1+\frac{n_1}{n_2}\left(1-\frac{D}{2}\right)}, \quad (4)$$

$$M_{(SCB-TCS)} = \frac{V_g D}{2}\frac{1}{\left(\frac{n_2}{n_1+n_2}\right)\left(1+\frac{n_1}{n_2}\frac{D}{2}\right)}. \quad (5)$$

This is dictated by the voltage balance in the series capacitor which is also defined by the turns ratio (Fig. 7) and the duty cycle applied for both tapped configurations:

$$V_{C_s\,(SCB-TSW)} = \frac{V_g}{2}\frac{1}{1-\left(\frac{n_1}{n_1+n_2}\right)\frac{D}{2}}, \quad (6)$$

$$V_{C_s\,(SCB-TCS)} = \frac{V_g}{2}\frac{1}{\left(1+\frac{n_1}{n_2}\frac{D}{2}\right)}. \quad (7)$$

2.3 Inductor Current Ripple

In the SCB, inductor current ripple equation is the same as in the traditional buck but the effect of the intermediate capacitor voltage has to be taken into account:

$$\Delta i_L\,(SCB) = \frac{V_o(1-2D)}{L}. \quad (8)$$

Depending on the output voltage, the SCB converter will offer a reduction in output current ripple [11]. The inductor current ripple equations for the tapped SCB converters include a relation for the different windings of the inductor:

$$\Delta i_L\,(SCB-TSW) = \frac{\left(\frac{n_1}{n_2}\right)V_o(1-2D)}{L}, \quad (9)$$

$$\Delta i_L\,(SCB-TCS) = \frac{\left(\frac{n_1}{n_1+n_2}\right)V_o(1-2D)}{L}. \quad (10)$$

While working with certain output voltages, this could help obtaining a higher reduction of the inductor current ripple, and, thus, reducing inductor core losses, as well.

2.4 Tapped-inductor design considerations

In tapped-inductor converters, voltage spikes occur during the turn-off of power switches. In some of these transitions one terminal of the tapped-inductor windings is leaved floating unconnected, which immediately generates an opposing magnetomotive force (MMF) that changes the polarity of the inductor current producing a voltage spike across the winding terminals. This effect is due to the energy stored in the leaking inductance of the tapped-inductor (L_{leak}).

This effect can be mitigated with the proper design of the inductor [12], [13] and the use of snubbers. These elements dissipate this energy in the form of heat and generate power losses affecting the overall efficiency of the converter, but, at the same time, offer an inexpensive and simple solution to this problem.

3 Experimental setup

A prototype to test the functionality of both SCB tapped topologies has been built (Fig. 8). The components used for each converter were identical and are listed in Table 1. Diodes have been used instead of MOSFETs as synchronous rectifiers to reduce the number of driving signals and complexity of the prototype. A summary of the experiments conducted in this paper and the obtained results can be found in Table 2, which shows the different configurations of input voltage, inductance, turns ratio, MOSFET's ON resistance, switching frequencies and snubber values that have been used in each topology. It also serves as a comparison between the converters proposed and the conventional SCB. Output voltages that can be achieved with each topology, as well as the duty cycles required are listed. Power losses and the efficiencies obtained are also included.

3.1 SCB-TSW Experimental results

The results for the SCB-TSW converter prove the theoretical concepts described in the previous sections. The voltage in the series capacitor increases according to the turns ratio and the duty cycle applied to the converter (Fig. 9a). In the experiments conducted, a 24 V input, and a turns ratio (N) of 1 were used. The converter output was set to 1.2 V and 15 A, with a duty cycle of 25.5 $\%$, which verifies that very high conversion ratios can be achieved applying a higher duty cycle than the conventional SCB. Tests at 2.5 V and 25 A were conducted, with an applied duty cycle of 25.5 $\%$ for the conventional SCB, and 45.5 $\%$ for the SCB-TSW, which better illustrate this behaviour. Voltage spikes of 48 V_{pk-pk} and 28.5 V_{pk-pk} were observed in S2 and S3 of the SCB-TSW, respectively (Figs. 9b and 9c) due to a not optimized leakage inductance and snubber values.

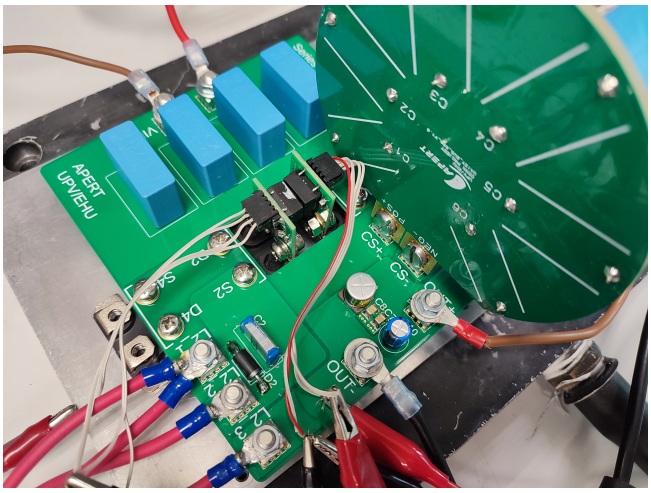


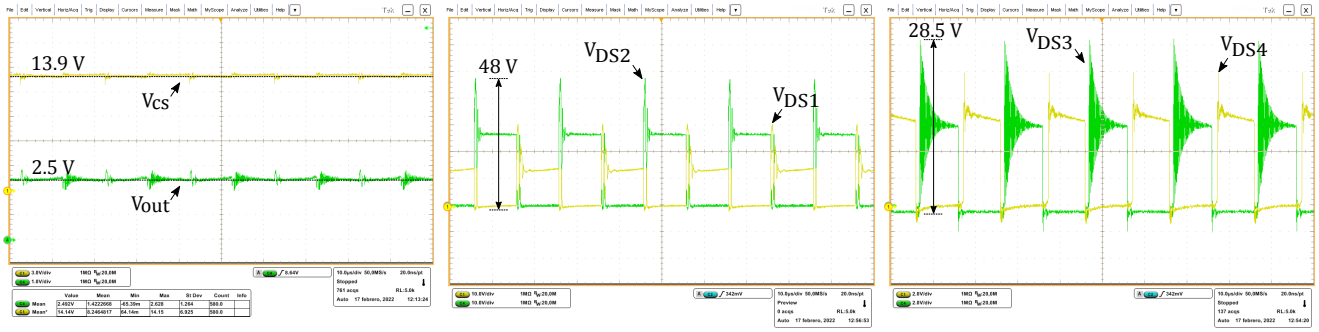
Fig. 8: Tapped SC Experimental Platform.

Tab. 1: Hardware component parameters.

Component	Parameter
Inductance (L)	3.5 μH
Input Capacitance (C_{in})	100 μF
Output Capacitance (C_o)	100 μF
Series Capacitance (C_s)	400 μF
Power MOSFET	IXFN520N075T2
Power diode	DSS2X121-0045B
Gate driver	1C20H12A
Inductor core material	3C92
Inductor core dimensions	64 x 51 x 10 mm

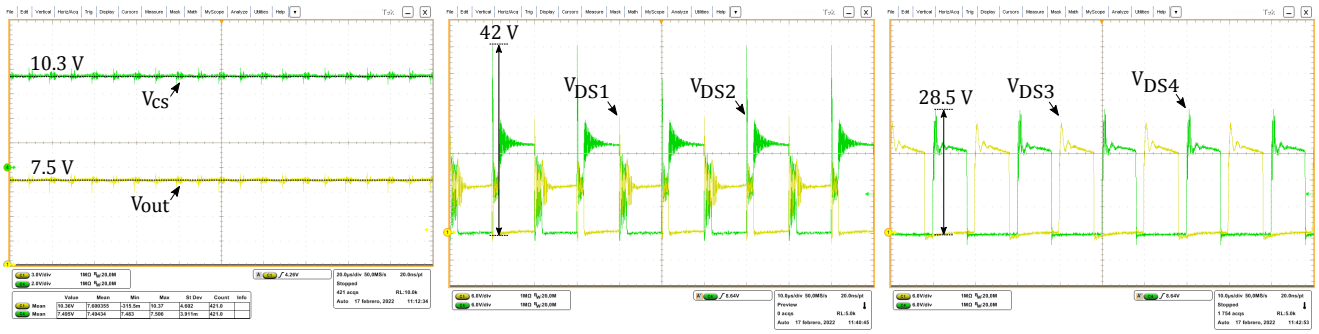
3.2 SCB-TCS Experimental results

The results for the SCB-TCS converter show that the voltage in the series capacitor decreases according to the turns ratio and the duty cycle applied to the converter (Fig. 10a). The experiments were conducted with a 24 V input, and a turns ratio (N) of 1. The converter output was set to 7.5 V and



(a) Output and C_s voltage. (b) V_{DS1} and V_{DS2} voltage levels. (c) V_{DS3} and V_{DS4} voltage levels.

Fig. 9: SCB-TSW Captured waveforms.



(a) Output and C_s voltage. (b) V_{DS1} and V_{DS2} voltage levels. (c) V_{DS3} and V_{DS4} voltage levels.

Fig. 10: SCB-TCS Captured waveforms.

Tab. 2: Results overview (V_g = 24 V, f_{sw} = 50 kHz, $R_{DS(ON)}$ = 1.9 $m\Omega$, $R_{snubber}$ = 6.8 Ω, $C_{snubber}$ = 1 uF).

$Topology$	V_{out} (V)	I_{out} (A)	N	L_{mag} (μH)	D $(\%)$	P_{out} (W)	P_{in} (W)	P_{loss} (W)	η $(\%)$
SCB	2.5	25	–	3.5	25.0	62.5	80.2	17.7	77.9
$SCB-TSW$	1.2	15	1	3.5	25.5	18	25.7	7.7	70.0
$SCB-TSW$	2.5	25	1	3.5	45.5	62.5	82.6	21.1	75.7
$SCB-TCS$	7.5	12	1	3.5	41.2	90	105.1	15.1	85.6

12 A, with a duty cycle of 41.2 %, demonstrating the converter ability to go past $V_{DC}/4$, which expands the SCB applications range. Voltage spikes of 42 V_{pk-pk} and 28 V_{pk-pk} were observed in S2 and S4, respectively (Figs. 10b and 10c). Optimizations in the inductor design construction, as well as an improved snubber network are needed to mitigate this effect.

4 Conclusions and future work

The series capacitor buck converter is a topology that offers several advantages over the traditional buck, such as an extended duty cycle. However, it presents a limited maximum output voltage of $V_{DC}/4$, which holds it to be used in some applications. In this work, two tapped-inductor configurations derived from this topology have been discussed, that allow for a fine tuning of the output voltage and current ripple. Experimental results from 24 V to 1.2 V and 7.5 V confirm the theoretical functionality of both topologies, respectively. In the case of the SCB-TSW, a very low output voltage can be set with an increased duty cycle, which allows for a better regulation. As for the SCB-TCS, an output voltage higher than $V_{DC}/4$ can be set, expanding the voltage range of the conventional SCB, and, thus, its application range.

Further optimisations of the experimental platform in this paper, can be conducted, such as the adjustment of the turns ratio in the tapped-inductors to better suite a desired output voltage with a convenient duty cycle and ripple. An optimised snubber network and the use of MOSFETs as synchronous rectifiers will increase the efficiency of both topolo-

gies. Furthermore, designing low-leakage inductance magnetic components, will reduce voltage spikes. Thus, a lower voltage grade power switches can be used, reducing power losses and further improving efficiency.

5 Acknowledgements

This work was supported in part by the Government of the Basque Country within the fund for research groups of the Basque University system IT978-16 and by the ELKARTEK research program (project ENSOL2-KK-2020/00077) and by the MCIN/AEI/10.13039/501100011033 within the project PID2020-115126RB-I00. Open Access funding provided by University of Basque Country.

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