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Analysis and design of a multilayer DC bus with low stray impedance and homogenous current distribution

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Abstract

The aim of this work is to design a DC bus for a silicon carbide power converter whose application is the automotive sector. This power converter works at high voltage and current levels with high frequencies signals, so a DC bus design with low impedance is necessary. Moreover, current has to flow homogeneously to avoid imbalances between bus capacitors. In order to get this goal, different design criteria are explained. These criteria are based on the theory of semiconductor parallelization, where the control and equal distribution of parasitic impedances is fundamental to get a modular bus structure, where the symmetrical design and mutual coupling effect of different layers produce a current balance over the wide and long copper areas of this DC bus.

1. Introduction

DC bus is an important component of power converter to exchange current between the different power sources. Nowadays, automotive and traction converters work at higher switching frequencies producing high *dv/dt* and *di/dt* [1, 2]. These effects are more critical in converters of silicon carbide MOSFETs [3] than in silicon IGBT converters [4], so decreasing stray impedance, especially inductances, is fundamental to avoid overshoots, overvoltage spikes across power semiconductors and resonance effects between bus capacitors [5]. Apart from restricting the stray impedance with the DC bus shape and dimensions, using a multilayer structure [6] minimizes total parasitic inductance due to coupling effect between layers. Moreover, applying the semiconductor parallelization technique [7] by means of the concept of a symmetrical design, the internal current imbalances are reduced. These imbalance effects can produce thermal problems in capacitors, instead of making a modular design that can be expanded easily.

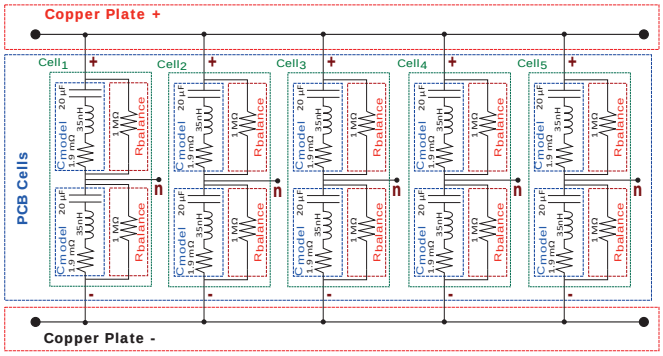


Fig. 1: Schematic of the DC bus with its main parts.

This work presents a multilayer DC bus rated at 400/500 V taking into account the parallelization technique of power devices [8] in order to make a balanced design between capacitors with low stray impedances. For this, the DC bus design is made with *Keysight* ADS^{TM} software to obtain the electromagnetic model [9] based on equivalent *S-parameters*, thus this non-ideal model allows to analyse 3D current density distribution. Finally, the simulation results are validated with different experimental measures obtained from the prototype.

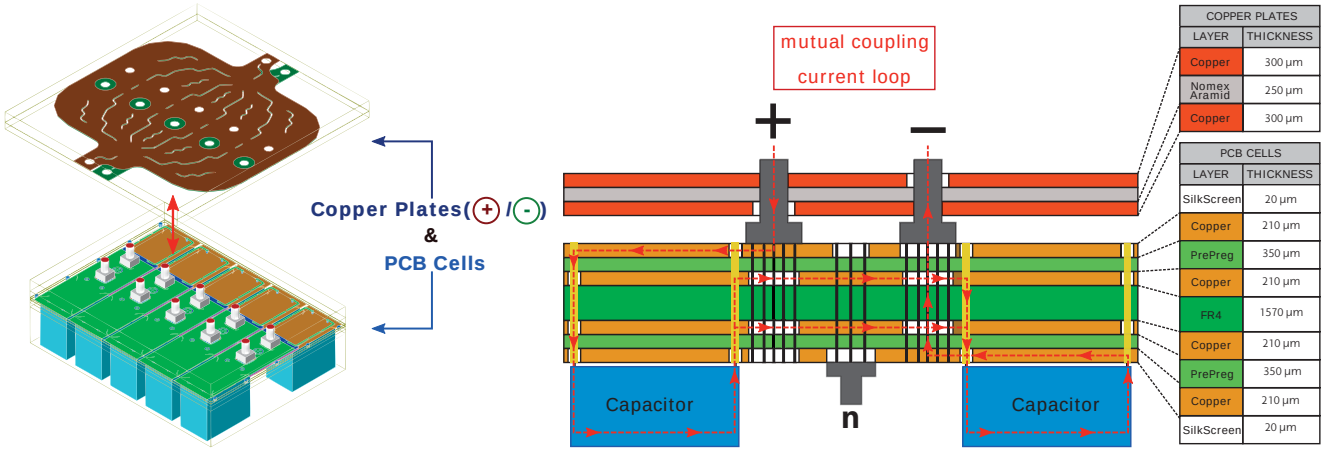
2. DC bus design

The design presented in this work has the goal of improving the DC bus behaviour by means of [10]:

a) Decreasing stray impedances, especially inductances.

b) Balancing current capacitor branches [11, 12].

c) Allowing scalability to obtain a standard structure for multiple applications.



(a) Bus designed by PCB and Copper Plates. (b) Multilayer stackup with the internal current loop.

Fig. 2: DC bus main structures and its multilayer substrate.

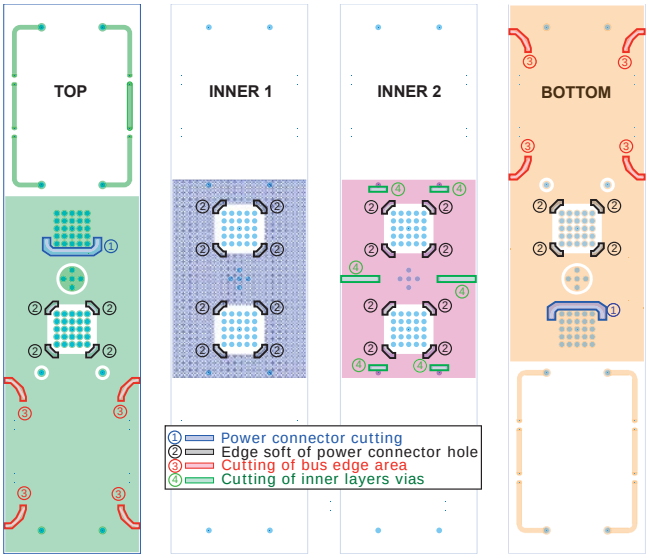


Fig. 3: Layout of each layer of the PCB cell.

In order to take these objectives, the present design has two main parts, as Fig.1 shows:

1. PCB Cells (Fig 2(a)): consisting of a PCB with 5 isolated capacitor cells [6]. Each cell has two capacitors (C4ATHBW5200A3NJ, 20 μF, 600 V and 29 A) in series, to get the range voltage for automotive (400/500 V) and traction (1000 V) applications, and resistances (1 $M\Omega$) to balance the voltage between the two serie capacitors. Fig 2(b) shows the different layers and thickness of this power PCB (3.2 mm).

2. Copper Plates (Fig 2(a)): these two copper plates (Fig 2(b)), with a dielectric in the middle, connect the 5 parallel capacitor cells of PCB, reducing the ripple current of capacitors, with and homogenous current distribution [11].

In the following sections, the design criteria of each part is explained to understand the design benefits of this DC bus made with a PCB and copper plates. These criteria are based on the device paralellization technique [7, 8], specially when different cuts are applied in order to get symmetrical paths with stray impedances as identical as possible.

2.1. Power multilayer PCB

The capacitor cells have been designed with a PCB multilayer structure to satisfy the next criteria:

1. The material has to show facilities and flexibility for designers, so a PCB structure (Fig. 2(b)) is cheaper than a lamited busbar based on copper plates with dielectrics [13].

2. The design has to offer an easy scalability to be applied in other power applications. For this reason, this DC bus is divided in basic cells (Fig. 2(a)) to be add or subtracted according to application requirements.

3. The power connectors must be ready for high voltages and currents, present low stray impedances and be easy assembly over PCB. This way, the REDCUBE PRESS-FIT connectors (300 A and 8 nH at 10 kHz) of CuZn39Pb3 (0.062e-6 $\Omega \cdot cm$) have been selected.

4. The design must benefit from mutual coupling effect to reduce stray inductances, thus a multilayer structure has been defined. Inside each capacitor cell, the current flows with opposite di-

rections through each layer due to an internal loop (Fig 2(b)), getting a high coupling effect.

5. The current distribution inside the cell has to be as homogenous as possible to avoid thermal problems. Moreover, PCB designs cannot support high temperature, so an equal current distribution is fundamental. With this aim, the different layers of the capacitor cell (Fig.3) have special cuts to get a good current distribution over these copper areas:

   a) The top and bottom layers have a cut in front of power connector (Fig.3-①) to avoid a high current in only few connector pines, so current flows with better distribution through power connector.

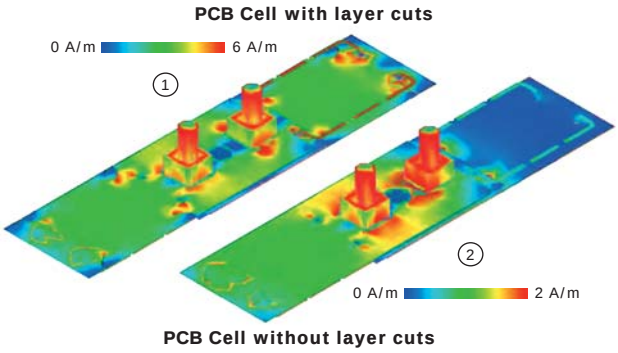
   b) The four layers (top, inner1, inner2 and bottom) have soft edge in the power connector clearance (Fig.3-②) to avoid high current densities due to vertex.

   c) The top and bottom layers have wide and long copper areas, to find a good current distribution without high current densities in borders of these areas, rounded cuts (Fig.3-③) are done to control current density instead of increasing stray inductance.

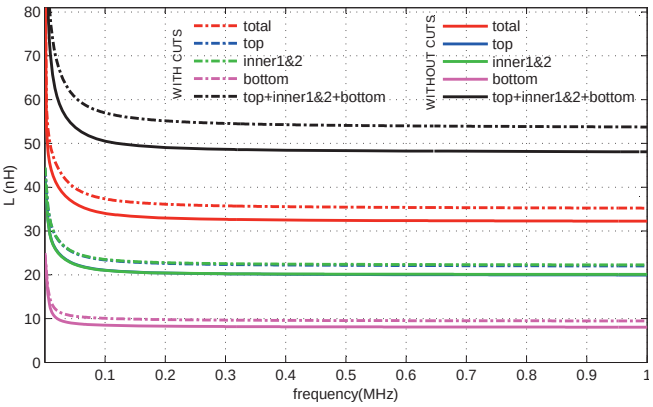
   d) The inner1 and inner2 are electrically connected. Due to the current loop, inner 2 has a higher current density. However, current must be distributed as equal as possible between the two inner layers, so the solution is to apply rounded cuts (Fig.3-④) in inner2 to distribute the current between the layers.

The design criteria mentioned and layer cuts in the PCB capacitor cell produce an improvement of current distribution as Fig.4(a)-① and Fig.4(a)-② show. Layer cuts improve the current distribution, but they increase the parasitic inductance of each layer (Fig.4(b)). However, this increase of stray inductance is assumable to get a better current distribution. Moreover, the effect of mutual coupling inductances due to internal current loop reduces the total parasitic inductance value, as Fig.4(b) shows in the total value, which is less than the sum of each layer (1).

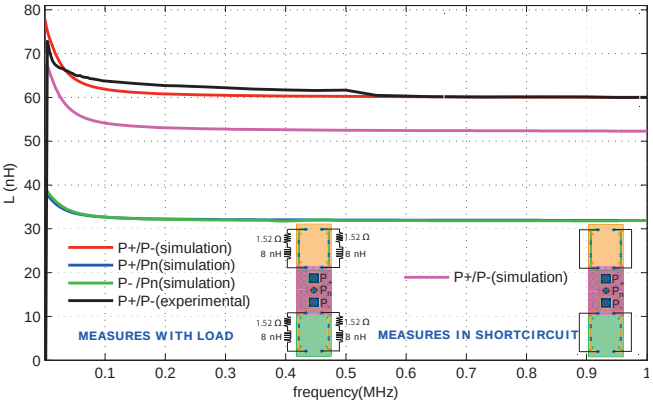
$$L_{total} < L_{top} + L_{inner1} + L_{inner2} + L_{bottom} \quad (1)$$



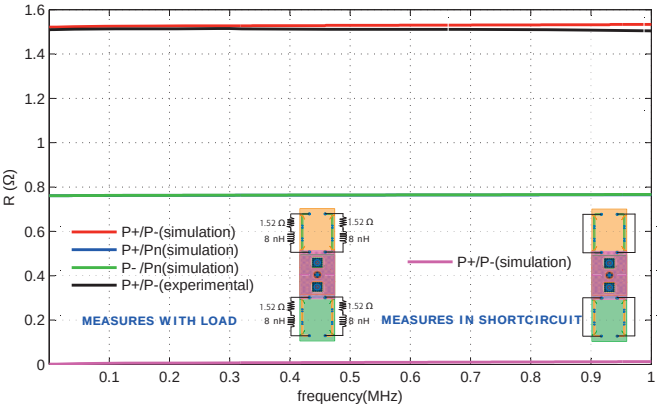
(a) DC current density distribution with/without cuts.



(b) Inductance values of each layer with/without cuts.



(c) Inductance values of between power connectors.



(d) Resistance values of between power connectors.

Fig. 4: Capacitor cell simulations and experimental data.

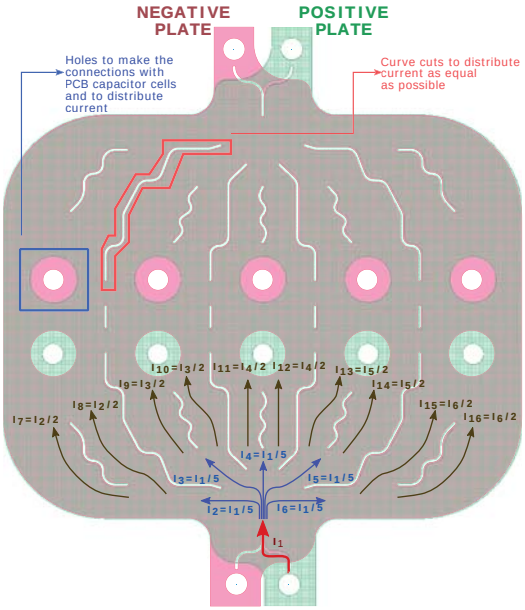


Fig. 5: Design of the two plates of copper.

The PCB capacitor cell is a circuit with low stray inductance (Tab.1) and low resistance values, according to simulation and experimental data. Fig.4(c) and Fig.4(d)) compare the experimental total values (P+/P- experimental) with different simulation measures between main terminals: positive-negative (P+/P- load), positive-neutral (P+/Pn load), negative-neutral (P-/Pn load) and positive-negative (P+/P- short-circuit). It is important to indicate that test and simulations are done with 1.5 Ω and 8 nH to be able to obtain the inductance values of PCB without high-pass capacitor effects.

2.2. Low inductance Copper Plates

These two copper plates (positive and negative, Fig.5) connect in parallel the isolated capacitor cells of the power PCB. As in the case of PCB capacitor cells, the copper plates have been designed to satisfy the next design criteria:

1. The structure has to present low resistance and inductance values to minimize the total impedance of DC bus, so two copper plates of 300 μm have been used (Fig.2(b)).

2. The mutual coupling effect has to be used in order to reduce the total inductance value. For this reason, both copper plates have to be as symmetric as possible with same dimensions (Fig.5). Moreover, the current of each layer must flow with different direction, so a high coupling effect appears between both plates.

3. The plates must distribute the current as equal as possible between capacitor branches, since a higher current in a particular cell or a wide imbalance between them could produce the PCB crystallisation and capacitor thermal break. To get these goals, the design must implement the next cuts, as in Fig.5:

   a) The holes, which connect copper plates with the positive and negative terminals of PCB cell power connectors, must be circles to improve the current flowing.

   b) The copper cuts must be used to make as equal as possible the distances and dimensions between PCB cells connectors and the main power DC bus inputs/outputs.

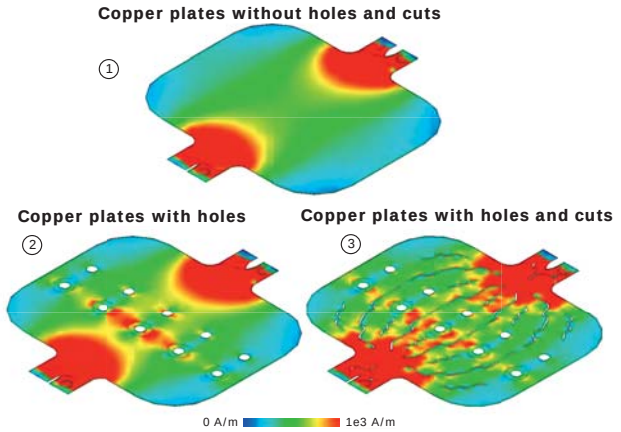
Tab. 1: Parasitic impedances values at 10 kHz.

Structure	Frequency: @10kHz	
	L (nH)	R (mΩ)
PCB cell	64.8	126
Copper plates	18.4	67
Full structure (without stray capacitor impedances)	17.2	68
Full structure (with stray capacitor impedances)	30.3	145

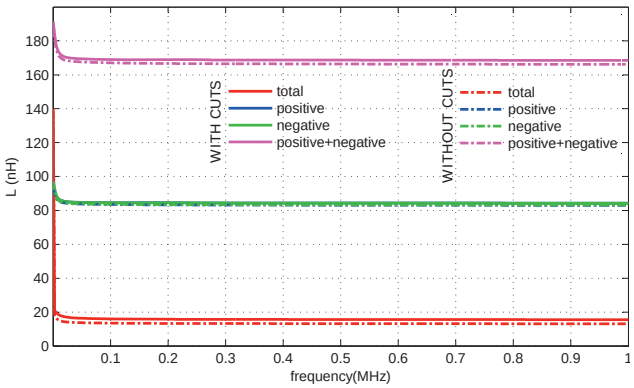
According to these requirements, the copper layers present an improvement in the current distribution due to the holes and cuts, as Fig.6(a)-①, Fig.6(a)-② and Fig.6(a)-③ show. The rounded holes are necessary to be able to connect copper plates with PCB cells. They produce by default a good current distribution (Fig.6(a)-②) because circular structures are not major obstacles for current flux. However, this current distribution can be improved with the copper cuts (Fig.6(a)-③). These cuts increase the stray inductance value of each copper plate (Fig.6(b)), but they improve current distribution. Moreover, the high mutual coupling effect produces a low stray inductance (Fig.6(b)) (2).

$$L_{total} < L_{positive} + L_{negative} \quad (2)$$

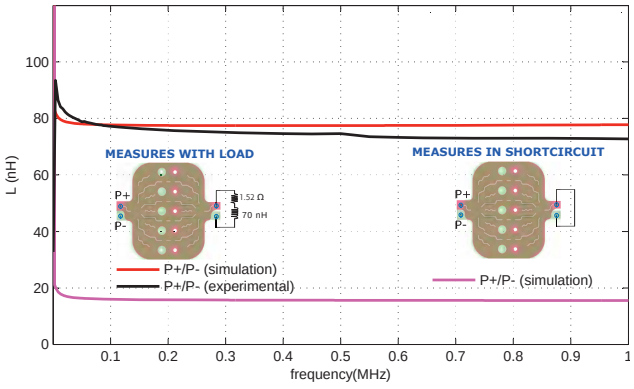
Finally, different measures between the main terminals (Fig.6(c) and Fig.6(d)) with/without and external load (1.5 Ω and 70 nH) verify the low resistance and inductance values of these copper plates, approximately, 2 $m\Omega$ and 15 nH in short-circuit.



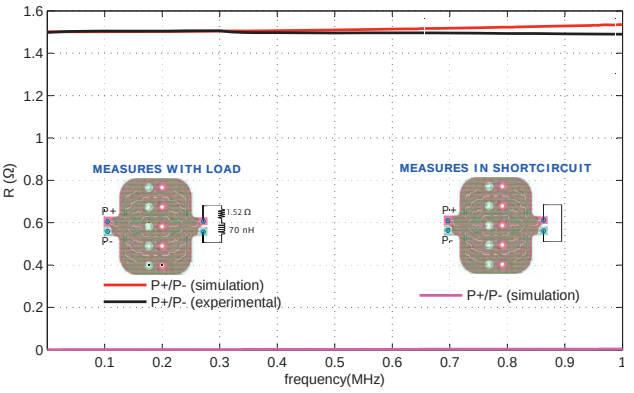
(a) DC current density distribution.



(b) Inductance values with/without cuts.

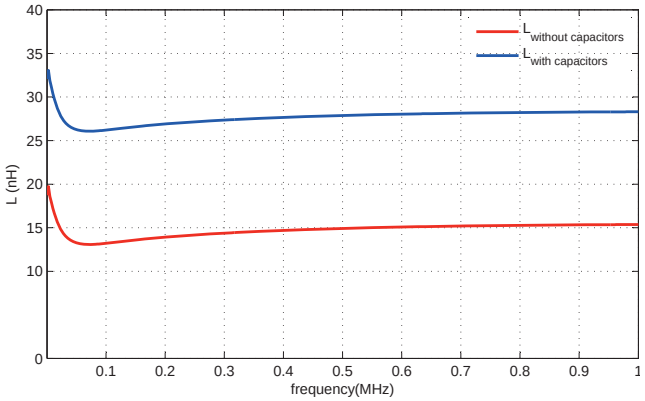


(c) Inductance values between main terminals.

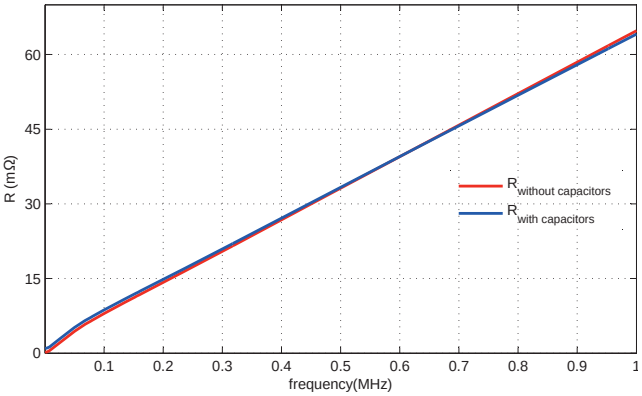


(d) Resistance values between main terminals.

Fig. 6: Copper plates simulations and experimental data.



(a) Inductance values with/without capacitors.



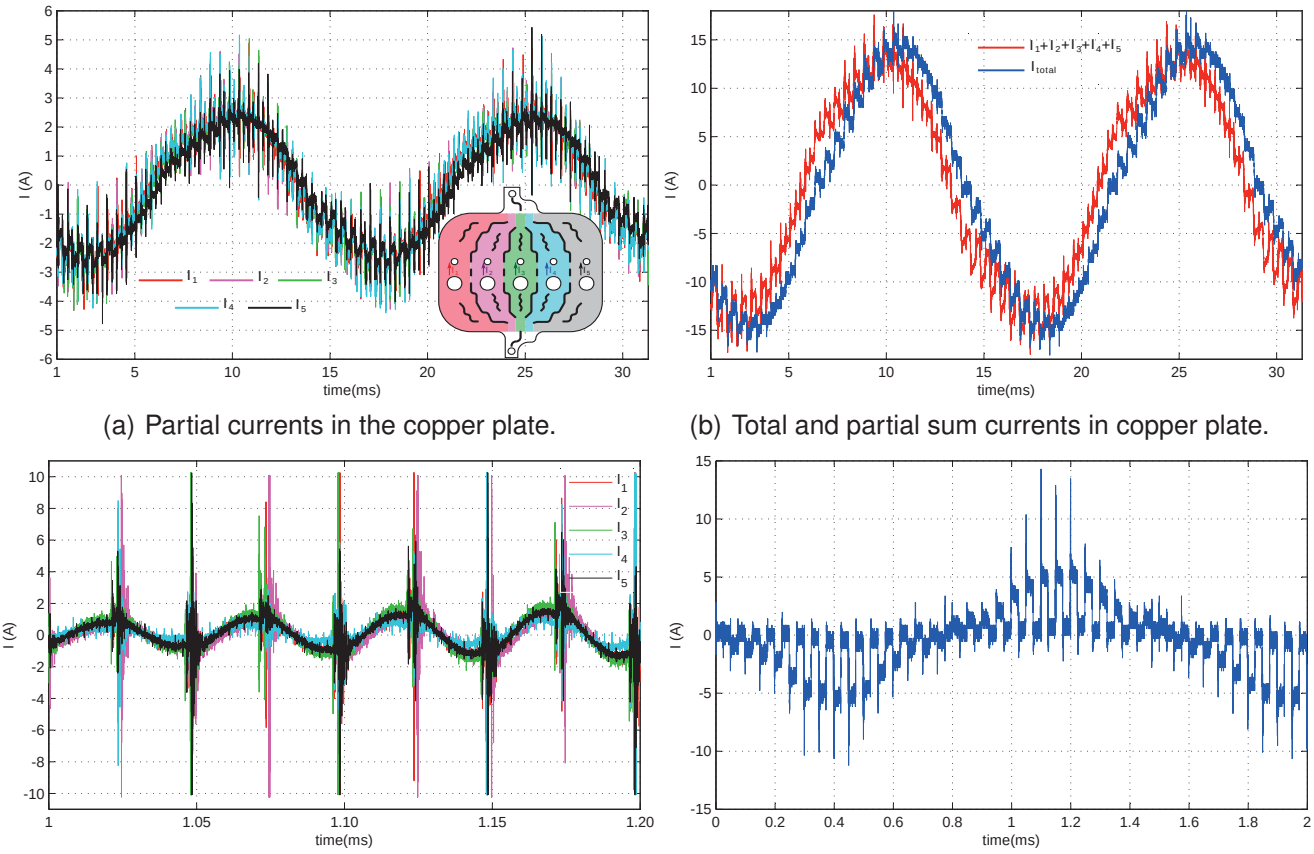
(b) Resistance values with/without capacitors.

Fig. 7: Impedance values of PCB cells + Copper plates.

2.3. Total DC bus structure

The union of the two parts of the design, PCB capacitor cells and copper plates, forms the total DC bus structure (Fig.2(a)). The positive and negative copper plates connect in parallel the 5 PCB cell branches of DC bus. The stray impedance value of the full structure is lower than each part of the design due to this parallel connection with its coupling effects [14]. For example, Tab.1 shows a comparative of each partial structure and the full design taking into account or not the values of ESL and ESR capacitors. The parasitic inductance and resistance values of the full structure with/without the stray impedance of the 10 capacitors are shown in the Fig.7(a) and Fig.7(b), respectively.

These stray impedances of this DC bus are higher than some market solutions, which have inductances between 15-20 nH. However, these solutions cannot be customized easily depending on voltages and currents of the power applications. In this DC bus, the current level can be modified



(a) Partial currents in the copper plate.

(b) Total and partial sum currents in copper plate.

(c) Partial currents in each PCB cell.

(d) Current in the inductive load.

Fig. 8: Current measures in copper plate and PCB cell.

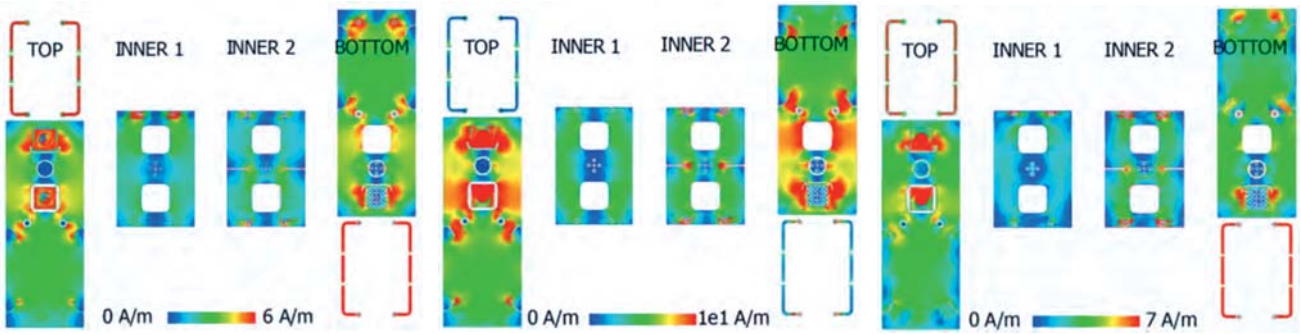
adding or subtracting the number of PCB capacitor cells and voltage levels using different capacitors. Moreover, the design has a symmetrical layout to balance the current in each part, so capacitors are going to provide a similar current, the same concept than in semiconductor paralellization.

3. Testing current balance and current density distribution

In this design is fundamental to find a current distribution as homogenous as possible to avoid problems with PCB cell branches, since they are made of FR4 dielectric and any current imbalance or higher concentration can produce a thermal breakdown. For this reason, copper plates have to divide the current as equal as possible between PCB cells.

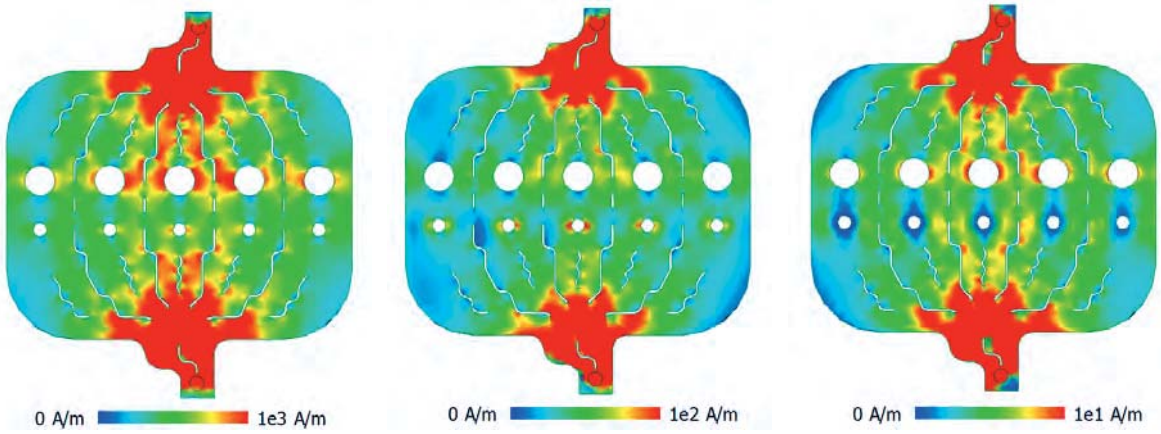
In order to check that copper plates divide equally the current, a signal of 16 App at 660 Hz flows through one copper plate. Different current measures are made in the points where PCB cells have to be connected. The results of each partial current are shown in the Fig.8(a). These results verify that the copper plate makes a good current division, since high imbalances are not appreciated. Moreover, Fig.8(b) shows a comparative between the total current and the sum of each partial current, this test indicates that losses are very low because both signals have the same amplitude. Finally, Fig.8(c) shows the current per each PCB cell when the DC bus is connected to a power converter with 600 Vdc and a current in the inductive load as in Fig.8(d). The signals of Fig.8(c) are similar, without wide current imbalances, so the 5 PCB cell branches are balanced and each one provides, approximately, the same current for DC bus.

Other important point to be tested is the current density distribution. A single PCB cell and the copper plates have been tested independently (to avoid long computing times in ADS^{TM} simulation platform). Each part of the design is connected to a simplified circuit emulating a power converter. This circuit consists of a voltage source of 600 V (1 Ω and 2 μH) and a current source of three spectral



(a) DC current density. (b) 1 kHz current density. (c) 20 kHz current density.

Fig. 9: Current density distribution at different frequencies in the layers of PCB cell capacitors.



(a) DC current density. (b) 1 kHz current density. (c) 20 kHz current density.

Fig. 10: Current density distribution at different frequencies in the positive copper plate.

components: DC (0 Hz), 1 kHz and 20 kHz with amplitude of 200 A, 50 A and 5 A, respectively.

The current density simulations of the PCB cell at different frequencies (Fig.9(a), Fig.9(b) and Fig.9(c)) allow to detect areas with a higher current density. Due to design criteria, specially internal cuts of layers, the PCB cell does not show wide current imbalances. In Fig.9(c), Fig.9(b) and Fig.9(c), the critical points are PCB vias and power connectors, but these always have higher current density because of being points with high current flux.

Finally, the Fig.10(a), Fig.10(b) and Fig.10(c) show the current density distribution of the positive copper plate. The negative copper plate has not shown because of its symmetry, which presents identical current density values. As in the PCB cell case, due to holes and cuts, the current does not show wide current imbalances at different frequencies. Moreover, the Fig.10(a), Fig.10(b) and Fig.10(c) show similar current distribution at different frequencies, so copper plates produce a good current division between the 5 cell branches. It is obvious that cell branches of borders do not have the same current than the centre branch. However, the difference is not critical as Fig.8(a) and Fig.8(c) demonstrate.

4. Conclusions

This DC bus design, based on the parallelization technique, gets a balanced design where each capacitor provide the same current level. According to simulation data and experimental results, the design shows a low stray impedance with and homogeneous current distribution. These parasitic impedances are very similar to commercial solutions with the advantage of scalability and customization.

This design has two main parts with different technologies: the power PCB and the copper plates. The power PCB allows using the printer board technology to design the symmetric cuts in copper areas to avoid skin effects. Moreover, with the multilayer stackup is possible to reduce total stray inductance thanks to coupling effects of current loop.

The copper plates allow connecting capacitor cells of PCB distributing the total current as equal as possible between parallel cells thanks to the different cuts and holes over copper area of low stray impedance.

Finally, this DC bus design is possible to expand easily because the number of isolated cells can be increased without modifying its design. Only the copper plates should be changed to connect the number of total capacitor branches.

5. Acknowledgement

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6. References

[1] A. D. Callegaro, J. Guo, M. Eull, B. Danen, J. Gibson, M. Preindl, B. Bilgin, and A. Emadi. Bus bar design for high-power inverters. *IEEE Transactions on Power Electronics*, 33(3):2354–2367, March 2018.

[2] J. Stewart, J. Neely, J. Delhotal, and J. Flicker. Dc link bus design for high frequency, high temperature converters. In *Applied Power Electronics Conference and Exposition*, pages 809–815, 2017.

[3] F. Alkayal and J. B. Saada. Compact three phase inverter in silicon carbide technology for auxiliary converter used in railway applications. In *European Conference on Power Electronics and Applications*, pages 1–10, 2013.

[4] L. Popova, R. Juntunen, T. Musikka, M. Lohtander, P. Silventoinen, O. Pyrhnen, and J. Pyrhnen. Stray inductance estimation with detailed model of the igbt module. In *European Conference on Power Electronics and Applications*, pages 1–8, 2013.

[5] X. Pei, W. Zhou, and Y. Kang. Analysis and calculation of dc-link current and voltage ripples for three-phase inverter with unbalanced load. *IEEE Transactions on Power Electronics*, 30(10):5401–5412, Oct 2015.

[6] C. Chen, X. Pei, Y. Chen, and Y. Kang. Investigation, evaluation, and optimization of stray inductance in laminated busbar. *IEEE Transactions on Power Electronics*, 29(7):3679–3693, July 2014.

[7] A. Matallana, J. Andreu, J. I. Garate, I. Aretxabaleta, and E. Planas. Analysis and modelling of igbts parallelization fundamentals. In *Conference of the IEEE Industrial Electronics Society*, pages 3247–3252, 2016.

[8] A. Matallana, J. Andreu, J. I. Garate, I. M. de Alegra, and I. Kortabarria. Analysis of impedance and current distributions in parallel igbt design. In *International Symposium on Industrial Electronics*, pages 616–621, 2017.

[9] D. Cottet and I. Stevanovic. Electromagnetic simulation and design of complex, planar bus bars for multi-level, high power converters. In *Control and Modeling for Power Electronics*, pages 1–6, 2012.

[10] F. Zare and G. F. Ledwich. Reduced layer planar busbar for voltage source inverters. *IEEE Transactions on Power Electronics*, 17(4):508–516, Jul 2002.

[11] H. Wen, W. Xiao, H. Li, and X. Wen. Analysis and minimisation of dc bus surge voltage for electric vehicle applications. *IET Electrical Systems in Transportation*, 2(2):68–76, June 2012.

[12] G. Zou, Z. Zhao, and L. Yuan. Study on dc busbar structure considering stray inductance for the back-to-back igbt-based converter. In *Applied Power Electronics Conference and Exposition*, pages 1213–1218, 2013.

[13] H. Yu, Z. Zhao, T. Lu, L. Yuan, and S. Ji. Laminated busbar design and stray parameter analysis of three-level converter based on hvigbt series connection. In *Applied Power Electronics Conference and Exposition*, pages 3201–3207, 2015.

[14] M. C. Caponet, F. Profumo, R. W. De Doncker, and A. Tenconi. Low stray inductance bus bar design and construction for good emc performance in power electronic circuits. *IEEE Transactions on Power Electronics*, 17(2):225–231, Mar 2002.