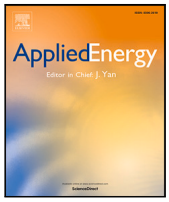
Applied Energy 371 (2024) 123730

Contents lists available at ScienceDirect

Applied Energy

journal homepage: www.elsevier.com/locate/apenergy



Hardware design of a high-current, high step-down ratio Series Capacitor Buck converter prototype for slow-ramped powering of High-Luminosity Large Hadron Collider inner triplet superconducting electromagnets

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ARTICLE INFO

Keywords:
High-current low-voltage DC/DC converters
Series Capacitor Buck converter
Large Hadron Collider

ABSTRACT

In this work, the main hardware design aspects of a slow-ramped DC/DC power converter prototype, developed to feed superconducting inner triplet (IT) electromagnets for the High Luminosity (HL) upgrade of the Large Hadron Collider (LHC), is presented. The proposal comprises a two-quadrant multiphase interleaved converter, based on the Series Capacitor Buck architecture, which operates at very high-current and high step-down ratio conditions. A series of innovative solutions were investigated and developed in order to fulfill the challenging aspects such as waveform quality, power loss, volume and size. All these hardware aspects are thoroughly described in the manuscript. Finally, experimental results that demonstrate the validity of the proposal are presented, operating the converter close-to-nominal conditions during power delivery and energy recovery modes. Thus, this work provides valuable information that will help researchers and engineers alike to build these type of specialized converters for future upgrades of high-energy scientific particle accelerators.

1. Introduction

Superconducting electromagnets are specialized devices used in large scientific particle accelerators, such as in the Large Hadron Collider (LHC) [1,2] at CERN, Geneva, for bending (dipoles) and focusing (quadrupoles) the trajectories of particle beams [3] running at relativistic speeds. From an electrical point of view, these loads behave as large inductances (L_{mag}) with a very small wiring resistance (R_w) [4]. Electromagnets are fundamental to make possible high energy particle-to-particle collisions at the detectors, study the resulting new particles and deepen in the knowledge of the standard model of particle physics.

High-precision switched-mode power supplies that are used to feed particle accelerator electromagnets can be broadly classified into two categories:

- Fast-ramped converters, providing very fast voltage/current transients. For example, a Marx converter is proposed by Redondo et al. in [5] for kicker magnet applications, generating pulses at 1 Hz with a 3 μs flat-top duration, and 30 ns rise- and fall-times. A pulsed power supply based on a second order LRC circuit is proposed by Liu et al. for kicker magnet powering, generating pulses at 1 MHz, with a pulse-width of less than 1 μs [6].
- Slow-ramped converters that keep a prolonged flat-top operation lasting for hours. Recently, various specialized slow-ramped converter alternatives have been reported in the literature to feed quadrupole electromagnets, such as the series capacitor buck solution originally proposed by the authors in [7], and also more conventional architectures based on the parallel connection of H-bridge converters proposed by Coulinge et al. [8,9], Garcia-Retegui, Maestri et al. [10,11] and Cao et al. [12]. In such slow-ramped applications, very low voltages are applied to slowly energize the electromagnets. This leads to the circulation of high currents throughout the magnets, which, in turn, produce the magnetic field required for focusing particles at the collision points and increase luminosity or rate-of-collisions.

The hardware development of these kind of slow-ramped power systems possess a number of challenges in terms of waveform quality (current needs to be regulated in the part-per-million or ppm range to guarantee a precise magnetic field) [13], power losses, thermal management, reliability [14] and component selection [15] (note that power semiconductor devices are susceptible to faults and play a critical role in system reliability [16]), etc., that need to be addressed

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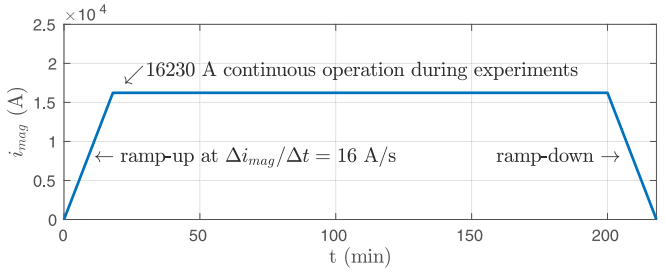
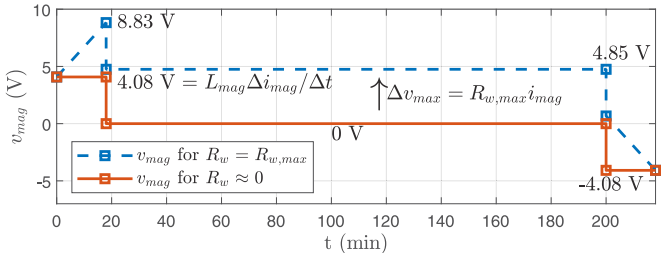
https://doi.org/10.1016/j.apenergy.2024.123730
Received 15 March 2024; Received in revised form 29 May 2024; Accepted 13 June 2024



(a) Electromagnet current profile.



(b) Voltage values to be applied by the power converter depending on the value of the wiring resistance, R_w.

Fig. 1. Typical operation profiles for powering the IT magnets of the HL-LHC. *Source:* adapted from [7]

by researchers and/or field engineers. This work aims to describe the underlying design and hardware solutions of such a challenging converter, providing a comprehensive reference document for scholars in the field of power electronics.

Fig. 1 shows the typical operation profile regarding output current and voltage for the slow-ramped powering process under study. In this particular case, the expected current and voltage profiles for the new large-aperture Niobium-Tin (Nb_3Sn) Inner Triplet (IT) superconducting electromagnets, cooled at 1.9 K and capable of producing a magnetic field of 12 T [17] for the High Luminosity (HL) upgrade of the LHC, are provided.

In the ideal absence of load resistance, the necessary voltage is shown in red in Fig. 1(b), while the dashed blue line shows the necessary voltage in a worst case scenario with estimated maximum load resistance. Three operational phases are differentiated. During the first 15 to 20 min ramp-up phase, a positive voltage is applied to energize the magnet in order to increase the magnet current. Once the current reaches its value (16.230 A), a flat-top operation is kept with a current regulation during the realization of the physics experiments, typically lasting up to 10 h. ppm precision is required during these two phases. Finally, a current ramp-down is conducted during another 15 to 20 min. Negative voltage needs to be applied for discharging the electromagnet following the reference current ramp (second-quadrant regenerative operation), until the load is discharged. The exact output voltage values depend on the value of R_w. This value, while small, is still present due to the copper connection between the novel high-temperature (50 K) Magnesium diboride (MgB_2) superconducting link and the converter [18].

In general, the power electronics systems currently feeding quadrupole superconducting electromagnets are modular solutions based on the parallel connection of one-quadrant sub-converters [19] directly fed from the grid in a single stage. However, two-stage power conversion approaches are being investigated at CERN (Fig. 2) in order to decouple the load operation from the grid and recover part of the energy stored in the magnets. In such configurations, a rectifier charges an intermediate 24 V battery pack [20] from the grid. Then, a two-quadrant multiphase DC/DC converter supplies the magnet. This DC/DC stage is constituted by m modules, occupying various rack units, while each of the modules incorporates n sub-modules, herein named cells. Then, groups of cells providing up to 2 kA are interleaved in order to reduce output voltage ripple. In [7], the utilization of the Series Capacitor Buck architecture [21] was proposed by the authors for the ramp-up and flat-top operation of the power supply [Fig. 2(b)] as an alternative to the conventional Asymmetric Bridge approach (Fig. 2(a), which can be found in [9]). The results presented in the current paper and in [7] show that the advantages achieved in high-frequency Point of Load (PoL) applications using the Series capacitor Buck converter [22,23], also known as double step-down two-phase buck [21], can also be achieved in LHC's IT magnets powering DC/DC converters. Note that, in Figs. 2(a) and 2(b), diodes can be substituted with synchronous MOSFETs in order to reduce power losses.

This two-stage approach posses a number of advantages over current technologies operating at CERN:

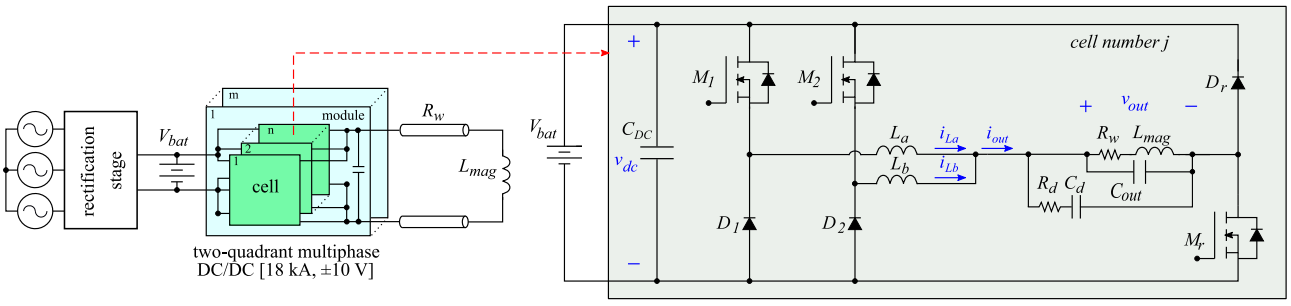
(a) The rectifier and the DC/DC stage can be optimized independently, as the battery pack can be slowly charged from the grid without considering the output magnet load dynamics [7].
(b) Significant robustness or ride-through capability against grid perturbations is achieved. This is a relevant aspect as, according to the study conducted in [24], a high percentage of faults at CERN's power systems is induced by grid disturbances.
(c) The interleaved operation of the paralleled cells enhances the quality of the synthesized output waveforms [7,9], a factor that is critical to reach the ppm requirements for the electromagnets' current [25].
(d) The power-down time of the magnets is reduced by incorporating second-quadrant operation capabilities during the current ramp-down (positive output current, negative output voltage). As R_w is too low, discharging the electromagnet by freewheeling takes an excessive amount of time. This operation mode allows to recover part of the energy stored in the electromagnets, reducing power consumption.

In this work, a proof-of-concept modular unit prototype for a complete DC/DC power supply for slow-ramped electromagnet powering, constituted by one module ($m = 1$) with $n = 4$ cells, all of them interleaved, is developed [Fig. 2(b)]. Each cell's nominal current is rated at 167 A. The adoption of 4 cells per module unit simplifies the layout of the output busbar in order to match impedances. The proposed cell topology is the Series Capacitor Buck configuration [26] [Fig. 2(b)], which was selected as the operation of the converter is improved in terms of the converter's internal inductor current ripple, output voltage ripple and efficiency [7].

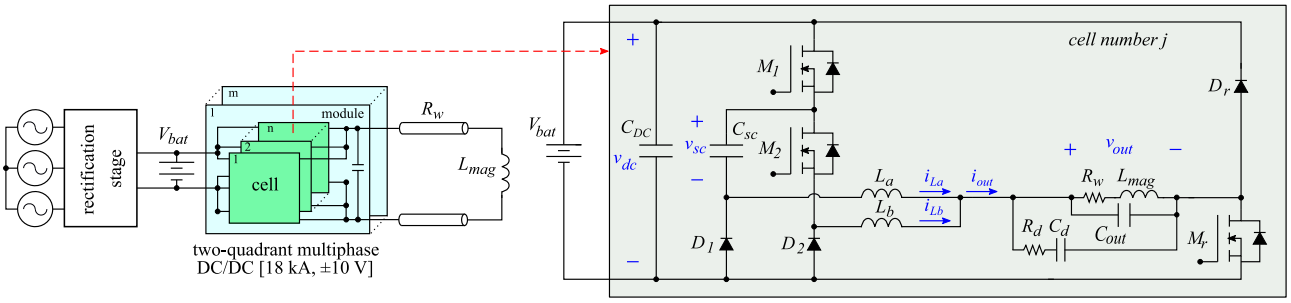
In the following, this paper describes the operation principles of the proposed DC/DC power converter architecture for superconducting electromagnet powering and compares its figures-of-merit vs the conventional interleaved Buck architecture. The advantages of the selected approach are then highlighted, and its utilization for the IT magnets powering is justified. After that, the main hardware design aspects of a novel proof-of-concept converter, including the aforementioned two-quadrant operation capabilities (Buck and energy recovery modes), are presented. The main hardware elements and the innovative solutions developed during the investigation are outlined. Finally, a number of representative experimental results that validate the proposal are provided.

2. Description of the proposed two-quadrant power converter architecture and its operating principles

The Series Capacitor Buck was introduced by Shenoy in PoL applications [27] as an improvement over traditional Buck converters that require very high step-down ratios [28]. It is derived from a conventional interleaved two-phase Buck, connecting in series the two

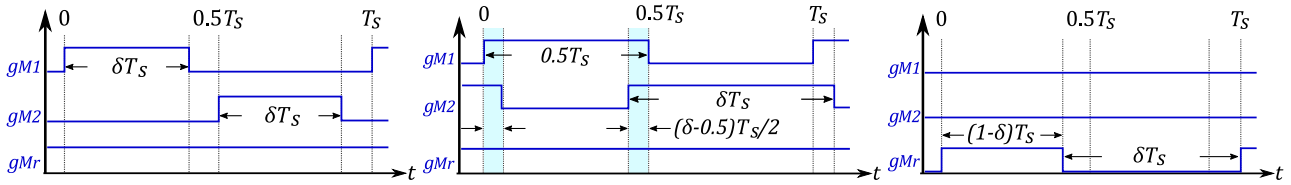


(a) Conventional Asymmetric Bridge solution.



(b) Proposed Series Capacitor Buck solution.

Fig. 2. IT magnet powering strategies.



(a) $\delta < 50\%$. (b) $\delta > 50\%$. (c) Energy recovery.

Fig. 3. Firing signals of the proposed converter architecture operation modes.

main switches and introducing a series capacitor, C_{sc}, between the switch and the corresponding diode of the first branch, M_1 and D_1 [Fig. 2(b)].

The DC/DC converter stage in the first quadrant operation is controlled using a novel algorithm that regulates the output voltage while it interleaves and balances all $n = 4$ cell currents [7]. Bearing in mind that each Series Capacitor Buck cell automatically interleaves and balances two inductor currents, the result is the interleaving of 8 output inductor currents using only 4 current sensors.

2.1. Operation principles

There are three PWM modulation modes for the MOSFETs' gate signals (g_{Mj}), illustrated in Fig. 3, for the proposed converter: two during Buck operation and one during energy recovery or power-down.

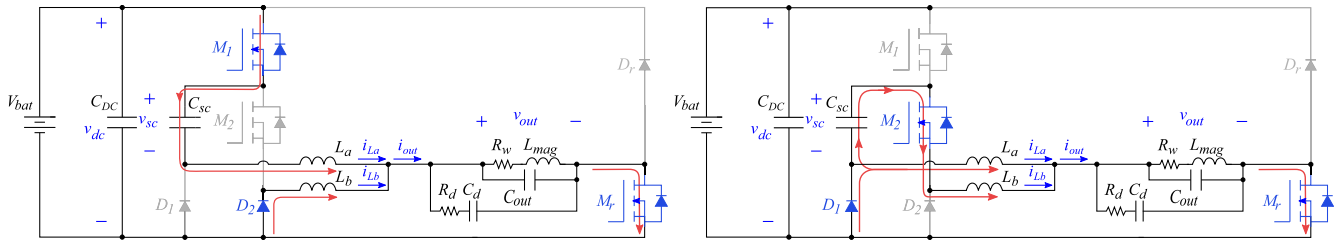
2.1.1. 1st quadrant operation with $\delta < 0.5$

During ramp-up and flat-top operation, the DC/DC converter operates in Buck mode, drawing power from the batteries to the magnet and having the MOSFET M_r continuously on and diode D_r off. In general, the required high step-down ratio demands duty-cycles lower than 50%. The PWM is applied symmetrically to switches M_1 and M_2, as shown in Fig. 3(a). This operation condition is applied during flat-top and most part of the ramp-up period. The power supply will work around 97% of its operational time in this mode (Fig. 1). This is the region where most of the energy is required and when the tight output voltage ppm-precision requirements must be met. For these reasons, the proposed converter is optimized for these conditions. Regarding modulation, a conventional PWM pattern is applied to the semiconductors, reaching typical four-stage steady-state operation (Fig. 4). M_1 and M_2 MOSFETs are turned on for a time $t_{on} = \delta T_{sw}$, and phase shifted 180° [Fig. 6(a)]. As a result, the two inductor currents within each Series Capacitor Buck cell become naturally balanced [$avg(i_{La}) = avg(i_{Lb})$].

The main waveforms under this operation mode are shown in Fig. 6(a). The operation stages are depicted in Fig. 4. In the first stage [Fig. 4(a)], during $0 < t < \delta T_{sw}$, transistor M_1 is carrying the phase one current and starts charging the series capacitor C_s, while D_2 is carrying the current of phase two. Next, in stage two [Fig. 4(b)], during $\delta T_{sw} < t < 0.5T_{sw}$, current in both phases circulates through D_1 and D_2. Then, in stage three [Fig. 4(c)], during $0.5T_{sw} < t < 0.5T_{sw} + \delta T_{sw}$, the series capacitor discharges through M_2, and D_1 briefly carries the current of both phases. Finally, while $0.5T_{sw} + \delta T_{sw} < t < T_{sw}$, the converter transitions to stage four [Fig. 4(b)], which is identical to stage two.

2.1.2. 1st quadrant operation with $\delta > 0.5$

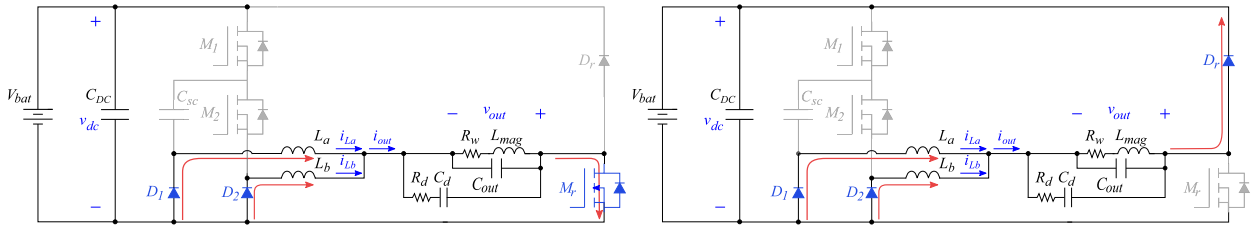
During the final phase of ramp-up, in order to overcome the resistive voltage drop due to the high value of the current, high output positive voltage may be needed ($V_{out} > V_{bat}/4$). These high output voltage values may require duty-cycle values higher than 50%. Using conventional Series Capacitor Buck PWM modulation, duty-cycles higher than 50%



(a) Stage 1 - Buck mode ($0 < t < \delta T_{sw}$). (b) Stage 3 - Buck mode ($0.5T_{sw} < t < 0.5T_{sw} + \delta T_{sw}$).

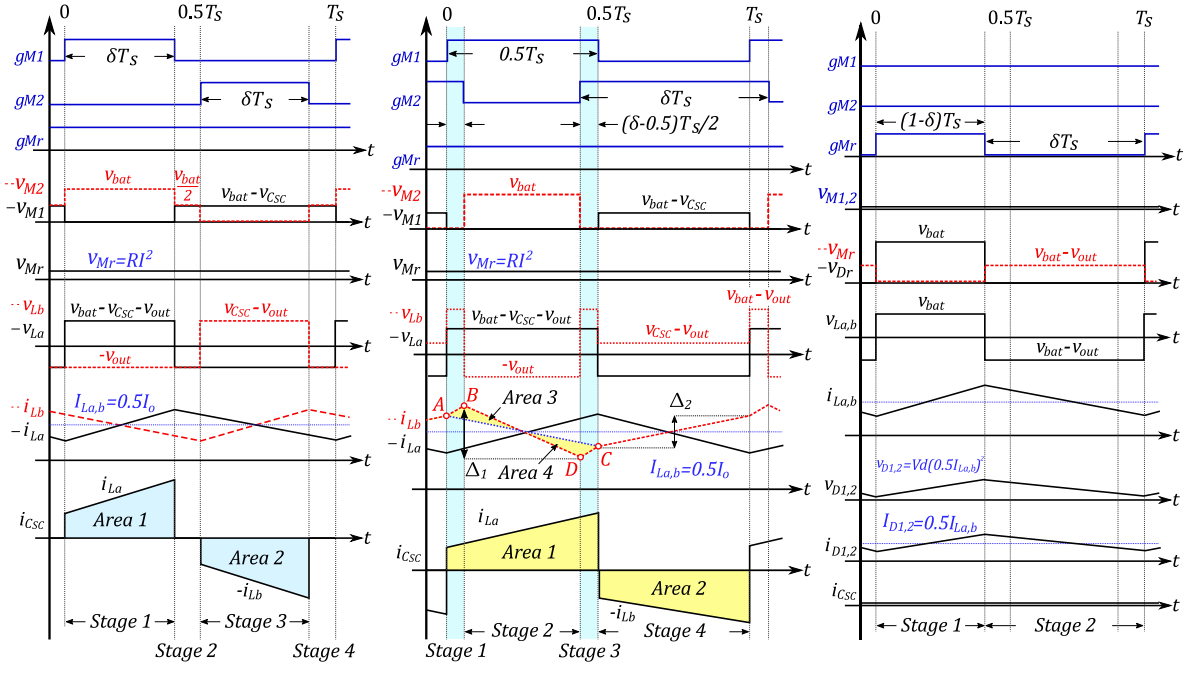
(c) Stages 2 and 4 - Buck mode ($\delta T_{sw} < t < 0.5T_{sw}$) and ($0.5T_{sw}+\delta T_{sw} < t < T_{sw}$).

Fig. 4. Operation stages in 1st quadrant Series Capacitor Buck mode.



(a) Stage 1 - Energy recovery ($0 < t < \delta T_{sw}$) (b) Stages 2 and 4 - Energy recovery ($\delta T_{sw} < t < T_{sw}$)

Fig. 5. Operation stages in 2nd quadrant energy recovery mode.



(a) 1st quadrant $\delta < 50\%$. (b) 1st quadrant $\delta > 50\%$. (c) 2nd quad. energy recovery.

Fig. 6. Waveforms of the proposed converter architecture operation modes.

lead to current unbalance in the two inductors of the cell. In order to avoid this current unbalance, an extended duty-cycle modulation pattern, proposed in [29], is implemented. The modification of the PWM modulation allows to maintain the current balance in both inductors. In this asymmetrical PWM scheme used when $\delta > 0.5$, the duty-cycle of M_1 is locked to the value of 50%, and the required duty-cycle, higher than 50%, is only applied to M_2. The additional duty-cycle above 50% in M_2 is added symmetrically between the start and the end of the conduction period of M_2 [see Fig. 3(b)]. This mode allows to achieve output voltages up to 10 V using $\delta > 0.5$ and still maintaining current balance in the inductors in the Series Capacitor Buck cell. The main waveforms under this working conditions are shown in Fig. 6(b). Operation is very similar to the previous mode and is not further discussed.

2.1.3. 2nd quadrant operation

The magnets need to be discharged with a controlled current ramp-down, at a defined rate, in order to recover part of the energy stored in them. Therefore, the power supply has to work in the second-quadrant applying a negative voltage at the output. In this energy recovery situation, M_1 and M_2 switches are deactivated and diodes D_1 and D_2 freewheel the current in inductors L_a and L_b, respectively (Fig. 5). All the M_r switches are simultaneously activated/deactivated with duty-cycle $1-\delta$ [see Fig. 3(c)], provided by the voltage control loop of the algorithm proposed in [7]. During this operation mode no interleaving pattern is utilized in order to simplify the control system. No special regulation requirements apply here, apart from guaranteeing a safe turn-off of the system. Current balancing between cells relies on a convenient impedance matching of the current paths. In this mode the converter operates as a conventional Boost (see Fig. 5). The main waveforms under this regime are shown in Fig. 6(c).

2.2. Main operational characteristics in 1st quadrant operation with $\delta < 0.5$

As previously mentioned, the converter operates approximately 97% of the time in 1st quadrant with a value of $\delta < 0.5$, and the converter was optimized for the operation in this region. Table 1 compares the main ideal theoretical values and figures-of-merit of the interleaved two phase Buck converter and the Series Capacitor Buck converter in this operation mode.

The main benefits of the Series Capacitor Buck over the conventional interleaved Buck are:

1. For the same duty-cycle, the step-down ratio of the Series Capacitor Buck converter is twice higher. Thus, for a given output voltage reference, the duty-cycle δ required is doubled compared to a conventional Buck converter, which brings better use of the semiconductor switches as well as better regulation while working with very high step-down voltage conversion ratios. As an example, for an output voltage of 4.5 V, at nominal cell current of 167 A, the duty-cycle required by the conventional Buck converter is 20.8%, compared to the 42.8% of the Series Capacitor Buck.
2. The current between the two inductors is naturally balanced in the Series Capacitor Buck converter, thus only one current sensor is needed per cell. This reduces by half the sensor requirements when a high number of cells, $n \times m$, must be integrated, and it also decreases the current balancing regulation loop count, leading to a lower software complexity and computational burden.
3. The inductors' current ripple is considerably lower in the Series Capacitor Buck converter. Such inductor current ripple reduction gives the possibility to choose a lower inductance value to meet the same maximum ripple constraint, thus reducing costs and size. This fact is highlighted in the comparison chart where the two-phase Buck presents a peak-to-peak value of inductor ripple of 20.0 A, and the Series Capacitor Buck 15.54 A, a reduction of 23%, for the aforementioned particular operating point.

Table 1
2-phase interleaved Buck vs Series Capacitor Buck theoretical ideal characteristics comparison.

Figure	Buck 2-phase	Series capacitor Buck
V_{out}	$V_{bat} \cdot \delta$	$\frac{V_{bat} \cdot \delta}{2}$
$I_{L1,L2}\langle RMS\rangle$	$\frac{I_{out}}{2}$	$\frac{I_{out}}{2}$
$I_{M1}\langle RMS\rangle$	$\frac{I_{out}}{2} \cdot \sqrt{\delta}$	$\frac{I_{out}}{2} \cdot \sqrt{\delta}$
$I_{M2}\langle RMS\rangle$	$\frac{I_{out}}{2} \cdot \sqrt{\delta}$	$\frac{I_{out}}{2} \cdot \sqrt{\delta}$
$I_{D1}\langle RMS\rangle$	$\frac{I_{out}}{2} \cdot \sqrt{1-\delta}$	$\frac{I_{out}}{2} \cdot (1+2\delta) \cdot \sqrt{1-\delta}$
$I_{D2}\langle RMS\rangle$	$\frac{I_{out}}{2} \cdot \sqrt{1-\delta}$	$\frac{I_{out}}{2} \cdot \sqrt{1-\delta}$
ΔI_L	$\frac{(V_{bat}-V_{out}) \cdot \delta \cdot T_{sw}}{2L}$	$\frac{\left(\frac{V_{bat}}{2}-V_{out}\right) \cdot \delta \cdot T_{sw}}{2L}$
$V_{C_{SC}}$	-	$\frac{V_{bat}}{2}$
$I_{C_{SC}}\langle RMS\rangle$	$\frac{I_{out}}{2}$	$\frac{I_{out}}{2}$
V_{M1} [a]	V_{bat}	$\frac{V_{bat}}{2}$
V_{M2} [a]	V_{bat}	$\frac{V_{bat}}{2}$
V_{D1} [a]	V_{bat}	$\frac{V_{bat}}{2}$
V_{D2} [a]	V_{bat}	$\frac{V_{bat}}{2}$
P_{M1}	$R_{DS(on)} \cdot I^2_{M1}\langle RMS\rangle$	$R_{DS(on)} \cdot I^2_{M1}\langle RMS\rangle$
P_{M2}	$R_{DS(on)} \cdot I^2_{M2}\langle RMS\rangle$	$R_{DS(on)} \cdot I^2_{M2}\langle RMS\rangle$
P_{D1}	$V_D \cdot I_{D1}\langle RMS\rangle$	$V_D \cdot I_{D1}\langle RMS\rangle$
P_{D2}	$V_D \cdot I_{D2}\langle RMS\rangle$	$V_D \cdot I_{D2}\langle RMS\rangle$
$P_{C_{SC}}$	-	$R_{ESR} \cdot I^2_{C_{SC}}\langle RMS\rangle$

[a] Voltage in switches at commutation.

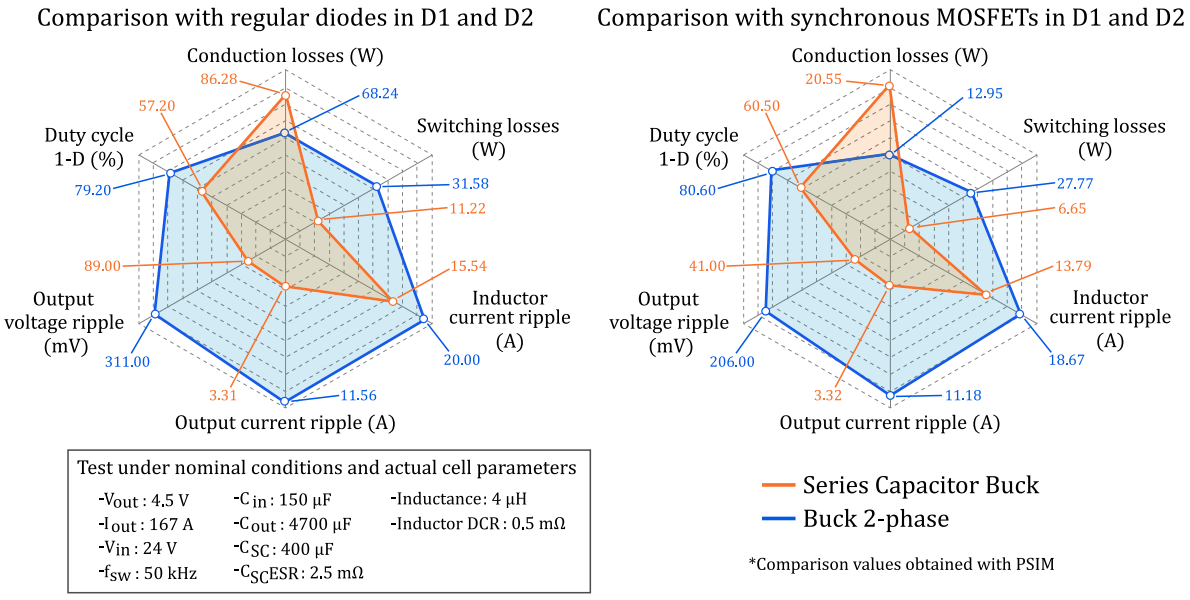
4. The voltage in the semiconductors at the commutation instants is lower, thus the switching losses are reduced. This allows the selection of lower voltage grade semiconductors, usually resulting in better R_{ds} values to choose, improving power losses. Indeed, in the proof-of-concept prototype of this proposal, 40 V grade MOSFETs could be selected (IXTN660N04T4) with $R_{DSon} = 0.85$ mΩ instead of 75 V MOSFETs (IXFN520N075T2) with $R_{DSon} = 1.9$ mΩ.

Fig. 7 compares the key converter features obtained when using a conventional two-phase interleaved Buck architecture vs the proposed Series Capacitor Buck configuration under electromagnet powering nominal working conditions. These figures were estimated by simulating both architectures in PSIM. IXTN660N04T4 MOSFET and DSS2X121-0045B diode parameters were used for power loss analysis in the model. Note that, for this power loss analysis, only the buck stage was considered (i.e. elements M_1, M_2, D_1, D_2, L_a, L_b and C_{SC} for the series capacitor buck) as the energy recovery stage (i.e. elements M_r and D_r) is equivalent for both systems. Resistive power losses in busbars are neither being considered for the shake of simplicity.

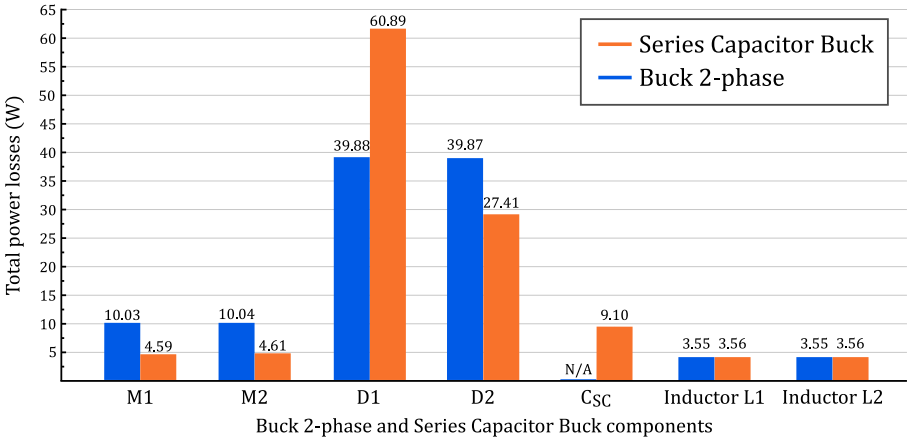
Two hardware scenarios were considered:

(a) Both studied converters incorporating ultra-fast diodes to constitute elements D_1 and D_2, as is the case in the proof-of-concept prototype developed within this work.
(b) Substituting the aforementioned diodes by synchronous MOSFETs.

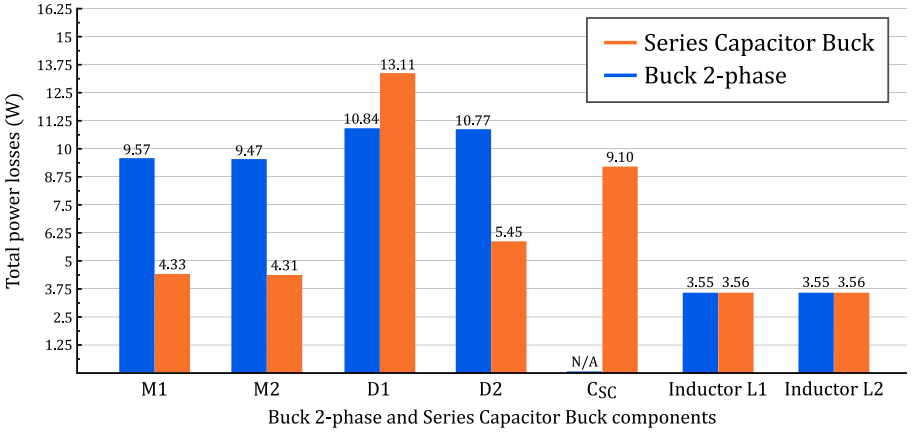
In both case studies, two main drawbacks are present in the Series Capacitor Buck. The converter requires an additional capacitor, C_{sc}, and the diode D_1 must carry a considerable amount of current, and high power losses are concentrated in these elements [Figs. 7(b) and 7(c)]. What is more, following the synchronous MOSFETs approach, the Series Capacitor Buck stands out as a more efficient topology at nominal operating conditions. Power losses in element D_1 are significantly reduced, resulting in similar losses in D_1 as with the two-phase Buck configuration [Fig. 7(c)]. In addition, losses become lower in diode D_2 than with the conventional two-phase Buck. In total, the Series



(a) Two-phase interleaved Buck vs Series Capacitor Buck comparison charts, at nominal conditions, with regular diodes (left) and synchronous MOSFETs (right).

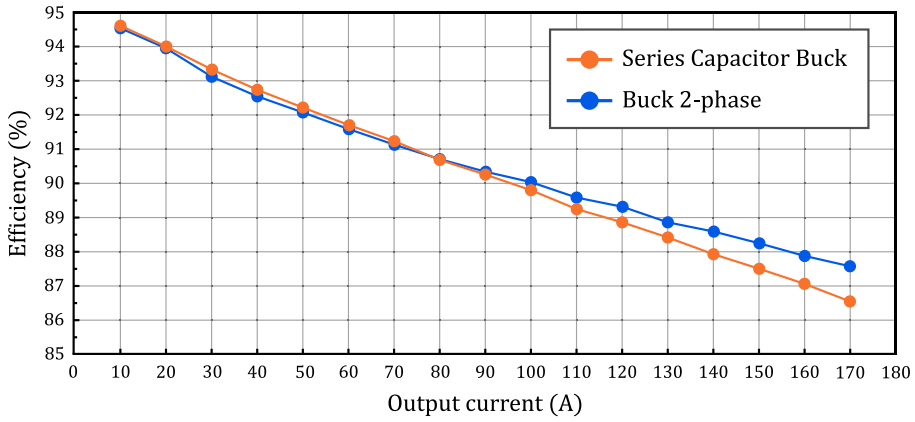


(b) Two-phase interleaved Buck vs Series Capacitor Buck power losses distribution chart, considering regular diodes.

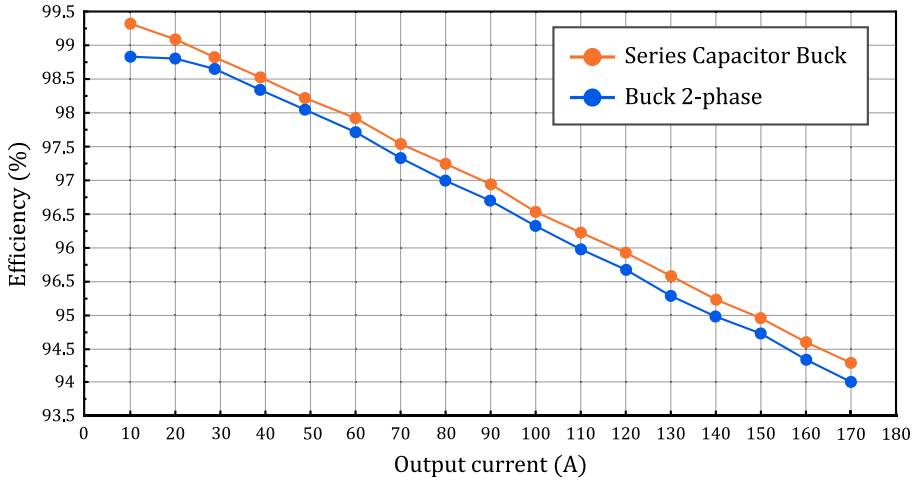


(c) Two-phase interleaved Buck vs Series Capacitor Buck power losses distribution chart, considering synchronous MOSFETs.

Fig. 7. Power loss comparison charts: two-phase interleaved Buck vs Series Capacitor Buck.



(a) Estimated efficiencies considering regular diodes.



(b) Estimated efficiencies considering synchronous MOSFETs.

Fig. 8. Efficiency comparison charts for nominal output voltage: Two-phase interleaved Buck vs Series Capacitor Buck.

Capacitor Buck exhibits 43.41 W of overall power losses vs 47.76 W for the two-phase Buck.

Furthermore, Fig. 8 compares the estimated efficiencies of the two-phase Buck and the Series Capacitor Buck architectures, operating at nominal output voltage conditions, but considering a wide range of output current values. Again, it is corroborated that the efficiency of the Series Capacitor based solution is higher when synchronous MOSFETs are incorporated.

All the above simulation results show that, in general, benefits of the Series Capacitor based approach are considerably higher than the drawbacks. All this justifies the adoption of the Series Capacitor Buck as an alternative to the conventional interleaved Buck DC/DC.

It is important to highlight that, as a proof-of-concept prototype, conventional diodes were used in this work to simplify the hardware design and its control. However, in the light of these comparative results, synchronous MOSFETs should be implemented in further iterations of an industrializable prototype version targeting the final application.

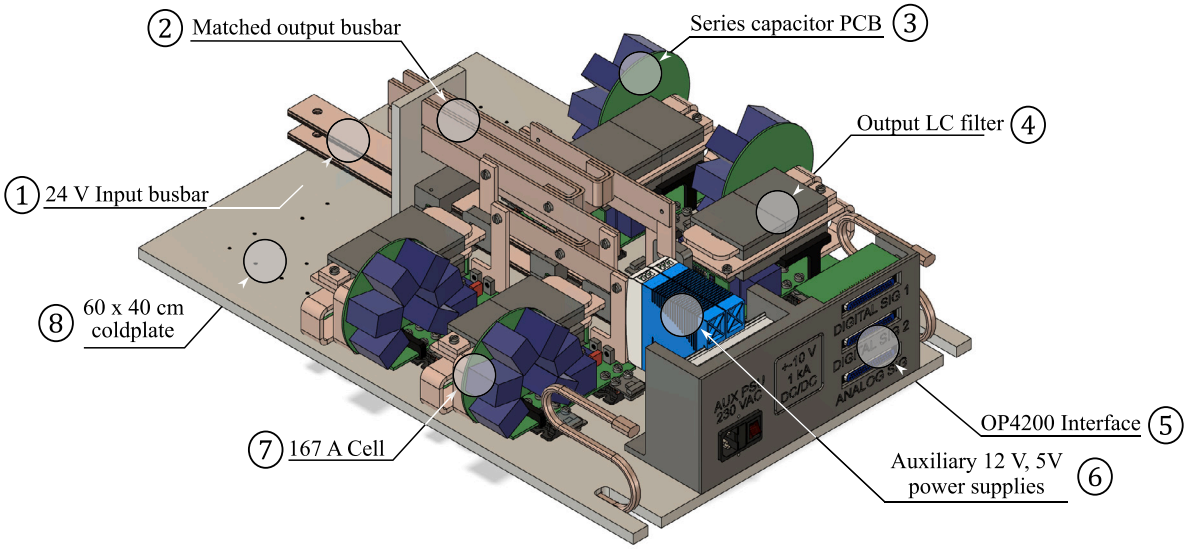
3. Hardware design aspects of the developed power converter prototype

In this section, the most relevant hardware design aspects of the developed 687 A rated proof-of-concept power converter module (m = 1, n = 4) are presented. A general overview of the converter's layout is provided first. Then, the design of each single power cell unit is described. Details on the power inductors' design, and the developed daisy chain PCB configuration for the series capacitor element C_{sc} are shown, as these are critical parts of the hardware proposal. Finally, the output LC stage implementation is discussed.

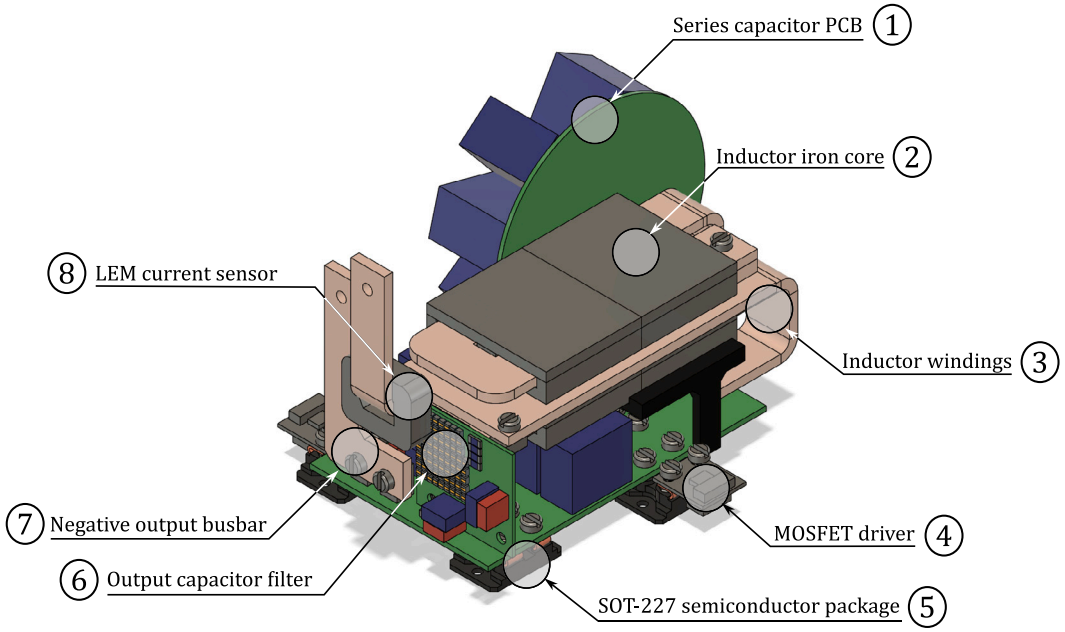
One of the main design parameters is the switching frequency of the converter. In a preliminary analysis, the switching frequency f_{sw} was selected pursuing a trade-off between power losses and the size of the magnetic components. In order to use available off-the-shelf standard ferrite cores, to limit cost, and minimize conduction power loss in inductors, a single turn inductor design was selected. As a result, a value of f_{sw} = 50 kHz was chosen, which provides a good trade-off between size, cost and power losses. In the final product, in order to achieve a 2 kA interleaved converter, 12 Series Capacitor Buck interleaved cells will provide an equivalent 50 kHz × 12 × 2 = 1.2 MHz output current ripple.

3.1. Overview of the power converter layout

Fig. 9(a) shows the 3D CAD layout of the proposed hardware unit with 4 Series Capacitor Buck cells. Each of the four paralleled cells is connected to the 24 V input port through a common input side busbar [Fig. 9(a), item number 1 - note that, in the following, items refer to hardware design areas indicated by encircled numbers within figures]. Each Series Capacitor Cell unit is connected to a custom laser-cut copper, in order to match in length, i.e. resistance, among cells [Fig. 9(a), item 2]. Thus, minimally unbalanced impedance among cells is guaranteed. This results in very close duty-cycle values from the four active closed-loop current balancing loops [7] during Buck operation



(a) General overview of a 667 A power converter unit.



(b) Detail of a 167 A single-cell unit.

Fig. 9. 3D CAD layout of the proposed power converter hardware architecture.

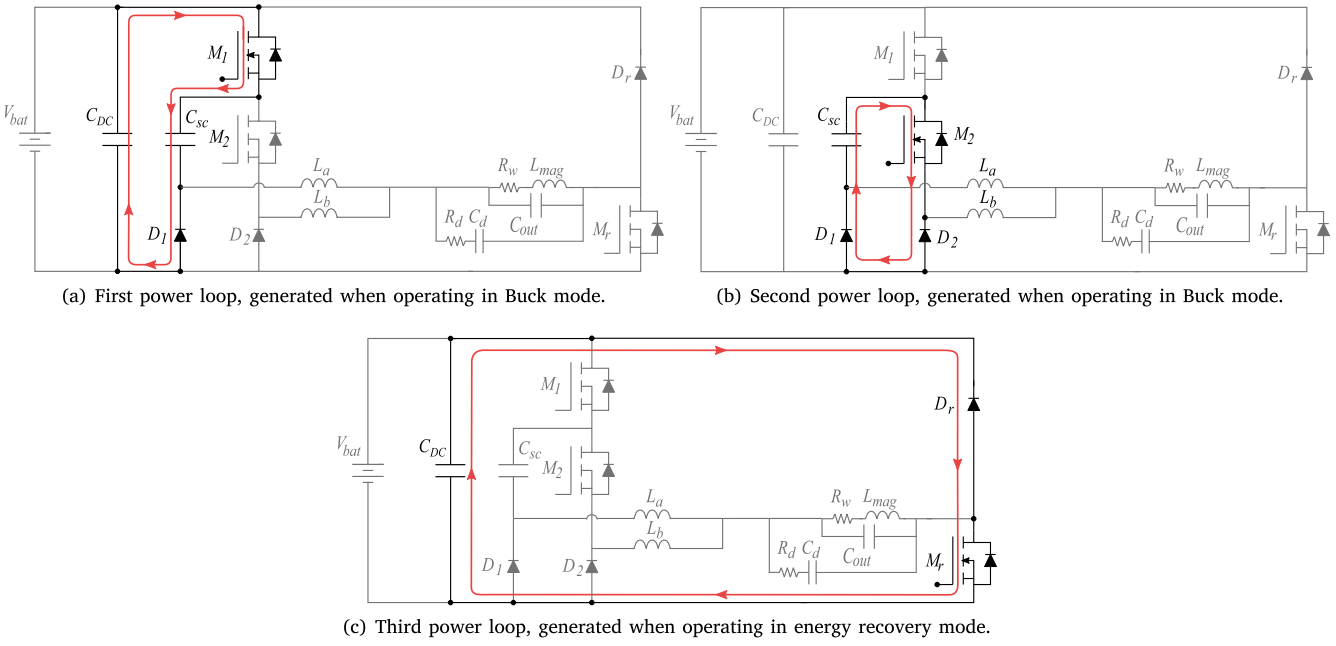
(Section 4.2), leading to improved output voltage ripple results. This design aspect is also critical for the energy recovery mode (second quadrant operation), were cells' current balance relies on impedance matching, as no closed-loop current regulation algorithm is enabled.

Thermal management of power semiconductors is done, according to CERN specifications, by incorporating a liquid-cooled heat-sink [see Fig. 9(a), item number 8] using, in this particular laboratory setup, a 50% water 50% ethylene-glycol cooling liquid, with a flux-rate of 2.4 l/min. The base-plate has a total surface of 40 × 60 cm, covering the surface area of a single rack unit. It provides fitting to all the elements that constitute the developed power conversion unit. Ancillary power supplies of 12 V and 5 V are located up front of the prototype, mounted in a 3D-printed front panel [Fig. 9(a), item number 6]. These low-power DC supplies provide energy to the drivers and measurement electronics, connected to the digital control platform through DB37 connection ports [Fig. 9(a), item 5].

The four individual power cell units [Fig. 9(a), item number 7], rated at 167 A, are the main components of the power converter design. Each cell comprises a single two-quadrant DC/DC [Fig. 9(b)], including a main power PCB, the series capacitor PCB, two power inductors, an output capacitor bank PCB, and individual PCBs for the MOSFET drivers [Fig. 9(b), item 4]. Such a modular design was chosen to allow an easy and fast element replacement in case of any problem. Finally, special care must be taken when designing and selecting the most critical elements due to the special requirements of the application. These relevant parts and their design guidelines are explained in the next sections.

3.2. Printed circuit board traces

Regarding PCB traces, mean per-phase output current values up to 85 A_{rms} circulate through them due to the two-phase nature of the



(a) First power loop, generated when operating in Buck mode.

(b) Second power loop, generated when operating in Buck mode.

(c) Third power loop, generated when operating in energy recovery mode.

Fig. 10. Main AC power loops within the converter's individual cells.

Table 2
Cell and series capacitor PCB stackups.

Layer	Cell PCB stackup	Series capacitor PCB stackup
	Thickness (μm)	
Silkscreen - Top side	–	–
Soldermask - Top side	20	20
Copper - Top side	400	400
Prepreg	95	95
FR-4	540	2140
Prepreg	95	95
Copper - Bottom side	400	400
Soldermask - Bottom side	20	20
Silkscreen - Bottom side	–	–
Total thickness	1570	3170

proposed power cell. Consequently, copper layers were designed with a thickness of 400 μm. Table 2 summarizes all thicknesses of the PCB stackups.

The minimization of the parasitic elements, specially inductances, within the AC power loops is crucial when designing power PCBs [30], requiring the estimation of the parasitic inductance through 2-D analysis [31], or following parameter-oriented methodologies [32]. During semiconductors' turn-on and turn-off processes, large AC voltages and currents can be generated due to such parasitic inductances. As a result, harmful Electromagnetic Interferences (EMI) may appear, extra power losses are generated, and even the integrity of the converter can be jeopardized if excessive voltage/current spikes are produced.

Fig. 10 shows the three main AC power loops present in the proposed cell unit. The first one comprises the input capacitor C_{DC}, transistor M_1, series capacitor C_{sc} and diode D_1 [Fig. 10(a)]. The second one comprises C_{sc}, transistor M_2 and diodes D_1 and D_2 [Fig. 10(b)]. Both loops are present when the converter operates in Buck mode. In contrast, when the converter works in energy recovery mode, the main loop is formed by the input capacitor bank C_{DC}, transistor M_r and diode D_r [Fig. 10(c)].

To guarantee that the designed PCB exhibits acceptable inductance levels within these power loops, such parasitic inductances were estimated using the Keysight Pathwave Advanced Design System (ADS) software. The study was carried out across a wide frequency spectrum up to 1 MHz. Using an iterative design process, with component size and PCB traces' current capability constraints, a PCB with low switching loop inductances was achieved.

For the particular switching frequency of 50 kHz, estimated parasitic inductances and resistances of 10.91 nH and 0.598 mΩ were obtained for the first power loop on the final PCB design [Figs. 11(a) and 11(b)]. Values of 10.92 nH and 0.597 mΩ were obtained for loop number two [Figs. 11(c) and 11(d)]. Finally, impedance values of 13.15 nH and 1.143 mΩ where obtained for the power loop that corresponds to the energy recovery operation mode [Figs. 11(e) and 11(f)]. For frequencies higher than the switching frequency of 50 kHz, these values slightly decrease. These parasitic inductances are considered sufficiently low for the application

These values were obtained performing the calculation of scattering parameters (S-parameters) of the PCB traces [33,34] in the Keysight Pathwave ADS simulation tool:

$$S_{ij} = \frac{V_i^-}{V_j^+}\Big|_{V_k^+ = 0 \ for \ k \neq j}, \tag{1}$$

where S_{ij} are the elements of the $i \times j$ scattering matrix $\mathbf{S}$. These are obtained by driving port j of the circuit with an incident voltage wave V_j^+, and by determining the reflected wave V_i^-, coming out of port i. Then, the Y-parameters of the admittance matrix $\mathbf{Y}$ can be extracted from:

$$Y_{ij} = \frac{I_i}{V_j}\Big|_{V_k^+ = 0 \ for \ k \neq j}, \tag{2}$$

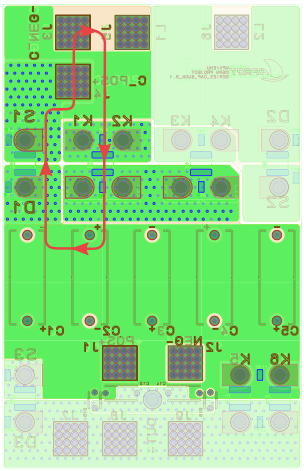
where Y_{ij} are the elements of $\mathbf{Y}$, and V_j and I_i are the voltage and current in ports j and i, respectively.

Finally, the resistance and inductance values are estimated from the admittance Y_{11}:

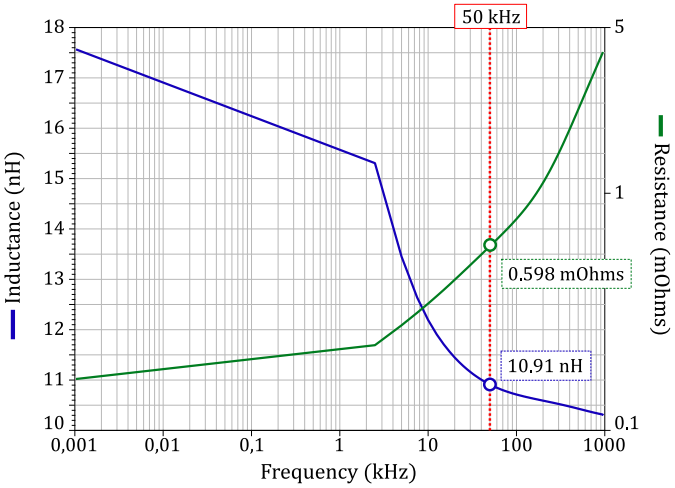
$$R = \Re\left(\frac{1}{Y_{11}}\right), \tag{3}$$

$$L = \frac{\Im(\frac{1}{Y_{11}})}{2\pi f}, \tag{4}$$

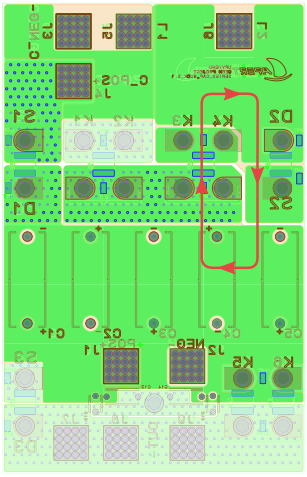
where $\Re(1/Y_{11})$ and $\Im(1/Y_{11})$ are the real and imaginary parts of the inverse of the admittance Y_{11}, and f is the frequency under study.



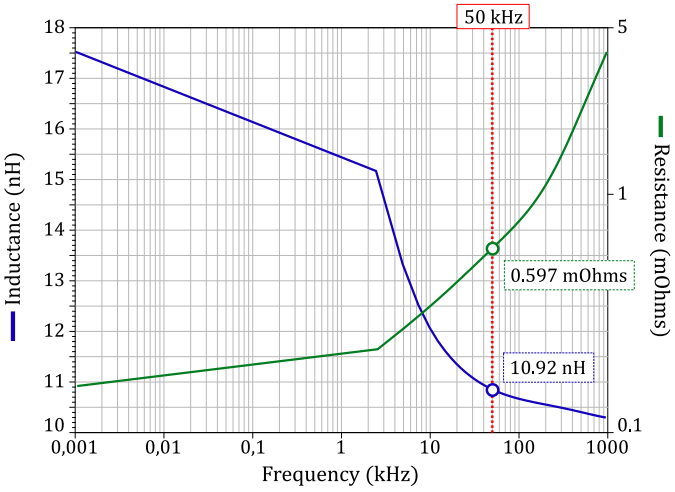
(a) First PCB AC power loop (Buck mode).



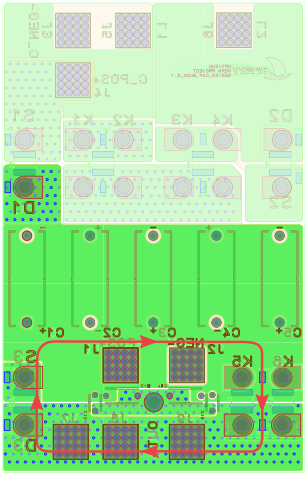
(b) First AC power loop impedance chart (Buck mode).



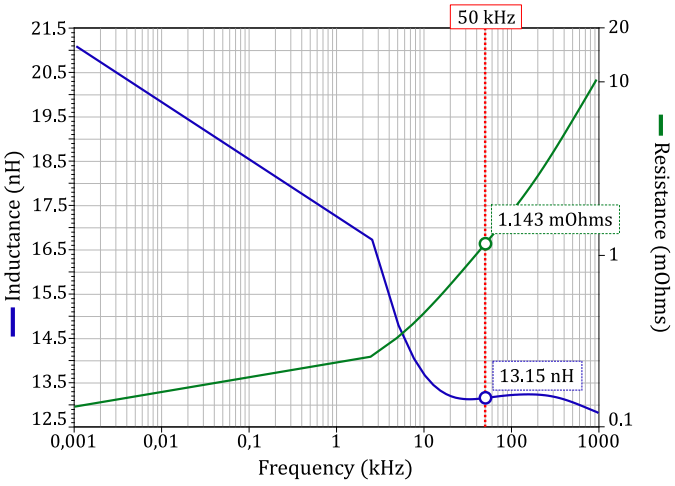
(c) Second PCB AC power loop (Buck mode).



(d) Second AC power loop impedance chart (Buck mode).

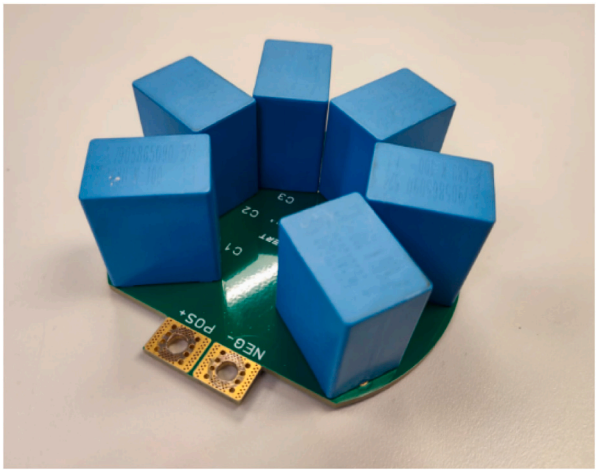


(e) PCB AC power loop in energy recovery mode.

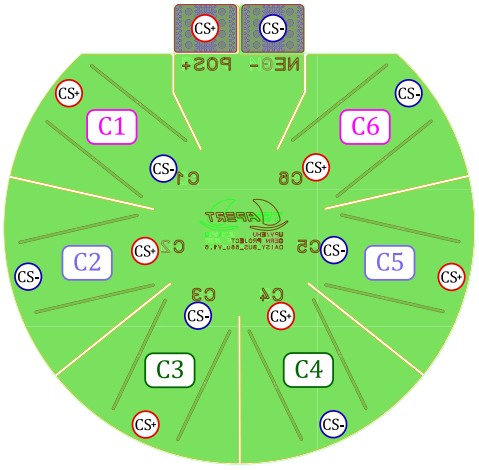


(f) AC power loop impedance chart for energy recovery mode.

Fig. 11. Power loops and impedance charts in Buck and energy recovery modes of the converter.



(a) Built Series Capacitor in the proposed daisy array configuration.



(b) Current distribution in the Series Capacitor PCB.

Fig. 12. Proposed series capacitor circuit with paralleled film capacitors in daisy array configuration.

3.3. Selection of power semiconductors

Regarding the selection of power semiconductors, the required maximum blocking voltage and circulating current values were considered first. Silicon based IXTN660N04T4 power MOSFETs from IXYS, with $V_{DS,max}$ = 40 V and $R_{DS(on)}$ = 0.85 mΩ, meet the aforementioned requirements, and were selected for M_1, M_2 and M_r. Power diodes DSS2X121-0045B, with $V_{rrm,max}$ = 45 V, V_F = 0.59 V and R_F = 2.6 mΩ, were chosen for D_1, D_2 and D_r. Special care was taken in facilitating installation and maintenance duties. Their SOT-227 (*miniBLOC*) encapsulation makes them attractive for mounting them to the PCB and the heat-sink [Fig. 9(b), item number 5]. These devices are rated to avoid potential long term thermal issues, minimize breakages and guarantee a prolonged life-cycle. It must be borne in mind that accessing the LHC tunnels between experiments to substitute broken power electronics elements needs to be minimized in time and keep staff's exposure to radiation under safe limits. Miniblock housing semiconductors were chosen in order to ease the connection to the cold plate and substitution of devices. In the final product these devices can be substituted by equivalent SMD devices if cost and manufacturing requirements demand so. However, contact between the SMD devices and the cold-plate must be carefully studied.

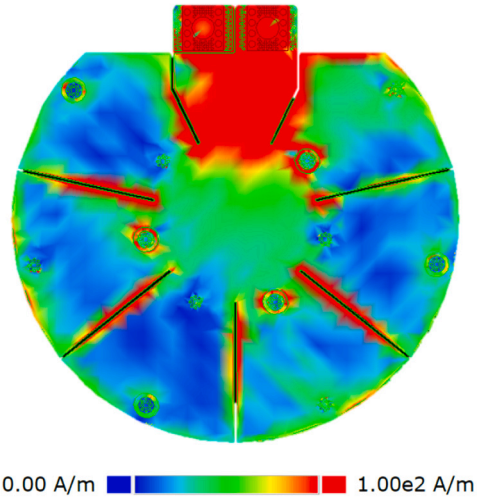


Fig. 13. Series Capacitor PCB current density.

3.4. Series capacitor daisy configuration

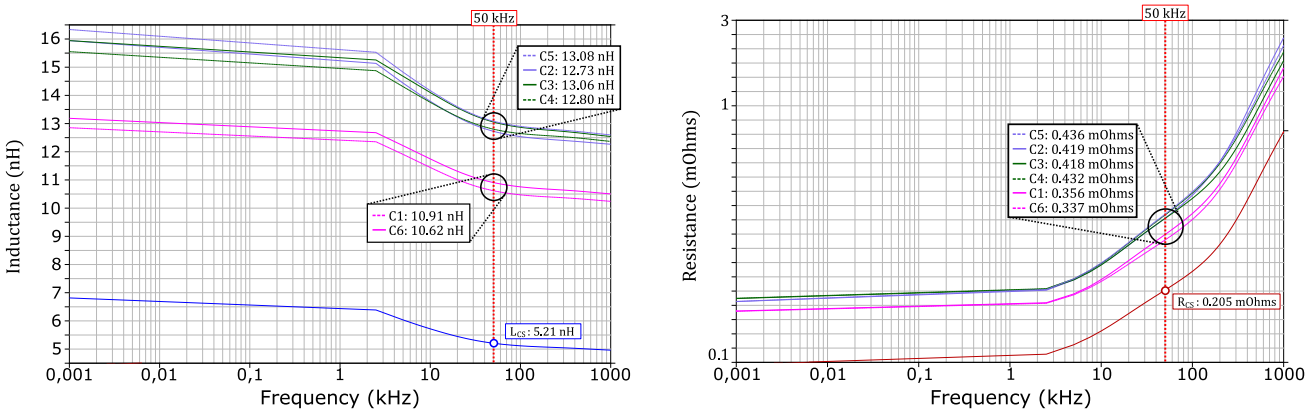
Considering the selected switching frequency of 50 kHz, a capacitance value of 400 μF was chosen for the series capacitor C_{sc}, as a trade-off between the capacitor's size and voltage ripple. This element must provide very high current rating, up to 85 A_{rms}. In this particular case, it is not possible to comply with this capacitance/current rating requirements mounting a single capacitor, since its volume would be unreasonable. Paralleling multiple film capacitors is an effective solution, which is cheaper and better in terms of Equivalent Series Resistance (ESR) and inductance (ESL).

From a mechanical point of view, capacitor C_{sc} was mounted in a separated PCB [Fig. 9(b), item number 1]. This approach improves modularity. In addition, it provides flexibility for attaching the element to the cell's main PCB. A vertical layout was followed to take advantage of the remaining available space and comply with the surface and volume constraints of the application.

One of the most challenging parts for the successful implementation of the proposed architecture was the design of the mounting PCB for this critical element. As C_{sc} is present in the AC power loops during Buck operation (Section 3.2), many considerations needed to be taken, since it may include additional parasitics, such as inductance or extra resistance from connectors, PCB traces, and capacitor' leads. This element introduces additional power losses that have to be minimized and thermally managed. To overcome the aforementioned problems, a novel approach regarding the layout of C_{sc} was taken. A daisy layout was proposed [Fig. 12(a)].

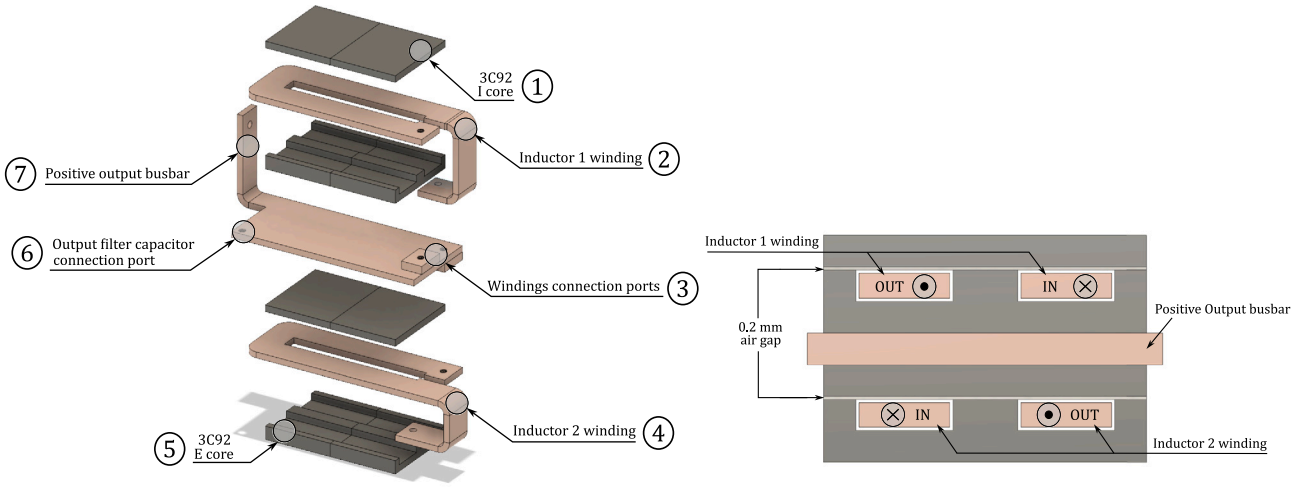
This daisy arrangement avoids the most common issue present in linear capacitor distribution, i.e., having a few of them carrying the majority of the current (typically the ones closer to the terminals). In the proposal, the capacitors were set at almost the same distances from the terminals of the PCB, as well as alternating the polarity of their mounting holes [Fig. 12(b)]. This way, an even current flows among all of them, achieving a uniform temperature gradient (see the finite element simulation results of Fig. 13). Therefore, a reliable operation of this critical element is to be expected in the long term.

The parasitic impedances in the proposed daisy array configuration PCB were estimated with the Keysight Pathwave ADS software. Simulation results at 50 kHz show similar figures for all PCB traces: inductance and resistance values of 13 nH and 0.42 mΩ for C2, C3, C4 and C5, and slightly smaller values of around 10.75 nH and 0.34 mΩ for C1 and C6



(a) Series capacitor's inductance chart. (b) Series capacitor's resistance chart.

Fig. 14. Series capacitor's impedance charts.



(a) Power inductors set's exploded view. (b) Power inductors' section view.

Fig. 15. Power inductors architecture.

[Fig. 14(a)]. Note that C1 and C6 are the ones slightly closer to the PCB terminals. Regarding the whole capacitors' PCB, parasitic inductance and resistance values of 5.21 nH and 0.205 mΩ were determined by the software, respectively.

3.5. Output inductors and capacitor stage

The output power inductors [two per cell, Fig. 2(b)], were designed using the following criteria:

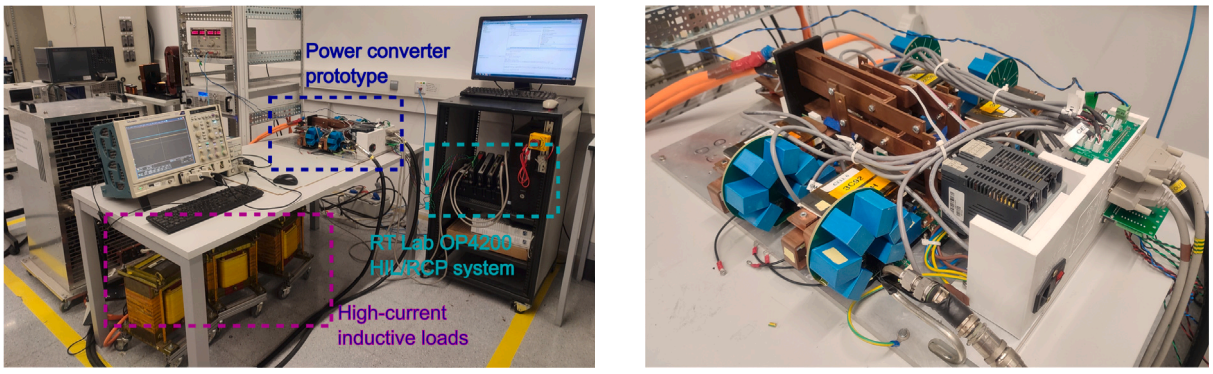
1. Off-the-Shelf Ferrite cores should be used to avoid high costs.
2. Planar cores were preferred to reduce the height of the cells.
3. The size of the cells should allow mounting up to six 167 A Series Capacitor Buck cells for each of CERN's custom cold-plate
4. A single turn inductor design was preferred to minimize conduction power losses, which are the main power loss source in this application.

The inductors were designed around an array of planar E and I cores [Fig. 15(a), items number 1 and 5] from an E64/10/50 form factor. All these criteria led to the selection of two pairs of Ferroxcube E64/10/50 and PLT64/10/50 3C92 for each inductor. The outputs of the two inductors of a single Series Capacitor Buck cell were connected to a common copper plate. An inductance value of 3.5 μH was achieved, offering a good trade-off between current ripple and size. Figs. 15(a) and 15(b) depict a 3D overview of this element.

To achieve the aforementioned 3.5 μH value with a single winding turn for each inductor, an air gap of 0.2 mm [Fig. 15(b)] was used. The windings of these inductors were laser-cut to fit the window area and minimize DC resistance [Fig. 15(a), items 2, 4 and 7]. The AC resistance can be highly reduced if the single layer copper winding is replaced by thinner isolated copper layers, with thickness equal to the skin depth corresponding to the frequency generating the highest amount of AC losses. Ports were added to this element to connect the individual windings for each inductor [Fig. 15(a), item 3] and the output capacitor bank [Fig. 15(a), items 1 and 6].

Regarding the output side capacitor bank, it was made of multiple 1210 MLCC capacitors to keep ESR and ESL values low, resulting in a total capacitance of 4.7 mF per power cell. The designed output capacitor PCB has some space left blank to place damping resistors R_d and C_d [Fig. 2(b)] in case they are required for hardware damping of the power supply.

Finally, the per-cell current sensing feature required by the current balancing algorithm during Buck operation is provided by a LEM HO 250-S/SP30 current sensor, which is located after the output capacitor bank [Fig. 9(b), item 8].



(a) General view of the test-bench.

(b) Physical layout of the manufactured four-cell DC/DC power converter prototype.

Fig. 16. Overview of the experimental set-up used to test and validate the four-cell power converter prototype.

Table 3
Cell main components characteristics summary.

Power semiconductors			
MOSFET		Diode	
Model	IXYS IXTN660N04T4	Model	IXYS DSS2X121-0045B
Package	SOT-227	Package	SOT-227
V_{DSS}	40 V	V_{RRM}	45 V
I_D	660 A	I_{FAV}	120 A
$R_{DS(on)}$	0.85 mΩ	R_F	2.6 mΩ
		V_F	0.59 V
Gate driver & Sensing components			
MOSFET gate driver		Current sensor	
Model	Infineon 1EDI30I12	Model	LEM HO 250-S/SP30
Package	DSO-8	V_{supply}	5 V
Max. gate voltage	20 V	Range I_{meas}	± 250 A
Gate current	3 A	f_{BW}	100 kHz
Max f_{sw}	1 MHz	$Rise\ time_{90\%}$	3.5 µs
Magnetics			
E core		I core	
Model	Ferroxcube E64/10/50	Model	Ferroxcube PLT64/10/50
Material			3C92
Initial Permeability μ_i			1500 ±20%
Resulted saturation current			+120 A
Resulted inductance value			3 µH
Resulted DCR			500 µΩ

Capacitors					
Input capacitor C_{in}		Series capacitor C_s		Output capacitor C_{out}	
Manufacturer	EPCOS	Manufacturer	EPCOS	Manufacturer	Generic
Model	B32524Q1336K000	Model	B32524Q1686K000	Model	X6S, 1210
Maximum voltage	63V	Maximum voltage	63V	Maximum voltage	16V
Capacitance	33 µF	Capacitance	68 µF	Capacitance	10 µF

Table 4
Main parameters of the experimental platform.

Power system parameters			
Number of cells (N)	4	Switching frequency (f_{sw})	50 kHz
Controller execution frequency (f_c)	50 kS/s	Input voltage (V_{bat})	24 V
DC-link capacitors per-cell (C_{dc})	100 µF	Series capacitor per-cell (C_{sc})	400 µF
Output capacitors per-cell (C_{out})	4.7 mF	Per-cell inductances (L_a, L_b)	3.5 µH
Load inductor parameters		Closed-loop settling times	
Load inductance (L_{load})	50 µH	Voltage $ST_{2\%}$	1 s
Load resistance (R_{load})	1 mΩ	Current $ST^I_{2\%}$	5 ms

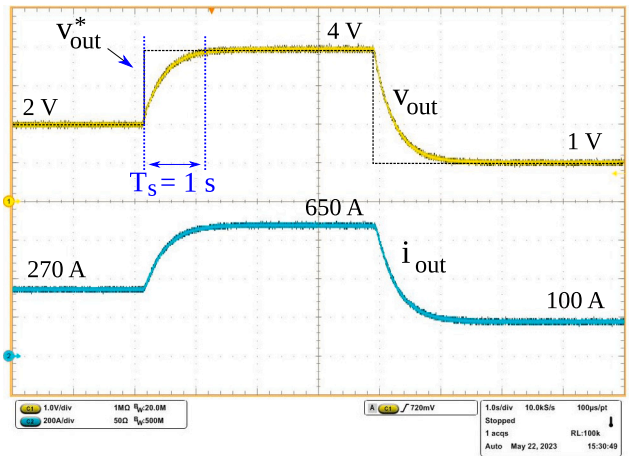
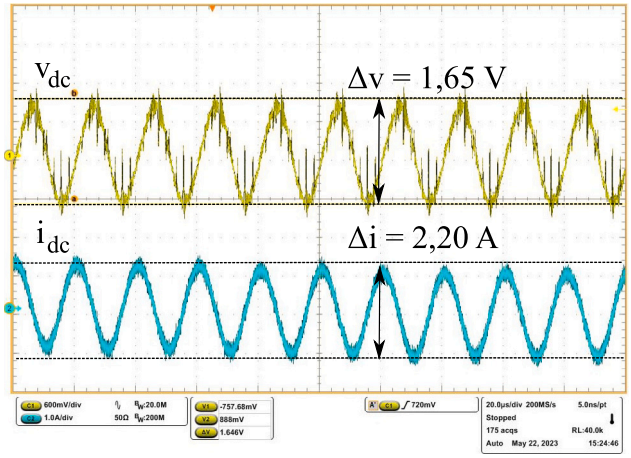
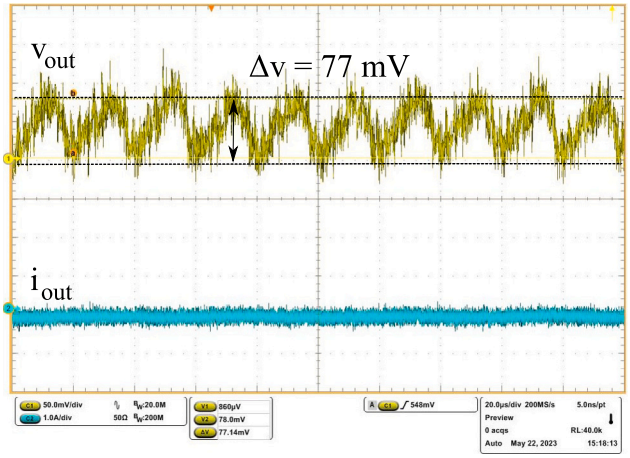


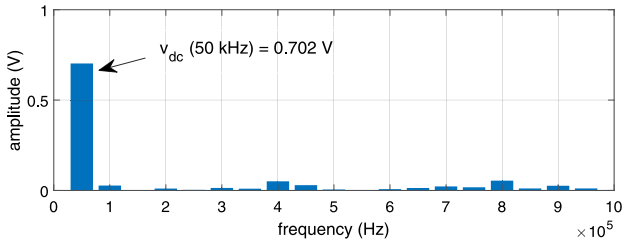
Fig. 17. Converter prototype experimental output voltage and current during transients.



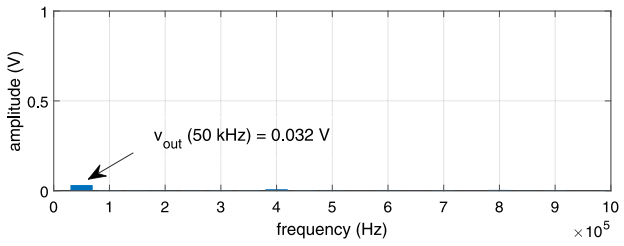
(a) Input side voltage and current AC components.



(b) Output side voltage and current AC components.



(c) Input side voltage harmonic components.



(d) Output side voltage harmonic components.

Fig. 18. Detail of the input and output side voltages and currents at nominal output current operation conditions.

3.6. Summary of main hardware elements

To conclude with the hardware description of the prototype, as a summary, Table 3 collects the main hardware components that make up the Series Capacitor Buck based two-quadrant DC/DC converter cell.

4. Experimental results

4.1. Experimental platform description

The experimental setup shown in Fig. 16(a) was used to analyze and validate the performance of the proposed multiphase DC/DC converter. It included the following elements: the four-cell power converter prototype under test [Fig. 16(b)], three series-connected high current inductor loads, a Keysight N8951 A 80 V/510 A DC power supply, a TTi QL335T low-power supply, an OPAL-RT OP4200 rapid control prototyping platform (incorporating a XilinX Zynq 7030 Kintex 7 FPGA, a dual core ARM9TM processor at 1 GHz and 16 bit ADCs), a custom-made liquid cooling system, and a Tektronix DPO 7054C digital oscilloscope (500 MHz). In addition, a Power Prove DC110 load bank for 24 V battery testing was used to emulate the regenerative operation mode. Table 4 collects the most relevant parameters of the platform.

In the following, the most relevant experimental results in Buck (with conventional modulation and extended modulation) and regenerative modes are provided.

Table 5
Efficiency figures obtained in Buck mode operation for a variety of output voltage and current levels.

Test	$v_{out}(V)$	i_{out} (A)	v_{dc} (V)	i_{dc} (A)	P_{out} (W)	P_{in} (W)	P_{loss} (W)	η (%) - meas.	η (%) - estim.[a]
1	0,497	85	24,04	3,3	42,245	79,332	37,087	53,251	76,471
2	0,997	171	24,92	10,9	170,487	261,818	91,331	65,117	80,837
3	1,497	255	24,00	22,4	381,735	537,600	155,865	71,007	83,360
4	1,997	334	23,96	37,4	666,98	896,104	229,106	74,433	84,752
5	2,497	405	23,92	55,2	1011,285	1320,384	309,099	76,590	85,498
6	2,997	480	23,86	77,0	1438,560	1837,220	398,660	78,301	86,288
7	3,497	570	23,81	103,9	1993,290	2473,859	480,569	80,574	88,158
8	3,997	610	23,76	127,8	2438,170	3036,528	598,358	80,295	86,939
9	4,495	665	23,69	156	2989,175	3695,640	706,465	80,884	87,019

[a] Estimations mathematically calculated considering synchronous diodes.

4.2. Results obtained in Buck operation mode with conventional modulation

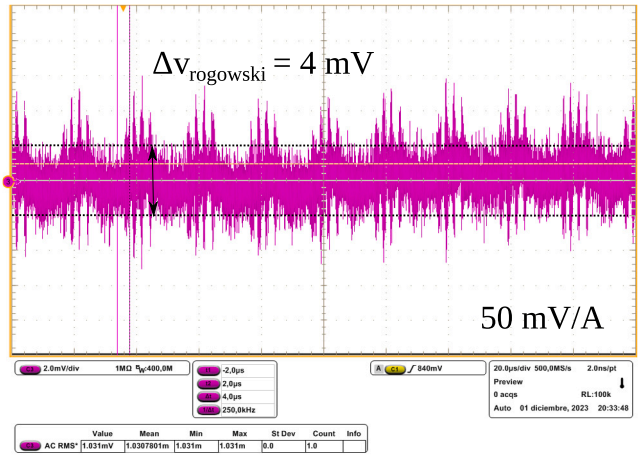
Fig. 17 shows the first test conducted in Buck mode to illustrate the correct control operation and dynamic performance of the converter. A Tektronix voltage probe, reference P5205 A (100 MHz bandwidth), and a current probe, reference TCP404XL (2 MHz bandwidth), were used to capture the oscilloscope measurements. The OP4510 digital device incorporated the decoupled digital control algorithm presented by the authors in [7]. A step-up from 2 V to 4 V was first commanded, followed by a step-down from 4 V to 1 V. The voltage and current balancing closed-loop control dynamics were set to 1 s and 5 ms (Table 4), respectively, with a damping factor ξ equal to one. The desired control dynamics were achieved and no overshoot was produced during transients.

Fig. 18(a) shows, in detail, the input side voltage (v_{dc}) and current (i_{dc}) waveforms, setting the oscilloscope in AC coupling mode, when operating close to nominal output current conditions ($i_{out} \simeq 650$ A). A resonance is generated at the input side of the converter due to the parasitic inductance present between the programmable power supply and the converter's DC-link. As a result, a voltage ripple with an approximate peak-to-peak amplitude of $\Delta v = 1{,}65$ V is generated. Fig. 18(c) shows the harmonic components of such voltage, where the main component of 702 mV peak lies at 50 kHz. This frequency corresponds to the switching frequency (f_{sw}) of the converter (Table 4).

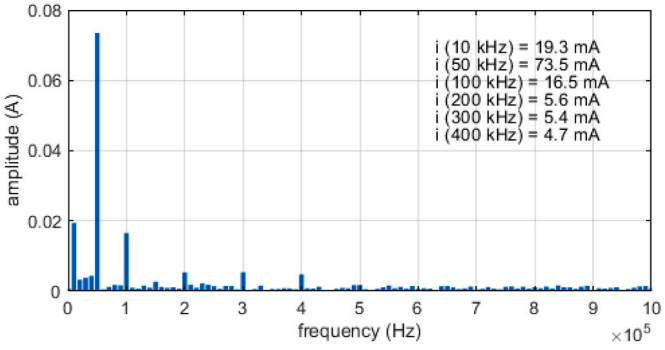
Fig. 18(b) shows the output side voltage (v_{out}) and total current (i_{out}) AC components. The output voltage ripple is reflected at the output side of the converter, but it is minimized thanks to the control feed-forward action, achieving a small output ripple. Again, the most relevant harmonic component lies at 50 kHz, with a peak value of 32 mV [Fig. 18(d)]. In addition to this and thanks to the interleaved operation, the output current ripple lies below the noise level of the current probe. Thus, no i_{out} ripple information could be obtained from these measurements.

To further analyze the AC waveform of i_{out}, this current was measured using a PEM CWT Ultra Mini rogowski coil (30 MHz). AC component of i_{out} was measured at nominal conditions [Fig. 19(a)], showing an amplitude of around 4 $mV_{peak-peak}$, which equals to 80 $mA_{peak-peak}$ since the Rogowski probe scale is 50 mV/A. Fig. 19(b) presents the spectral analysis of such waveform. A component of 73.5 mA lies at 50 kHz, while other harmonic components remain very low. The 50 kHz input voltage and output current harmonic in Figs. 18(c) and 19(b) should not be present in theory. The possible cause is a resonance in the input side of the experimental setup.

Fig. 20(a) shows the per-cell series capacitor currents $i_{sc,j}$ for cells number one and two, measured using rogowski type probes when operating at nominal output current conditions. The total output current of each cell ($i_{out,j}$) can be easily reconstructed from the series capacitor currents [for example, see $i_{out,1}$ depicted with the dotted line of Fig. 20(a)]. Thus, the correct implementation of the interleaved operation is highlighted, showing that both cells are interleaved, with a shift in the switching of each cell of 25% the modulation period T_{sw}. The average values of all cell currents match, demonstrating that the average per-cell currents remain balanced. Alternating the



(a) Output current AC components.



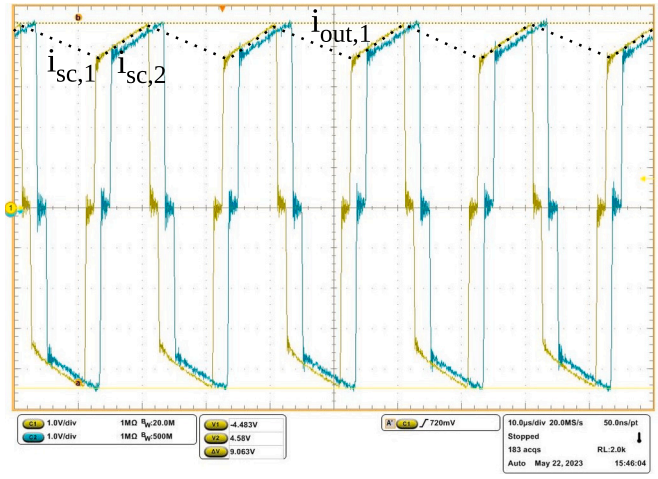
(b) Harmonic components of i_{out}.

Fig. 19. Rogowski coil output current AC component.

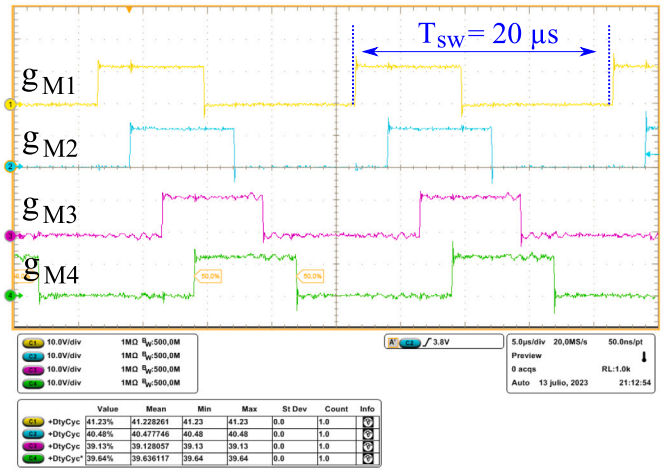
rogowski probes between different cell pairs leads to equivalent results, demonstrating the correct performance of the system and the current balancing algorithm.

The duty-cycle variations between cells, commanded by the controller to balance the per-cell output currents are shown in Fig. 20(b), where the firing signals of the four cell's M_1 MOSFETs are depicted. The highest duty-cycle variation results between cells one and three, and it is minor ($\Delta\delta = 2.10\%$). This last result highlights the correct impedance matching between cells and input and output connection bus-bars thanks to the proposed converter layout.

A short digression regarding power losses and efficiency (η) is required in this specific application. Theoretically, the load is a pure inductor and efficiency would always be zero in the ideal case, rendering the concept of efficiency useless. In reality, a minimum resistance is present in the converter and load connections. The concept of efficiency becomes less meaningful and is not the best indicator of the energy balance in the system. The main concern in this application is the



(a) Currents i_{sc} for cells number one and two, measured with rogowski probes.



(b) M_1 MOSFET's gate signals and duty-cycles.

Fig. 20. Details on current balancing, interleaving and duty-cycles at nominal output current conditions.

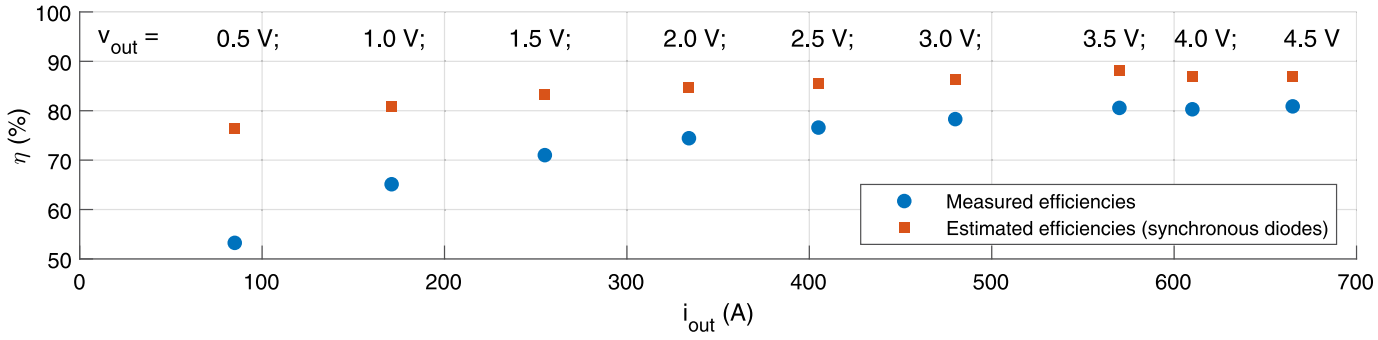


Fig. 21. Power converter prototype efficiencies (measured and estimated considering synchronous diodes, i.e. MOSFETs, instead of diodes) vs output current.

total power loss in the converter, specially at rated current conditions, which should be minimized at all cost, as it is the main source of overall power loss. To measure power losses and estimate efficiency, the four-cell converter was operated in Buck mode for a variety of output voltage and current (or power) levels. Table 5 collects the data obtained through experiments. Fig. 21 shows graphically the obtained measured efficiencies (in blue) vs output current. An overall efficiency of 80,9% was obtained at close-to-nominal conditions (Table 5, test number 9). For the measured efficiencies it must be borne in mind that the power converter operates with a low duty-cycle [see Fig. 20(b), for example], diodes conduct most of the time and their losses are dominant. By incorporating synchronous diodes (MOSFETs) instead of diodes, efficiency will improve. A mathematical power loss estimation considering synchronous diodes was carried out (Table 5, estimated η, and Fig. 21, red colored items), showing that efficiency at nominal conditions would be improved up to around 88%. Although for simplicity and gating signal number, the actual iteration of the power converter prototype does not incorporate synchronous diodes, these results highlight the convenience of their inclusion in the subsequent iteration of the hardware design.

4.3. Results obtained with extended modulation algorithm

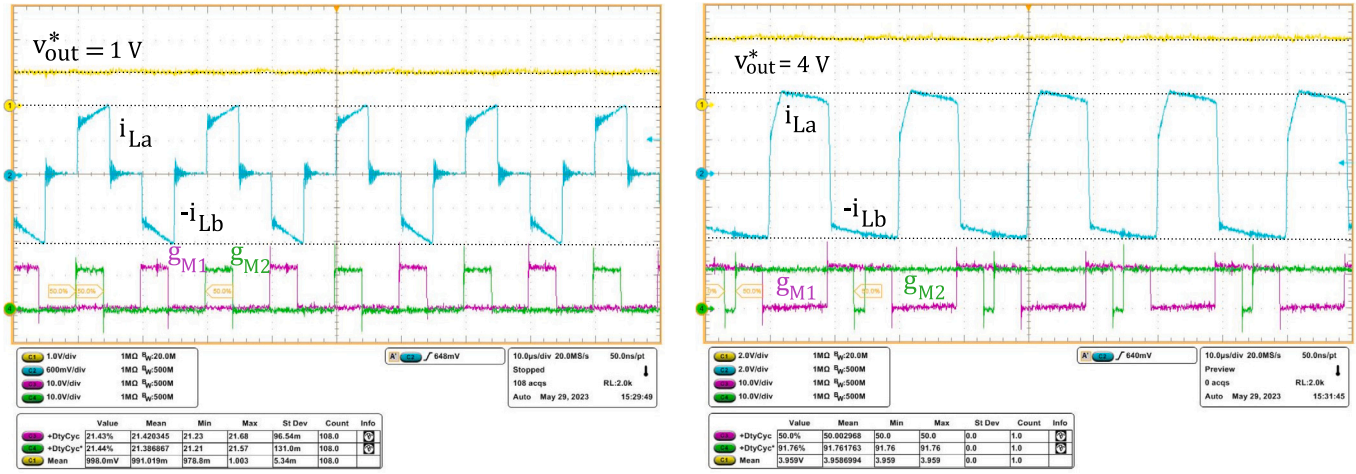
When operating with duty-cycle values lower than 50%, i_{La} and i_{Lb} currents circulating through the two inductors that make up each Series Capacitor cell remain naturally balanced when using the conventional PWM algorithm described in Section 2.1.1 [Fig. 22(a)]. However, if the conventional modulation pattern is applied for $\delta > 0{,}5$, i_{La} and i_{Lb} become unbalanced. Consequently, the modulation approach described in Section 2.1.2 is applied.

To test this extended PWM pattern over the proposed hardware design, input voltage was reduced to 12 V, forcing a duty-cycle greater than 0,5 V when applying a high enough voltage reference v^*_{out}. Under these conditions, average values of currents i_{La} and i_{Lb} where maintained balanced, with some differences between peak values, as shown from the series capacitor current of Fig. 22(b). Under such modulation constraints, inductor current waveforms vary, but the applied output voltage remains with a low harmonic ripple.

4.4. Results obtained in regenerative mode

Finally, the performance of the developed prototype was tested for regenerative operation, i.e., when power flows from the load to the power supply (Section 2.1.3). To carry out these experiments, the set-up depicted in Fig. 23 was implemented. The output terminals of the Keysight N8951 A power supply were connected to the output capacitor C_{out} with inverse polarity, simulating the power delivery capacity of the CERN magnets when energy is recovered from them to the batteries, and the power converter input side was connected to the Power Prove DC110 resistor bank. Tests were carried out in open-loop.

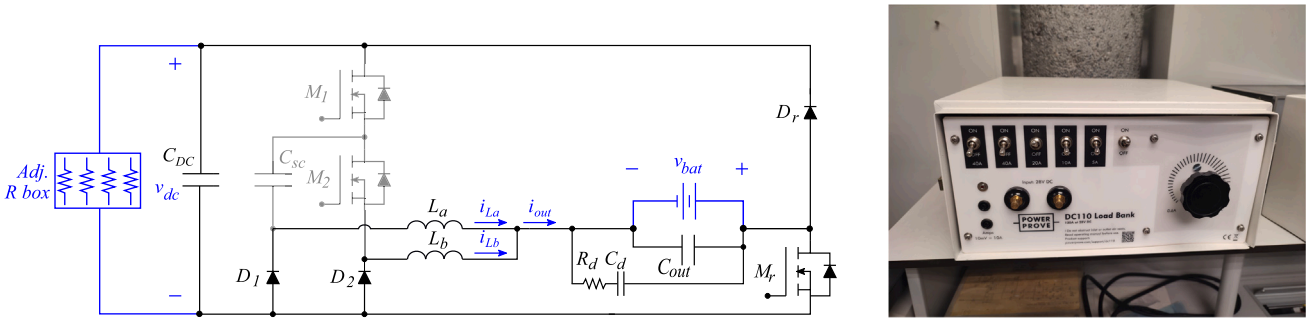
The aforementioned set-up was developed due to the following two limitations in the available resources: (a) The Keysight N8951 A power



(a) Power converter operation for δ < 0,5.

(b) Power converter operation for δ > 0,5.

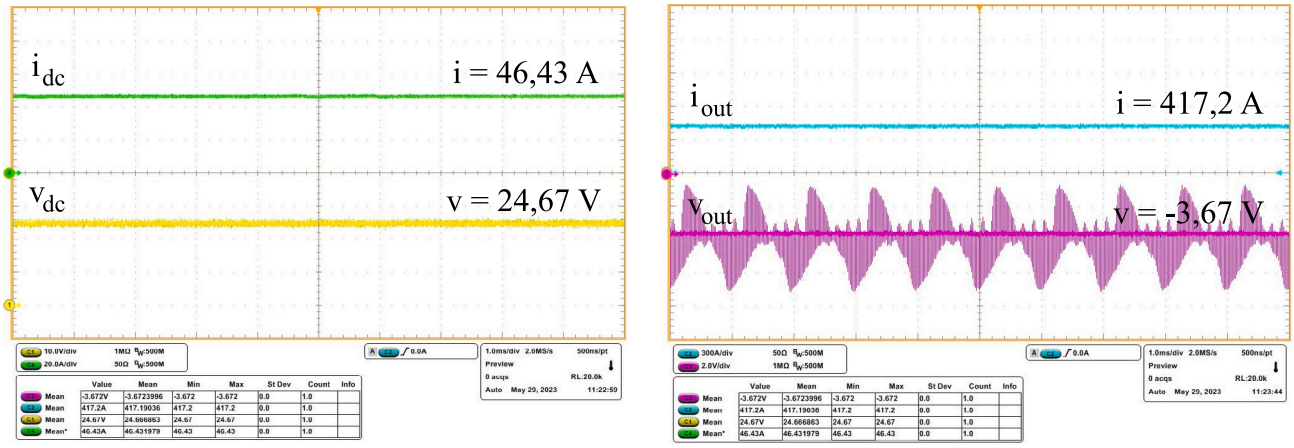
Fig. 22. Conventional vs extended Series Capacitor Buck modulation.



(a) Electrical scheme of the test-bench.

(b) Power Prove DC110 load resistor bank.

Fig. 23. Experimental set-up prepared at the laboratory to emulate the regenerative operation mode.



(a) Input side voltage and current during regenerative operation mode.

(b) Output side voltage and current during regenerative operation mode.

Fig. 24. Operation results for regenerative mode .

supply only provides single quadrant operation (positive voltage and current), and (b) there was no load available with sufficient energy storage capabilities to provide positive output current while working in regenerative mode and in steady-state for enough time to conduct the tests.

Regenerative mode represents a small time-interval of the total power supply operation (approximately 10 h in flat-top operation vs 15 to 20 min discharging), were hadrons do not circulate through the accelerator. Thus, no special current nor voltage waveform requirements are present, and only safe regenerative operation capabilities without putting on risk the power system need to be demonstrated.

To illustrate the performance of the proposed prototype in regenerative mode, Fig. 24(a) shows the v_{dc} and i_{dc} waveforms, while Fig. 24(b) shows v_{out} and i_{out}. Both oscilloscope captures were obtained for an

operating point with i_{out} = 417,2 A and v_{out} = −3,67 V. During the regenerative mode, all the M_r MOSFETs were commanded with the same duty-cycle. Consequently, the current balancing algorithm was not operative, and the per-cell current balancing relied on the impedance matching between cells. Low current unbalances in the range of 12,5% from the average per-cell current value were observed, confirming the safe operation of the proposed hardware solution during energy regeneration. What is more, an efficiency of 75,4% was measured for such operating point. Thus, it can be concluded that the proposed power converter works safely and with a good efficiency during the energy regeneration phase.

5. Conclusions

The HL upgrade of the LHC requires an innovative design of the powering electronics of the superconducting IT electromagnets. It is a highly demanding application, where the output DC/DC conversion stage works with a high step-down ratio and high rated currents.

This paper investigated an alternative to the conventional Interleaved Buck Converter using the Series Capacitor Buck, which provides the following advantages: reduction of output voltage ripple, natural balance of interleaved currents within each cell and high efficiency when operating at the rated current. As demonstrated in the paper, when the Series Capacitor Buck is used in combination with additional MOSFETs and diodes, two quadrant operation is feasible and power recovery of the energy stored in the magnets can be achieved.

The main drawback of the converter is the concentration of conduction power losses in one of the diodes, and the addition of a bulky capacitor. However, simulation and experimental results presented in the paper show that the benefits may outweight the drawbacks of the Series Capacitor Buck based approach. Results also show that the incorporation of synchronous MOSFETs instead of diodes increases considerably the efficiency of the system.

CRediT authorship contribution statement

Alberto Otero-Olavarrieta: Writing – original draft, Validation, Methodology, Investigation, Data curation, Conceptualization. **Asier Matallana:** Writing – original draft, Methodology, Investigation, Conceptualization. **Iñigo Martínez de Alegría:** Writing – review & editing, Writing – original draft, Supervision, Project administration, Methodology, Investigation, Funding acquisition, Conceptualization. **Edorta Ibarra:** Writing – review & editing, Writing – original draft, Validation, Software, Investigation, Formal analysis, Data curation. **Antoni Arias:** Writing – review & editing, Software. **Louis de Mallac:** Writing – review & editing, Supervision, Project administration. **Serge Pittet:** Supervision, Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

Acknowledgments

This work was supported in part by CERN and APERT (UPV/EHU) within the HL-LHC project named “Collaboration in the Study of Power Converter Topologies for Inner Triplet magnets with Energy Recovery in the framework of the High Luminosity upgrade for the LHC at CERN”, and also in part by the Government of the Basque Country within the fund for research groups of the Basque University system under Grant IT978-16. Open Access funding provided by University of the Basque Country.

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