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DOCTORAL THESIS

Contributions to the design of power modules for electric and hybrid vehicles: trends, design aspects and simulation techniques

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A los de casa,
Amatxu, Aita y Amama.
- Montse, Ovidio y Primi -

Gracias Amatxu y Aita
por estar siempre ahí,
Amama seguro que
lo estás viendo.

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En Bilbao, Diciembre de 2019.

Abstract

A large number of factors such as the increasingly stringent pollutant emission policies, fossil fuel scarcity and their price volatility have increased the interest towards the partial or total electrification of current vehicular technologies. This transition of the vehicle fleet into electric is being carried out progressively. In the last decades, several technological milestones have been achieved, which range from the development of basic components to the current integrated electric drives made of silicon (Si) based power modules. In this context, the automotive industry and political and social agents are forcing the current technology of electric drives to its limits. The technological targets proposed by Horizon 2020, USCAR, DOE and UN ESCAP regarding the power electronics are stringent, and can be summarized in the following items:

1. An increase of the power density of the power conversion stage of around 50 % (from 8.7 kW/l up to 13.4 kW/l).

2. A reduction of power converter losses (conduction and switching losses) by 50 %.

3. Significant costs reductions (a reduction by four) for on-board power electronics (from 30 $/kW to 8 $/kW).

4. Simplification of thermal management systems by using on-board coolants minimizing, as possible, the usage of additional components.

5. Whole drive size and weight reductions of 35 % and 40 %, respectively (from 1.1 kW/kg and 2.6 kW/l up to 1.4 kW/kg and 4.0 kW/l).

Specifically, the U.S. DOE's goals for 2020 propose the development of power converter technologies with specific power of more than 14.1 kW/kg and efficiencies greater than 98 %. At the same time, the aforementioned goals aim for a significant cost reduction up to 3.3 $/kW.

Thus, these goals encourage the development of the main parts of the traction system: battery, power converter and engine. The research line of this work is focused on the analysis and design of the power modules in order to improve their capabilities which are necessary to meet the aforementioned goals.

This thesis presents an in-deep review of the state of the art concerning its internal power semiconductors and many internal design aspects of power modules. According to semiconductor technology, *Wide bandgap* (WBG) semiconductors, and specially, silicon carbide (*SiC*) based power electronic devices, are identified as the most promising alternative to *Si* devices due to their superior material properties. In fact, the current silicon and WBG technologies are reviewed in this document and, after a market analysis, the most suitable power semiconductor devices are highlighted in order to be assembled inside a power module.

In addition to power semiconductor technology, the main concepts of electrical connections between devices, where the parallelization is required, are extracted in order to develop and propose some specific power module design criteria which ease this task. The main power module design concepts are identified through scientific, industrial and commercial literature taking into account the power module electrical requirements. These criteria allow routing correctly control and power signals with an optimum WBG-based die parallelization.

These proposed design concepts are put into practice and verified through three initial power circuits based on PCB substrate technology, where electrical co-simulations have been realised in order to extract circuit behaviour. These circuits are different parts of a power converter (power switch, half-bridge and DC-link) where a progressively parallelization and symmetry have been implemented at different levels. According to the electrical simulation results obtained, the alternatives with the highest integration of both concepts, the best voltage and current balances show.

Finally, two power module proposals have been presented, called *symmetric* and *cell* designs. Both circuits are half-bridge topologies where the proposed design criteria have been implemented. In the *symmetric* design a much stricter symmetry concept has been applied than in the *cell* design where the connections are practically identical, thus affecting the current balance that flows through each power semiconductor. In the case of *cell* design, the main benefits are due to the semiconductor placement in a P- and N- cell configuration (MOSFETs and diodes are connected as close as possible in the switching loop) with snubber capacitors, reducing the length of electrical connections and balancing the circuit. The electrical co-simulations through ADS^{TM} software verified the effectiveness of the layouts according to the design criteria application. Apart from the electrical behaviour, the electro-thermal response of each power module has been

extracted in order to detect reliability issues. Thanks to a specific methodology developed in this thesis, which combines 1D and 3D simulation techniques, the power modules are evaluated thermally according to real operation conditions provided by driving cycle profiles. After the analysis of thermal data in each proposal, no critical points have been detected, avoiding reliability issues.

The electrical and thermal simulations verified the improvements of the proposed design criteria for the development of HEV/EV power modules. The results of this methodology improve the prototyping step since it starts with more information about design electrical and thermal behaviour.

Resumen

En la última década, la protección del medio ambiente y el uso alternativo de energías renovables están tomando mayor relevancia tanto en el ámbito social y político, como científico. Problemas derivados de los gases de efecto invernadero, el alto grado de polución en las ciudades, la escasez de combustibles fósiles y la volatilidad de sus precios son cuestiones que están acelerando el desarrollo de sistemas de energía renovables más eficientes y sostenibles.

En este contexto, el sector del transporte es uno de los principales causantes de los gases de efecto invernadero y la polución existente, contribuyendo con hasta el 27 % de las emisiones a nivel global. Dentro del sector de transporte (aéreo, ferroviario y carretera), el transporte por carretera supone el 75 % de las emisiones, siendo este tipo de medio el principal causante del incremento de los niveles de contaminación. De acuerdo a las perspectivas de aumento de población, el parque de vehículos por carretera puede alcanzar los 200 millones de unidades en el año 2050. Por consiguiente, si se continua con la misma tendencia, se estima un alza de los niveles de polución entorno al 30 % para dicho año. En este contexto desfavorable, la electrificación de los vehículos de carretera se convierte en un factor crucial para solventar y paliar los problemas sociales y medioambientales. Para ello, la transición de la actual flota de vehículos de carretera debe ser progresiva (estimación de 100 millones de unidades para el año 2050, según el *IEA Energy Technology Perspective BLUE Map*), forzando la investigación y desarrollo de nuevos conceptos a la hora de producir vehículos eléctricos (EV) y vehículos eléctricos híbridos (HEV) más eficientes, fiables, seguros y de menor coste.

Sin embargo, los retos y desafíos futuros son cada vez mayores. En este sentido, diversos organismos como Horizon 2020, USCAR, DOE y UN ESCAP han fijado las siguientes metas:

1. Incremento de la densidad de potencia de la etapa de conversión entorno al 50 % (de 8,7 kW/l a 13,4 kW/l).

2. Reducción de las pérdidas de potencia del convertidor del 50 %.
3. Reducción significativa (x4) de los costes de fabricación de la electrónica de potencia (de 30 $/kW a 8 $/kW).
4. Simplificación de los sistemas de refrigeración, minimizando el número de componentes.
5. Reducción de la dimensiones (35 %) y peso (40 %) totales (de 1,1 kW/kg a 1,4 kW/kg y 2,6 kW/kg a 4 kW/kg, respectivamente).

A modo de ejemplo, el Departamento de Energía de EEUU tiene como objetivo lograr para 2020 desarrollar convertidores de potencia cuyas densidades de potencia sean superiores a 14,1 kW/kg y eficiencias superiores al 98 %. Estableciendo el precio objetivo de dichos convertidores por debajo de los 3,3 $/kW.

Teniendo en cuenta estos objetivos y desafíos, en las últimas décadas se han ido alcanzando gran cantidad de hitos tecnológicos, donde han predominado los desarrollos basados en semiconductores de potencia de silicio (*Si*). Los esfuerzos y desarrollos tanto de la industria de automoción, así como los requisitos y necesidades impuestss por diversos agentes políticos y sociales, están llevando el desarrollo de dicha tecnología hasta sus límites, lo que implica que las tecnologías actuales no pueden alcanzar estos nuevos desafíos.

En consecuencia, deben llevarse a cabo nuevas líneas de investigación, entre las cuales destacan el desarrollo y mejora de cada una de las partes fundamentales que constituyen el convertidor de potencia de los HEV/EV, tales como: sistemas avanzados de gestión térmica, nuevos diseños y componentes del *DC-link*, nuevas tecnologías de semiconductores de potencia, encapsulados optimizados, y topologías alternativas de conversión de potencia. En este contexto, el trabajo de investigación que se ha desarrollado en la presente tesis abarca los siguientes aspectos tecnológicos:

- **Arquitecturas de la etapa de conversión de potencia.** Las principales topologías que pueden ser implementadas en el tren de potencia para HEV/EV son descritas y analizadas, teniendo en cuenta las alternativas que mejor se adaptan a los requisitos técnicos que demandan este tipo de aplicaciones. De dicha exposición se identifican los elementos constituyentes fundamentales de los convertidores de potencia que forman parte del tren de tracción para automoción, siendo tomados estos elementos como el punto de partida para los distintos desarrollos y mejoras presentados a lo largo de la tesis.
- **Nuevos dispositivos semiconductores de potencia.** Los objetivos y retos tecnológicos anteriormente mencionados solo pueden lograrse median-

te el uso de nuevos materiales. Los semiconductores *Wide bandgap* (WBG), especialmente los dispositivos electrónicos de potencia basados en nitruro de galio (*GaN*) y carburo de silicio (*SiC*), son las alternativas más prometedoras al silicio (*Si*) debido a las mejores prestaciones que poseen dichos materiales, lo que permite mejorar la conductividad térmica, aumentar las frecuencias de conmutación y reducir las pérdidas. En este contexto, el conocimiento extraído de las alternativas comerciales proporciona una visión completa de las posibilidades de cada tecnología de semiconductores, así como su idoneidad para ser aplicadas.

- **Análisis de técnicas de rutado, conexionado y ensamblado de módulos de potencia.** Los módulos de potencia fabricados con *dies* en lugar de dispositivos discretos son la opción preferida por los fabricantes para lograr las especificaciones indicadas por la industria de la automoción. Teniendo en cuenta los estrictos requisitos de eficiencia, fiabilidad y coste es necesario revisar y plantear nuevos *layouts* de las etapas de conversión de potencia, así como esquemas y técnicas de paralelización de los circuitos, centrándose en las tecnologías disponibles.

Teniendo en cuenta dichos aspectos, la primera parte de la investigación que se ha desarrollado evalúa las alternativas de tecnología de semiconductores de potencia que pueden ser implementadas en aplicaciones HEV/EV de acuerdo a sus requisitos. Este estudio del mercado de los semiconductores de potencia indica la existencia de dos tendencias, las tecnologías de silicio (*Si*) y los materiales WBG:

- El silicio (*Si*) representa la alternativa de mayor madurez y resultados contrastados, siendo el IGBT el semiconductor dominador del mercado de la electrónica de media potencia, nicho en el que se engloban las aplicaciones del tren de propulsión del sector de la automoción. Por dicha razón, se ha analizado en detalle las características, propiedades y la evolución de este dispositivo con el objetivo de obtener una visión de sus ventajas y desventajas. En este sentido, esta tecnología presenta dos principales desventajas, como son las relativas bajas frecuencias de conmutación, insuficientes para cumplir con los objetivos de pérdidas, y la baja conductividad térmica, donde se demandan materiales que puedan proporcionar mayores densidades de potencia ocupando menos espacio y peso.

- Los materiales WBG, entre los cuales destacan el carburo de silicio (*SiC*) y nitruro de galio (*GaN*) son los materiales con mayores posibilidades de ser empleados en el futuro en el sector de la automoción. A partir del estudio realizado se puede decir que, los dispositivos *GaN* presentan buenos comportamientos para altas frecuencias de conmutación, pero la estructura

lateral de los transistores, la conductividad térmica similar al *Si*, los bajos rangos de tensión/corriente, así como la falta de cierto grado de madurez y fiabilidad, hacen que su inmediata incorporación en el desarrollo de módulos de potencia no sea inmediata. A diferencia del *GaN*, los semiconductores basados en *SiC* muestran una perspectiva diferente, donde existe un nivel de desarrollo mucho más importante y una amplia variedad de dispositivos con múltiples rangos de operación. Estos factores hacen de esta tecnología, no solo por su estado actual de desarrollo, sino también por sus futuras perspectivas, una de las mejores opciones para cumplir los requisitos y retos que se ha citado anteriormente.

Una vez analizadas las alternativas de semiconductores de potencia, este trabajo estudia las conexiones internas del módulo de potencia para obtener los rangos de tensión y corriente necesarios para los vehículos eléctricos. En particular, para obtención de las densidades de potencia requeridas se ha empleado la técnica de paralelización de semiconductores de potencia. Previamente, para la correcta aplicación de dicha técnica de diseño ha sido necesario conocer las partes de los circuitos de conmutación implicadas, así como los principales elementos, destacando los siguientes:

- El comportamiento estático y dinámico de los semiconductores de potencia a paralelizar.
- El conexionado de la señales de control con los semiconductores de potencia.
- El circuito de potencia a través del cual fluyen las señales de alta corriente.

Tras identificar las ventajas y desventajas para llevar a cabo la paralelización de los semiconductores de potencia, queda patente la falta de referencias técnicas donde se indique de forma concreta y exhaustiva como realizar el diseño entre varios semiconductores de potencia evitando los posibles desequilibrios que se produzcan entre los dispositivos.

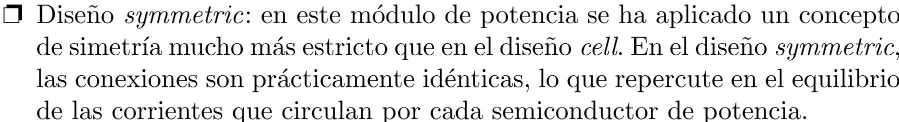
Debido a esta falta de información tanto científica como comercial e industrial, una de las principales contribuciones del presente trabajo ha sido la propuesta de una serie de criterios de diseño para el diseño de módulos de potencia, tomando como punto departida los módulos de potencia para aplicaciones HEV/EV. Dichos criterios parten de la recopilación de artículos científicos, así como de soluciones industriales/comerciales, donde se recogen soluciones locales para determinadas problemáticas, junto a otros documentos técnicos como *datasheets* y notas de aplicación. Toda esta información ha sido procesada para desarrollar y proponer los mencionados criterios de diseño, organizados y clasificados de acuerdo a un desglose del módulo de potencia en 5 partes fundamentales: mecánica, sustrato, ataque de compuerta, *layout* de potencia y terminales.

En cada una de las mencionadas partes del módulo de potencia, han sido detalladas las estrategias para aplicar la simetría, así como otra serie de consejos para realizar un buen conexionado. Concretamente, en las partes de ataque de compuerta y *layout* de potencia se han presentado diversas soluciones para equilibrar las conexiones eléctricas entre los semiconductores de potencia para reducir las impedancias parásitas del circuito y diversos efectos adversos como acoplamientos entre las señales de control y potencia. Una vez desarrollados y extraídos los criterios de diseño para módulos de potencia, éstos han sido puestos en práctica para, así, validar las hipótesis propuestas. Para dicha validación se han utilizado diversas técnicas de simulación y co-simulación, tanto eléctrica como térmica, usando el *software* ADS^{TM} y COMSOL Multiphysics, respectivamente.

Hay que tener en cuenta que un módulo de potencia es un diseño avanzado formado por múltiples partes, compactas entre sí, donde el espacio de diseño del *layout* es reducido, lo que dificulta el diseño de este tipo de soluciones. Por lo tanto, antes de cometer un desarrollo de tal índole, se ha recopilado información y experiencia a través del diseño de tres circuitos de potencia más simples. Estos circuitos son diversas partes de un convertidor de potencia, permitiendo comprender como aplicar la paralelización y la simetría en diferentes niveles de diseño. Dichos circuitos son un *switch* de potencia, un *half-bridge* y un *DC-link* implementados y diseñados sobre un sustrato PCB multicapa. El empleo de dicho sustrato ha facilitado el rutado de las pistas y áreas de cobre, ya que proporciona mayor flexibilidad al diseñador. Los resultados de simulación eléctrica que se han obtenido para cada uno de los circuitos muestran que las alternativas donde mejor han sido aplicadas las técnicas de paralelización y simetría garantizan el equilibrio de las corrientes en el circuito.

Comparado con otras soluciones como DBC/DBA y AMB, el uso de sustratos PCB aumenta claramente los valores de impedancia parásita. Esta es una de las razones por las que los circuitos de potencia para HEV/EV suelen implementarse sobre un formato de módulo de potencia. Por esta razón, esta tesis propone dos alternativas de módulo de potencia, utilizando la experiencia adquirida previamente en los circuitos diseñados sobre PCB. La topología de cada módulo es un *half-bridge*, donde se ha procurado reducir las longitudes de las conexiones eléctricas y equilibrar las conexiones entre los dispositivos en paralelo. Además, el sustrato empleado es una solución híbrida, una combinación de DBC y PCB, que permite aprovechar las ventajas de cada tecnología de sustrato. Así, por ejemplo, el rutado del ataque de compuerta se ha realizado de forma aislada respecto el *layout* de potencia, evitando los posibles efectos de retroalimentación.

Las dos propuestas de módulo de potencia *half-bridge* desarrolladas en esta tesis han sido las siguientes:



- Diseño *symmetric*: en este módulo de potencia se ha aplicado un concepto de simetría mucho más estricto que en el diseño *cell*. En el diseño *symmetric*, las conexiones son prácticamente idénticas, lo que repercute en el equilibrio de las corrientes que circulan por cada semiconductor de potencia.

- Diseño *cell*: en este módulo de potencia los principales beneficios se han debido a la implementación de las celda P y N (colocando lo mas próximo posibles el MOSFET y el diodo que forman el lazo de conmutación) con condensadores (*snubbers*) entre los MOSFETs y diodos, permitiendo reducir los caminos de conmutación y equilibrar los diversos lazos cerrados del circuito.

De acuerdo a los resultados obtenidos en las simulaciones eléctricas, ambas soluciones no muestran retardos críticos en las señales de control que puedan producir desequilibrios de corriente, poniendo en peligro la integridad del sistema. Además, la aplicación de las técnicas de paralelización y simetría permiten diseñar conexionados entre los semiconductores de potencia con impedancias parásitas similares, igualando las corrientes que circulan por cada dispositivo.

Además del estudio eléctrico se ha realizado también un estudio térmico para cada una de las soluciones de módulo de potencia propuestas, concretamente se han realizado simulaciones electro-térmicas de los *layout* de potencia de cada uno de las soluciones. En dichas simulaciones se ha propuesto una metodología que combina simulaciones 1D y 3D para poder aplicar perfiles de conducción de vehículo eléctrico y así someter los diseños a situaciones reales. Los resultados obtenidos para ambos módulos de potencia propuestos no han mostrado puntos críticos que indiquen un comportamiento de los circuitos por encima de las temperaturas de operación de los semiconductores que producirían la ruptura de los mismos.

Finalmente, los resultados que se han extraído de los circuitos propuestos demuestran la utilidad de los criterios de diseño propuestos, obteniendo circuitos de potencia con bajas impedancias parásitas, equilibrados eléctrica y térmicamente. A nivel industrial, el conocimiento expuesto en la presente tesis permite reducir los tiempos de diseño a la hora de obtener prototipos de ciertas garantías, ya que los criterios de diseño expuestos permiten comenzar la fase de prototipado habiéndose realizado muchas comprobaciones eléctricas y térmicas.

Laburpena

Faktore asko dira gaur egungo ibilgailuen teknologien elektrifikazio partziala edo osoa lortzeko interesa areagotu dutenak, hala nola gero eta zorrotzagoak diren gas kutsatzaileen emisio-politikak, erregai fosilen urritasuna eta hauen prezioen hegazkortasuna. Halaere, barne errekuntzako motoreetan oinarritutako ibilgailuetatik abiatuta motore elektrikotan oinarritutakoetarako trantsizioa era mailakatuan ematen ari da. Hainbat mugarri teknologiko lortu dira azkenengo harmakadetan, oinarrizko osagaien garapenetik hasi eta silizioan (Si) egindako potentzia moduluekin eginiko eragingailu elektriko integratuetaraino. Testuinguru honetan, ibilgailuen industriak zein eragile politikoek eta sozialek gaur egungo eragingailu elektrikoen teknologia bere muturretara bultzatzen ari dira. Hala nola DOE, Horizon 2020, USCAR eta UN ESCAP bezalako erakundeek potentzia eletronikoari dagozkion hurrengo helburu teknologikoak ezarri dituzte:

1. Bihurgailuaren potentzia-dentsitatearen % 50-eko igoera (8,7 kW/l-tik 13,4 kW/l-ra).
2. Bihurgailuaren eroate eta kommutazio-galeren % 50-eko murrizketa.
3. Potentzia-elektronikaren fabrikazio kostua murriztea (30 $/kW-tik 8 $/kW-ra).
4. Hozte-prozesuaren sinplifikazioa eta osagaien murrizketa.
5. Masa (% 35) eta bolumen (% 40) totalaren murrizketa, 1,1 kW/kg-tik 1,4 kW/kg-ra eta 2,6 kW/l-tik 4 kW/l-ra.

Esate baterako, AEBko energia-sailak % 14.1 kW/kg-ko potentzia-dentsitatea eta % 98-ko eraginkortasuna duten potentzia-bihurgailuen garapena espero du 2020 urterako, hau dena 3,3 $/kW-tako preziotik behera.

Helburu hauek trakzio-sistemaren atal nagusien garapena sustatzen dute. Bateria, potentzia-bihurgailua eta motorea. Lan honen ikerketa-ildoa aipatutako

helburuak burutzeko beharrezkoak diren potentzia-moduluen azterketara eta garapenera bideratzen da.

Ildo honetan, lan honek potentziako-erdieroaleen artearen egoera sakon bat eta moduluen barne diseinuko aspektu asko aurkezten ditu. Beraien goi-mailako ezaugarriak direla eta, banda zabaleko erdieroaleak (*Wide bandgap, WBG*), silizio karburoan (*SiC*) oinarritutakoak batez ere, siliziozko erdieroaleen etorkizuneko aukera bezala aurkezten dira. Honekin batera, gaur egungo silizio eta WBG teknologiaren merkatu azterketa bat egin eta potentzia-modulu baten barruan muntatzeko gailu egokienak azpimarratzen dira.

Potentziako-erdieroaleen teknologiaz gain, paralelizatutako gailuen konexio elektrikorako kontzeptu garrantzitsuenak aztertu dira. Kontzeptu hauek potetnzia-moduluen diseinurako irizpideak proposatzeko eta garatzeko erabiliko dira, eginkizun hau erraztuz. Potentzia-moduluen eskakisun elektrikoak kontuan hartuta, potentzia-moduluen diseinurako irizpideen kontzeptu garrantzitsuenak identifikatu dira literatura zientifikoa, industriala eta komertziala aztertuz horretarako. Irizpide hauek, WBG *die*-ak era optimoan paralelizatzeko kontrol eta potentzia seinaleak modu egokian bideratzea ahalbidetzen dute.

Aurkeztutako diseinu-irizpide hauek PCB sustratoan oinarritutako hiru zirkuituetan baieztatu dira, hauen jokaera ikertzeko simulazio elektrikoak erabiliz (zirkuituen eredu elektromagnetikoa + potentzia-erdieroaleen Spice-eko eredua). Zirkuitu hauetan paralelizazio eta simetria-kontzeptuak modu mailakatu batean erabili dira, hauek potentzia bihurgailu baten hiru atal ezberdin irudikatuz: potentzia-etengailua, *half-bridge*-a eta *DC-link*-a. Emaitzak, bi kontzeptu hauen mailakatze eta korronte-tentsio oreken arabera sailkatu eta aurkeztu dira.

Azkenik, bi potentzia-modulu proposamen aurkeztu dira: *symmetric* eta *cell* diseinuak. Biak *half-bridge* topologiak dira (potentzia-bihurgailuen oinarrizko osagaia kontsideratuta), eta bietan erabili dira tesian garatutako diseinu irizpide nagusiak. *Symmetric* diseinuan simetria-kontzeptu zorrotzago bat erabiliz erdieroale bakoitzean korronte oraken eragin da. *Cell* diseinuko abantaila nagusiak erdieroaleen kokapenagatik ematen dira, *snubber* kondentsadoredun P eta N *cell* konfigurazioak ezarri dira (MOSFET-ak eta diodoak konmutazio bukletik ahal dan gertuenen kokatzen dira) konexioen luzapena txikiagotuz eta zirkuitua orekatuz. ADS^{TM}-ko simulazioak aplikatutako diseinu-irizpideak balioztatzeko erabili dira. Honekin batera, 1D eta 3D simulazio-teknikak, Matlab eta COMSOL Multiphysics konbinatzen duten metodologia espezifiko bat garatu da modelo elektro-termiko konplexu bat lortzeko. Aipatutako guztia potentzia-moduluak egoera errealetako baldintzetan testeatzeko erabili da, puntu kritikoak eta fidagarritasun arazoak ez daudela baieztatuz.

Simulazio hauek, EV/HEV-tarako proposatutako potentzia-moduluen diseinu-irizpideak egiaztatzeko balio izan dute. Metodologia honen bitartez diseinuko arazo asko ekiditu ahal daitezkenez, prototipaziorako pausoa aurreratu, prototipazioa puntu tekniko hobe batetik hasi eta garapenaren denbora osoa murrizten da.

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List of Acronyms

1D	1 Dimension
2DEG	2-D electron gas
3D	3 Dimensions
AC	Alternating current
AMB	Active metal brazing
BJT	Bipolar junction transistor
CHB	Cascade H-bridge
CTE	Coefficient of thermal expansion
CSTBT	Carrier stored gate bipolar transistor
DBA	Direct bonded aluminium
DBC	Direct bonded copper
DC	Direct current
DfR	Design for reliability
DLC	Direct lead bonding
DOE	United States Department of Energy
DSP	Digital signal processor
D-mode	Depletion mode
EM	Electromagnetic method
EMC	Electromagnetic compatibility
EMF	Electromotive force
EMI	Electromagnetic Interference
E-mode	Enhancement mode
EV	Electric vehicle
FC	Flying capacitor
FCell	Fuel cell vehicle
FEM	Finite element method

FS	Field stop
FWD	Freewheeling diode
FZ	Float zone
GHG	Greenhouse gas
GRG	Generalized reduced gradient method
HEMT	High electron mobility transistor
HEV	Hybrid electric vehicle
HPC	High performance computing
HSEM	High speed electric machine
HV	High voltage
HVDC	High voltage direct current
ICE	Internal combustion engine
IEA	International Energy Agency
IGBT	Insulated gate bipolar transistor
JBS	Junction barrier schottky
JFET	Junction field effect transistor
LC_{JFET}	Lateral channel junction field effect transistor
LPT	Light punch through
MIS-HEMT	Metal insulator semiconductor gate field effect transistor
MOSFET	Metal oxide semiconductor field effect transistor
MPS	Merged PN schottky diode
MTBF	Mean time between failures
NEDC	New European driving cycle
NPC	Neutral point clamped
NPT	Non punch through
p-HEMT	p-GaN gate Field effect transistor
OEM	Original equipment manufacturer
PCB	Printed circuit board
PCC	Power converter circuits
PEEC	Partial element equivalent circuit
PHEV	Plug-in hybrid electric vehicle
PEEC	Partial element equivalent circuit
PiN	p-n diode with intrinsic region
PM	Permanent magnet
PT	Punch through
PMSM	Permanent magnet synchronous machine
RB	Reverse blocking

RC	Reverse conducting
R&D	Research and development
RE	Range extended
RT	Real time
SAE	Society of Automotive Engineers
SBD	Schottky barrier diode
SJT	Super junction transistor
SPT	Soft punch through
TIM	Thermal interface material
Trench FS	Trench field stop
UN ESCAP	United Nations Economic and Social Commission for Asia
USCAR	United States Council for Automotive Research
VT_{JFET}	Vertical trench junction field effect transistor
WBG	Wide bandgap
WLTP	Worldwide harmonized light-duty vehicles test procedure

List of Symbols

α	Thermal expansion coefficient (K^{-1})
λ	Thermal conductivity ($W/(m \cdot K)$)
A	Area of a surface (m^2)
BD_{xy}	Body diode top or bottom (x) and number of branch (y) (-)
C_{DC}	DC-link capacitor (F)
C_{th}	Thermal capacitance (W·s/K)
d	Thickness of a layer (m)
D_{xy}	Diode top or bottom (x) and number of branch (y) (-)
D_b	Drain bottom connection (-)
D_t	Drain top connection (-)
$freq$	Frequency (Hz)
G_b	Gate bottom connection (-)
G_t	Gate top connection (-)
I_{max}	Maximum semiconductor current (A)
I_{rr}	Recovery current (A)
L_o	Overall length of the material (m)
L_b	Equivalent parasitic inductance of bonding (H)
L_{bd}	Drain bottom equivalent inductance (H)
L_{bs}	Source bottom equivalent inductance (H)
L_d	Drain equivalent parasitic inductance (H)
L_{dBUS}	Drain DC-link equivalent inductance (H)
L_{DC^+x}	Equivalent parasitic inductance between x device and DC^+ power terminal (H)
L_g	Gate equivalent inductance (H)
L_{gate}	Gate loop total parasitic inductance (H)
L_{pi}	Parasitic inductance (autoinductance) (H)
$L_{p1-phase}$	Phase equivalent inductance of P-cell (H)

L_{loopi}	Total loop inductance value (H)
$L_{n1-phase}$	Phase equivalent inductance of N-cell (H)
L_{tg}	Gate top track equivalent inductance (H)
L_{tsaux}	Source auxiliary top track equivalent inductance (H)
L_{td}	Drain top equivalent inductance (H)
L_{ts}	Source top equivalent inductance (H)
L_{s}	Source auxiliary equivalent inductance (H)
L_{sBUS}	Source DC-link equivalent inductance (H)
L_{sw}	Power loop equivalent inductance (H)
L_{w}	Equivalent parasitic inductance of wire (H)
M_{effect}	Equivalent parasitic inductance due to mutual coupling effect (H)
M_{pij}	Mutual coupling inductance (H)
M_{xj}	MOSFET top or bottom (x) and number of branch (y) (-)
n	Number of devices in parallel (-)
P_{D}	Diode power losses profile (W)
$P_{loss,D}$	Diode power instant losses (W)
$P_{loss,M}$	MOSFET power instant losses (W)
P_{M}	MOSFET power losses profile (W)
S_{b}	Source bottom connection (-)
S_{baux}	Source bottom auxiliary connection (-)
S_{ij}	Scattering parameters (-)
S_{t}	Source top connection (-)
S_{taux}	Source top auxiliary connection (-)
Q_{c}	Charge value of diode (C)
Q_{g}	Gate charge (C)
Q_{rr}	Reverse recovery charge (C)
R_{dson}	Equivalent resistance when the device is on (Ω)
R_{g}	Internal gate resistance (Ω)
Rg_{ext}	External gate resistance (Ω)
R_{th}	Thermal resistance (K/W)
$R_{th_{subs}}$	Substrate equivalent thermal resistance (K/W)
SW_{xy}	Switch top or bottom (x) and number of branch (y) (-)
T	Temperature (K)
$T_{die,D}$	Diode die instant temperature (K)
T_{D}	Diode temperature profile (K)
$T_{die,M}$	MOSFET die instant temperature (K)
$t_{d_{(off)}}$	Turn *off* delay time (s)

$t_{d_{(on)}}$	Turn *on* delay time (s)
t_f	Fall time of transistors (s)
T_{jmax}	Maximum junction temperature of semiconductor (K)
T_M	MOSFET temperature profile (K)
t_r	Rise time of transistors (s)
T_{vj}	Vehicle junction temperature (K)
V_{block}	Semiconductor maximum blocking voltage (V)
$V_{ce_{(sat)}}$	Collector - emitter saturation voltage (V)
V_{DCbus}	DC-link voltage (V)
V_g	Gate voltage drop (V)
V_{ge}	Gate - emitter voltage (V)
$V_{ge_{(th)}}$	Gate - emitter threshold voltage (V)
V_{gs}	Gate - source voltage (V)
V_s	Source voltage drop (V)
V_{th}	Semiconductor threshold voltage (V)
Y_{ij}	Admittance parameters (Ω^{-1})

Chapter 1

Introduction

1.1 Thesis context

The research work of this doctoral thesis has been developed in the APERT (*Applied Electronics Research Team*) of the Electronic Technology Department in the University of the Basque Country (UPV/EHU). The research activities of this group are mainly focused on the following lines:

❒ **Reconfigurable circuits and Systems-on-a-Programmable-Chip**: this line is based on the usage of next-generation high capacity FPGAs to integrate digital systems on a single circuit, as well as make use of their reconfiguration capability: synthesis oriented design, interconnection architectures and cores, and fault tolerance techniques. Additionally, there are a line in the communication digital circuits for industry 4.0.

❒ **Power and control circuits for energy converters**: this research line is oriented to the design and study of power converters for electric power generation, conversion, storage and transmission. Actually the group is working in the following research lines:

- **Electric Vehicle**: this research line studies and develops improvements on the efficiency, control and cooling systems of power inverters and converters in the traction system of electric vehicles.

- **Power electronics for particle accelerators**: this research line investigates power supplies and their control applied to particle accelerators aimed at scientific research and medical applications.

The work done in this thesis is part of the second line of research, specifically in the research of the power train converter of Electric Vehicles (EVs). The work carried out in this thesis has served for the development of the following research projects:

- ❒ **Drive system, storage and energy management for hybrid electric vehicles based on fuel cell, battery and supercapacitors (ELECTRICAR-P).**

Reference:	DPI2014-53685-C2-2-R				
Financing entity:	Ministerio de Economía y Competitividad (R&D state program oriented to society challenges)				
Participating entities:	University of the Basque Country (UPV/EHU), University Carlos III from Madrid (UC3M)				
Duration, from:	January 2015	**to:**	December 2017	**Budget:**	96,800 €
Head researcher:	Jon Andreu Larrañaga			**Number of researchers:**	12

This coordinated project integrates the capabilities of two research teams from the University Carlos III from Madrid and the University of the Basque Country. The project addresses the propulsion system, energy storage and energy management (powertrain) of hybrid electric cars (HEV) based on fuel cells, batteries and supercapacitors. In the subproject of the APERT group, the research is focused on the vehicle propulsion system, mainly formed by the driver (inverter) and the motor. The main objectives are to: a) develop a hybrid modulation technique based on the combination of vector modulation and harmonic cancellation and its implementation on a real-time platform; b) design, manufacture and validate of an inverter with optimized performance, based on the parallelization of discrete IGBTs and based on new semiconductor materials (SiC and GaN).

- ❒ **Design and development of integrated power modules (POWINMOD).**

Reference:	Art. 83 LOU - ETORGAI				
Financing entity:	Fagor Electrónica S. Coop.				
Participating entities:	University of the Basque Country (UPV/EHU)				
Duration, from:	December 2015	**to:**	May 2018	**Budget:**	241,998.16 €
Head researcher:	Jon Andreu Larrañaga			**Number of researchers:**	7

The main objective of this project is to design advanced power modules based on silicon carbide (SiC) semiconductors. These modules must inherently provide a solution to the thermal, mechanical, electromagnetic and safety aspects through their designs. Likewise, the aforementioned modules must incorporate the control/firing system that guarantees the correct functionality of the power converter.

❒ **Key technologies for new concepts of urban electric transport (KT4eTRANS).**

<table>
<tr><td>Reference:</td><td colspan="5">KK-2015/00047 and KK-2016/00061</td></tr>
<tr><td>Financing entity:</td><td colspan="5">Eusko Jaularitza/Gobierno Vasco (ELKARTEK)</td></tr>
<tr><td>Participating entities:</td><td colspan="5">IRIZAR-CREATIO (consortium leader), CEIT, CIDETEC, TECNALIA and University of the Basque Country (UPV/EHU)</td></tr>
<tr><td>Duration, from:</td><td>September 2015</td><td>to:</td><td>December 2017</td><td>Budget:</td><td>71,264 €</td></tr>
<tr><td>Head researcher:</td><td colspan="3">Jon Andreu Larrañaga</td><td>Number of researchers:</td><td>16</td></tr>
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The objective of this project is to explore new concepts for the electrified city-mobility, conceiving new urban transport vehicles based on future mobility necessities and services for the smart city network. It emphasizes on the following technologies: ultra-rapid recharge and the infrastructure needed to integrate it to the electric-grid, new generation energy-storage technologies for interurban environment, embedded electronics for powertrain and advanced traction, and predictive maintenance. The particular objective of the APERT research team (UPV/EHU) is to maximize the energy density of the propulsion system, by developing new and optimum refrigeration solutions for the power stage.

1.2 Introduction to the research topics

The use of electric energy for propulsion is not new, as it dates back to the 19th century, when Robert Anderson designed the first non rechargeable battery powered electric vehicle. This invention was followed by other similar innovations, such as the vehicle known as "*Jamais contente*" (in the year 1899), which was the first electric vehicle (EV) able to reach 100 km/h [1]. Thus, at the dawn of road transportation, the primitive EV technology had a high market share. As a matter of fact, in the early 90s, there were more electric powered vehicles than petrol powered ones. Likewise, the first hybrid electric vehicle (HEV) was manufactured

in 1911 by Woods Motor Vehicle Company. However, several factors such as the invention of the electric starter for petrol powered vehicles (which eliminated the need of a hand crank), the low price of petrol, and the continuous improvement of many relevant features of Internal Combustion Engine (ICE) based vehicles (autonomy, power, comfort, etc.) lead to the decline of electrified vehicles. Around 1935, there where practically no EVs on the road [1, 2], as the electrical technology available at the beginning of the 20th century was not developed enough to compete with the ICE. However, the reintroduction of HEV/EVs started in the late 90s thanks to the maturity of power electronics [3–5] and digital signal processor (DSP) [6, 7] technologies. Nevertheless, it was not until the beginning of the 21st century when HEV/EVs regained significant popularity [1].

The main reasons of its reintroduction where both an increasing environmental awareness and oil shortage, this last leading to high and fluctuating oil prices. Nowadays, the environmental forecasts are becoming more pessimistic from day to day. According to the projections of the International Energy Agency (IEA), greenhouse gas (GHG) emissions are expected to double in 2050 the 2005 levels, unless decisive actions in climate policies are taken immediately [8]. Provided that the transportation sector accounts for about 23 % of GHG emissions [9], transportation electrification is considered one of the main solutions to reduce GHG levels in the atmosphere and slow down the climate change [10]. In this context and attending to the IEA Energy Technology Perspective BLUE Map scenario, electrified vehicles (EVs and Plug-in HEVs) will contribute to reduce CO_2 emissions produced by light-duty vehicles approximately a 30 % by 2050 [8]. This implies that the sales of PHEVs and EVs vehicles are expected to reach 50 million units by 2050 (figure 1.1 [8]). According to the Electric Vehicle World Sales Database, the PHEV/EV global fleet reached around 5.4 million units in 2018, which represents an increase of 64 % over 2017. In [11], an additional growth of 52 % is expected by the end of 2019. Thus, the global PHEV/EV fleet would reach 8.5 million units in 2019. Therefore and up to date, these recent data and forecasts match with the long term fleet evolution prediction presented in figure 1.1.

In order to achieve the BLUE Map goals, the worldwide adoption of electrified vehicle technologies before 2050 is mandatory. Nevertheless, the penetration of PHEVs and EVs will depend on several factors, such as supplier technologies, retailer's offers and promotions, vehicle specifications, charging infrastructures, consumer's demand and government policies, among others [8]. Currently, government policies largely influence all the others [8]; in fact, many countries are implementing restrictive emission regulations to promote PHEVs and EVs. For instance, the Euro 6 emissions standard is mandatory in the European Union since 2014 [12, 13]. National and international programs such as Horizon 2020

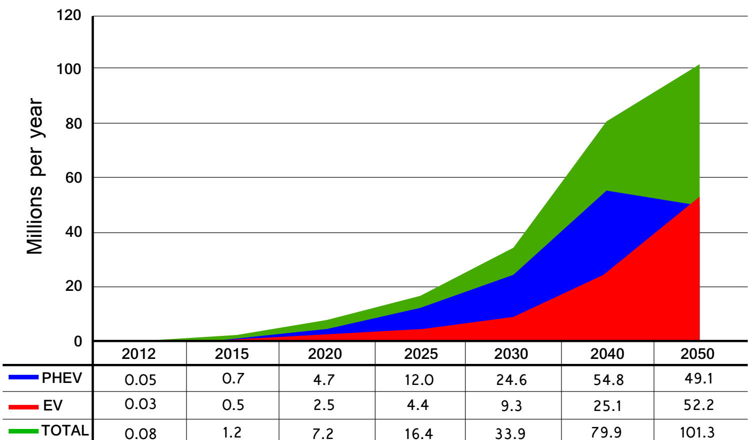


Figure 1.1: Worldwide EV and PHEV sales forecasted by the BLUE Map scenario (in millions per year).

[14, 15], or organizations such as the United States Council for Automotive Research (USCAR) [16, 17], the U.S Department of Energy (DOE) [18, 19] or the United Nations Economic and Social Commission for Asia (UN ESCAP) [20] establish qualitative and quantitative goals for the next generation of HEV/EVs.

From the previous reports, it can be concluded that current and future R&D efforts of the automotive HEV/EV industry should mainly be focused on electric drive technologies (i.e., the power converter, including DC-link capacitors and power semiconductors, the cooling systems and the electric motor), batteries and charging infrastructures. In this sense, figure 1.2 shows the general diagram of an EV, which includes the aforementioned elements. Among them, the power electronics that constitute the core of the propulsion system can be considered of capital importance, as they are responsible of controlling the power flow between the batteries and the electric machine (in motoring operation mode), and vice versa (in regenerative braking operation mode) [21].

The technological targets proposed by Horizon 2020, USCAR, DOE and UN ESCAP regarding the power electronics are stringent (when compared to 2010-2012 data), and can be summarized in the following items:

1. An increase of the power density of the power conversion stage of around 50 % (from 8.7 kW/l up to 13.4 kW/l).

2. A reduction of power converter losses (conduction and switching losses) by 50 %.

3. Significant costs reductions (a reduction by four) for on-board power electronics (from 30 $/kW to 8 $/kW).

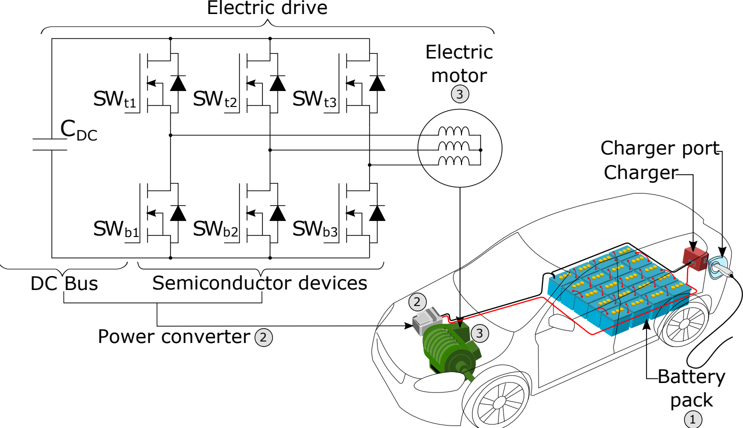


Figure 1.2: Explosion drawing of an automotive electric drive system main components.

4. Simplification of thermal management systems by using on-board coolants minimizing, as possible, the usage of additional components.

5. Whole drive size and weight reductions of 35 % and 40 %, respectively (from 1.1 kW/kg and 2.6 kW/l up to 1.4 kW/kg and 4.0 kW/l).

Specifically, the U.S. DOE's goals for 2020 propose the development of power converter technologies with specific power of more than 14.1 kW/kg and efficiencies greater than 98 %. At the same time, the aforementioned goals aim for a significant cost reduction up to 3.3 $/kW.

Current market technologies cannot achieve all these previous figures. Consequently, an extensive research and development regarding key technologies that constitute the power converter (figure 1.2-②) should be conducted, i.e. advanced thermal management systems [22–24], improved DC-link components and designs [25, 26], power semiconductor technology [27–30], optimized layouts and packaging [31–33] and alternative power conversion topologies [34–36], among others. Thus, it becomes clear that the research topics in this field are wide. In this context, the research line of this thesis takes into account the following power conversion stage design aspects:

- ❒ **Alternative power conversion architectures.** The most suitable alternatives are reviewed in this introduction chapter, and the ones that best suit the application is identified based on the operational requirements of future HEV/EV drive systems. Finally, the fundamental constituting elements of such architectures are derived and taken as reference in the thesis, because they are the fundamental power electronics units to be improved.

- **New power semiconductor devices.** The aforementioned technological goals could only be achieved by using advanced semiconductor technologies. *Wide bandgap* (WBG) semiconductors, especially gallium nitride (GaN) and silicon carbide (SiC) based power electronic devices, have been proposed as the most promising alternative to silicon (Si) devices due to their superior material properties, allowing to improve thermal conductivity, increase the achievable maximum switching frequencies and/or reduce power losses. In this context, an in-deep market analysis is conducted in this thesis in order to provide a whole picture of the current semiconductor technologies and their suitability for automotive applications, specifically the usage of new WBG power semiconductors in automotive power converters.
- **WBG automotive power module design aspects.** As it will be justified, power modules, from different manufacturers or manufactured ad-hoc with available die technologies, are the preferred option to achieve the automotive grade specifications. Considering the particularities of WBG technology, a review and discussion regarding possible power conversion stage layouts and parallelization schemes (required due to the high power ratings of the particular application) are conducted in this thesis, focusing on the available technologies and technical solutions that can be used.

1.3 Power electronics in HEV/EV applications

The determination of the most appropriate power conversion alternatives for both current and next generation HEV/EV drive systems is a topic of relevant importance. The selection of a given architecture (figure 1.2) would depend on the electric parameters of the system (battery voltage and phase currents), and also on a variety of desired features such as high power density, fault tolerance, high frequency operation and cost effective thermal management, among others. Thus, the following sections will provide valuable information, not only for the research community, but also for practical power electronics engineers that are focused on the design of the hardware elements of the power conversion stage of HEV/EVs, providing a list of the most suitable power converter topologies and their design requirements.

1.3.1 Battery and power semiconductors: electric operation conditions

Battery (figure 1.2-①) voltage is one of the key electrical parameters that must be considered for the design of an HEV/EV power conversion stage. According to a number of automotive standards, such as LV 216-1, LV 216-2 and SAE J1654, the maximum battery voltage should not exceed the low-voltage limit of 1500 V due to the following reasons [37]:

(a) Exceeding this limit significantly increases the requirements related to operational safety.

(b) As voltages exceeding 1500 V are not present in the automotive industry, it is very difficult to find automotive grade components that could withstand such high voltages.

Nominal voltages in the range of 300-400 V are common in battery packs installed on small and medium vehicles [37–40], while voltages up to 870 V can be found in sport cars and heavy duty vehicles (table 1.1) [37, 38, 40]. In this context, table 1.1 shows, among other relevant parameters, the common battery voltage levels according to the type of vehicle (electrification degree and vehicle class). Such high voltages (870 V) are also being considered, in general, for future HEV/EVs, because the section of power wires and battery charging times can be significantly reduced [37, 41].

In regard to the current and power ratings that should withstand the HEV/EV drive system power conversion stages, they will depend on the maximum torque and power requirements of the vehicle, and also on the torque per ampere production capabilities of the installed electric machine(s) [42]. When using permanent magnet (PM) based machines, the extra current required during field weakening should also be considered [43–45]. In this context, currents up to 255 A are generally found in three-phase systems with power ratings between 50 kW and 70 kW [43, 46, 47], and up to 480 A for systems of 125 kW [48, 49]. These numbers could significantly increase for high power heavy duty vehicles. The Irizar ieTran (18 m version) is an illustrative example of this statement, as it has a nominal power of 235 kW. Similarly, the Green Power EV350 all electric bus features a maximum power of 300 kW. In this context and taking into account the current ratings of discrete power semiconductors and bare dies, the parallelization (figure 1.3) of power semiconductor devices (or the usage of power modules including parallelized devices) becomes mandatory for all vehicles.

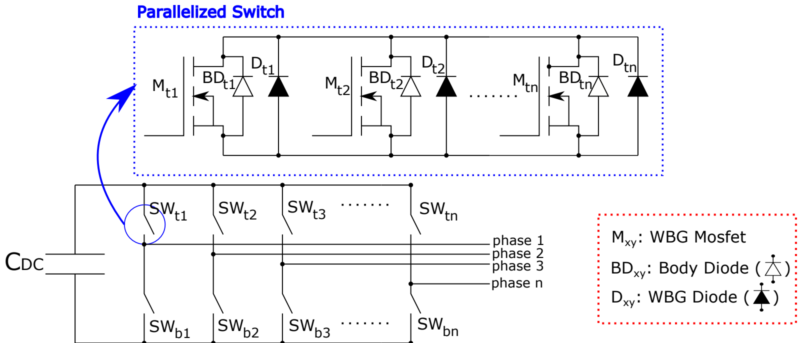


Figure 1.3: Generic power converter topology of future HEV/EV electric drives based on two-level multiphase topologies and with parallelized power switches.

1.3.2 Power conversion topology

Efficient, compact, robust and safe power systems (figure 1.2-②) are desirable for future HEV/EV drives [50]. In this context, it is relevant to identify the power conversion topologies that will best suit future HEV/EV applications. Two-level three-phase power conversion architectures (usually connected to synchronous machines -Toyota, Honda, Mercedes, BMW, Nissan, Volkswagen, etc.- or induction machines - Tesla, Hyundai, etc.) have become the standard in the current automotive industry [43, 47, 51–55]. Most relevant original equipment manufacturers (OEM), such as Tesla, Nissan, Audi, Toyota and Chevrolet rely on such architecture for their HEV and/or EVs [56, 57]. A number of Tier 1 and 2 automotive inverter suppliers such as Semikron (SKAI product family), Cascadia Motion LLC (former Rinehart Motion Systems, including the PM and RM inverter families) and Brusa Elektronik AG (DMC series), to name a few, provide complete two-level three-phase inverters for automotive use for both prototypes or industrialized vehicles. Power electronics suppliers such as Infineon (HybridPack modules), Semikron (SKIM, solderless sinter technology) and Fuji Electric (incorporating direct water cooling), among others, also provide automotive qualified two-level three-phase power modules [57–59]. Nevertheless, an increase on phase levels and number of phases could be considered.

In high power traction applications such as railway transport, it is of common practice to use multilevel converters with medium power semiconductors [60–62], following the well known Neutral Point Clamped (NPC) [63], Flying Capacitor (FC) [64] or Cascade H-bridge (CHB) [65] configurations. A number of benefits can be obtained from their use, such as the improvement of the synthesized voltage and current waveforms and power handling capabilities [60, 66–68]. However, multilevel technology has significant drawbacks for the automotive industry, as voltage oscillations must be avoided in NPC configurations [69, 70], increasing the

Table 1.1: Electric mobility performance class overview for passenger vehicles and commercial vehicles/buses.

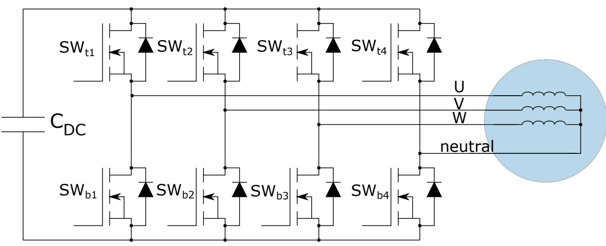
		Mild Hybrid			Full Hybrid/Plug-in		EV (Batt/RE[1]/FCell[2])			Unit
		12 V	48 V	HV	Mid	Power	Small car	Medium car	Sport car	
Passenger vehicles	Max. EM Power	4	12	20	60	100	60	100	180	kW
	Max. EM Speed	50	150	150	200	300	200	300	500	Nm
	Voltage converter DC/DC	--	60/12	200/12	400/12	450/12	400/12	400/12	800/12 420/12	V
	Charger AC/DC	--	--	--	--	230/420	230/400	230/400	230/450 450/800	V
	Battery	15	60	200	400	420	400	400	420/800	V
	Max. current DC[3]	333	333	167	200	400	200	333	550/280	A
	Max. current AC[4]	353	500	500	600	800	250	450	1000/500	A

		Mild Hybrid up to approx. 40 % internal combustion engine				Plug-in hybrid	EV (Batt/RE[1]/FCell[2])			Unit
		7.5 t	7.5-12 t	> 12 t	Bus 18 t	7.5-12 t	7.5 t	7.5-12 t	Bus 18 t	
Commercial vehicles/buses	Max. EM Power	50	65	120	120	90	100	120	2x120	kW
	Max. EM Speed	350	450	1000	1000	500	350	450	2x500	Nm
	Voltage converter DC/DC	400/12	400/24	420/24 800/24	420/24 800/24	420/24	420/12	800/24	800/24	V
	Charger AC/DC	--	--	--	--	3x400/420	3x400/420	400/420	3x400/800	V
	Battery	420	420	420/800	420/800	420	420	420	400/800	V
	Max. current DC[3]	180	223	400/200	400/200	300	330	400	400	A
	Max. current AC[4]	300	350	450/250	450/250	450	450	450	2x500	A

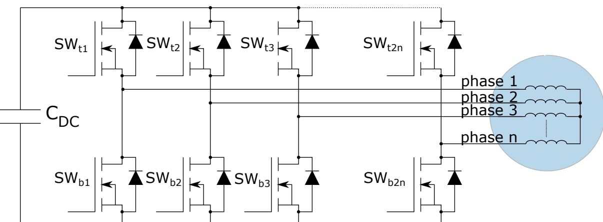
Table notes:
(1) RE: Range Extended hybrid vehicle.
(2) FCell: Fuel Cell vehicle.
(3) Supplied by battery pack.
(4) On electric machine stator.

complexity and computational burden of the control algorithms. On the other hand, system hardware complexity and costs are also increased [60, 66–68, 71, 72]. Taking the latter into account and considering both the battery voltage levels adopted by the automotive industry (section 1.3.1) and current power semiconductor technology, it can be stated that future HEV/EVs will continue relying on two-level power conversion stages.

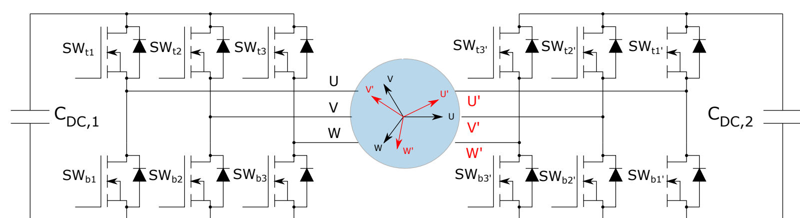
On the other hand, multiphase technologies (figure 1.4) include a number of relevant benefits that the automotive industry could exploit, such as power splitting (which allows greater power handling capabilities or a reduction of parallelization requirements), increased fault tolerance, high efficiency, high power density and lower torque ripple than equivalent three-phase systems [34, 35]. Additionally, some specific multiphase topologies can be effectively reused for battery charging, eliminating the dedicated charge power converter and reducing the volume, weight and overall costs of the vehicle power electronics systems [36, 73].



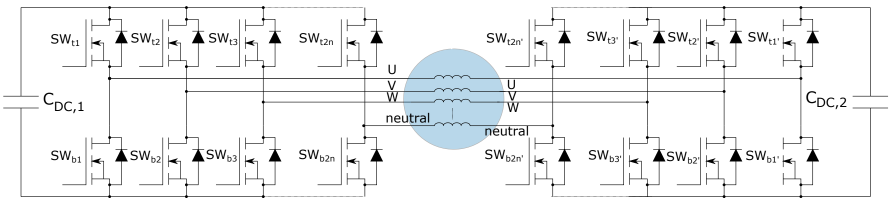
(a) Extension of the three-phase machine fault tolerance including access to the machine neutral.



(b) Multiphase topology with star connected windings and odd phase-number.



(c) Dual three-phase configuration with star connections in windings.



(d) Multiphase configuration for three-phase machine with open windings.

Figure 1.4: Alternative fault tolerant multiphase power conversion topologies for HEV/EV drives.

Additionally, an equivalent n-phase machine can be easily derived from a three-phase machine with the same characteristics and performance [74]. For all these reasons, multiphase technologies are successfully being introduced in electrified transportation systems [75].

Taking into account the current safety requirements for commercial vehicles (refer to the international standard for functional safety ISO 26262), the power system must be designed and dimensioned in a way that the Mean Time Between Failures (MTBF) is maximized. However, as an operation free of faults cannot be guaranteed at 100 %, fault tolerance can be considered as crucial. An extensive research to provide fault tolerance to three-phase systems under open and short circuit faults has been conducted [76–79]. However and thanks to the additional degrees of freedom of multiphase topologies, fault tolerance can be greatly extended by using corrective control strategies, improving passengers' safety and post-fault operation [34]. A number of fault tolerant architectures, such as neutral connected (figure 1.4(a)), star connected (figure 1.4(b)), dual three-phase (figure 1.4(c)) or open winding multiphase configurations (figure 1.4(d)) can be found in the scientific literature. Table 1.2 summarizes the most relevant features of each configuration, including a number of references regarding each alternative.

As a summary, it can be stated that although three-phase technologies have an industrial prevalence due to their maturity and simplicity, it is worth to explore the introduction of multiphase technologies beyond their usage in heavy duty vehicles. From the reviewed alternatives, the open winding multiphase configuration provides additional fault tolerance against machine winding short circuit faults [80, 81]. However, this additional fault tolerance is achieved at the expense of doubling the required power switches when compared to star connected multiphase topologies. Thus, the economical costs of this alternative could be high.

The dual three-phase configuration [97, 98, 102] has two significant advantages over the other two multiphase technologies. On the one hand, it can provide fault tolerance over power supply faults[1]. On the other hand, three-phase solutions (power electronics and control algorithms) can be directly translated into the dual three-phase scenario, simplifying the transition between three-phase and multiphase technologies.

It is important to consider that the degrees of freedom (regarding current control) are the same for both dual three-phase and star connected five-phase machines.

[1] Two separated battery packs could be required to take advantage of this feature, thus increasing the complexity of the vehicular architecture. Such feature can be better exploited in aerospace applications, where various independent high voltage direct current (HVDC) networks are available.

Table 1.2: Summary of the most relevant multiphase architectures suitable for HEV/EV drive systems, including their corresponding references and main features.

Topology	Fig.	Number of elements	Fault tolerance	Refs.[1]
3-phase with neutral[2]	1.4(a)	8 switches[3], 1 DC-link[4]	o.c. faults (control)	[76, 77]
5-phase	1.4(b)	10 switches[3], 1 DC-link[4]	Intrinsic or control (multiple o.c. faults)	[34, 35][75] [82–91]
7-phase		14 switches[3], 1 DC-link[4]		[92]
9-phase		18 switches[3], 1 DC-link[4]		[93, 94]
11-phase		22 switches[3], 1 DC-link[4]		[95, 96]
Dual three-phase	1.4(c)	12 switches[3], 2 DC-link[4]	o.c. and s.c. faults[6]	[97–103]
3-phase open winding	1.4(d)	12 switches[3], 2 DC-link[4,5]	o.c. and s.c. (control)	[76, 104]
4-phase open winding		16 switches[3], 2 DC-link[4,5]	o.c. and s.c. (intr./ctrl.)	[105]
5-phase open winding		20 switches[3], 2 DC-link[4,5]	o.c. and s.c. (intr./ctrl.)	[80, 81]

o.c.: open-circuit / **s.c.**: shortcircuit.

Table notes:

(1) Although some of these references do not strictly apply to HEV/EV applications, their underlying concepts can be extrapolated to automotive applications.
(2) From the power converter point of view, this architecture can be considered as multiphase.
(3) The switch will be constituted by a number of power semiconductor devices in parallel (figure 1.4).
(4) The DC-link may be constituted by a single or multiple C_{DC} capacitors and the corresponding busbar (integrated or not).
(5) Additionally and at the expense of losing some modularity, a single DC-link can be used instead.
(6) In some particular cases, braking torque produced by a short circuit in one of the two three-phase inverters can be compensated by properly regulating the healthy one.

Thus, five-phase architectures can provide an appropriate fault tolerance against open circuit faults [34, 82] with one less phase when compared to dual three-phase technologies. Additionally, harmonic control capabilities of five-phase topologies must be considered [106], as well as their capabilities to cope with up to two open circuit phase faults, ensuring a low torque ripple in the machine [91].

From the previous lines, it can be concluded that automotive power conversion topologies (figure 1.2) will rely on the two-level branch (figures 1.3 and 1.4) as a core constituting element. Thus, special focus on this element should be provided by automotive power electronics engineers to achieve an optimum design.

1.3.3 Influence of future electric machine design considerations on power electronics

The electric machine (figure 1.2-③) technology and its requirements must be also considered in the power converter design. In this sense, weight reduction targets and HEV/EV space constraints have lead to the research and development of high power density drive systems [14, 16, 20]. Being this one of the most important aspects for the automotive industry, the power density of the machine

can be significantly improved using multiphase technologies, as the additional control degrees of freedom allow to control the harmonic injection (generally fundamental and third harmonic), thus increasing torque production capabilities [74, 82, 92, 106]. As an illustrative example, a five-phase PMSM with a quasi-trapezoidal back-EMF distribution is controlled in [106] with fundamental and third harmonic injection, increasing the torque production by 14,5 %. Similarly, a torque enhancement of 20 % is claimed in [107]. For this reason, the use of multiphase topologies (section 1.3.2) is again justified.

Complementarily, power density can be further maximized increasing the operation speed of automotive electric machines, leading to High Speed Electric Machine (HSEM) desing concepts [47, 108–110]. A good example of how power density is improved by increasing the mechanical speed can be found in Toyota HEV IPMSMs. Both second and third generation Toyota IPMSMs have a rated power of 50 kW. The active volume of the second generation machine is of 4.78 l, with a maximum mechanical speed of 6000 rpm, while the third generation machine achieves the same power with an active volume of 2.74 l, as its maximum mechanical speed is significantly higher (13900 rpm) [47]. However, considering the future power density requirements, a great number of automotive machines with mechanical speeds higher than 15000 rpm are expected in the near future [109].

In such a high speed operation, torque control of automotive HSEMs can be challenging due to high fundamental-to-sampling frequency ratios (typical switching frequencies of IGBT based commercial automotive power inverters such as Semikron SKAI and Cascadia Motion PM families have typical switching frequencies ranging from 5 kHz to 12 kHz), which makes the stator current regulation and field weakening control difficult tasks [46, 111–114]. As a result, power electronics' switching frequencies should be significantly increased in order to achieve a satisfactory electric drive performance [115]. Therefore, due to efficiency requirements, the power losses in the conversion stage should be kept low under such operation conditions, future HEV/EV power electronics should rely on *Wide bandgap* (WBG) power semiconductors with low switching losses [30, 116–118].

1.3.4 Thermal management constraints

Appropriate thermal management is required to ensure the integrity (not exceeding the rated operation temperatures) and extend the lifetime (number of thermal cycles) of HEV/EV propulsion system critical elements such as battery packs [119–123], electric machines [124, 125] and power electronics [33, 126, 127], where liquid cooling or air cooling approaches are followed, being currently liquid cooling the preferred option for the OEMs [22].

Cost reduction is one of the main concerns for the automotive industry. In this context, a number of agents have focused on the simplification of the electric drive cooling systems to achieve the aforementioned goal [14, 16, 20]. Nowadays, most commercial HEV/EVs mount two separate liquid cooling circuits, a low temperature loop for power electronics cooling, and a high temperature loop for electric machine cooling (including ICE cooling in HEVs) [22, 33, 128, 129]. The nominal coolant temperatures are of around 65°C and 105°C for the low and high temperature loops, respectively. On the other hand, battery cooling should be provided separately, as the optimum operating temperature of a lithium-ion battery ranges between 20°C and 40°C [130].

Two approaches that have a considerable impact in power electronics cooling are being followed to simplify and reduce the costs of the aforementioned architecture:

(a) The elimination of the low temperature loop, sharing the high temperature cooling loop for both power electronics and electric machine/ICE [33, 129]. In this context, power converter cooling technologies must be very efficient in order to operate at such high coolant temperatures. Indirect water cooling [128] uses a thermal interface material (TIM) between the power module and the cold plate, simplifying the assembly process, but increasing the thermal resistance (R_{th}). Thus, direct cooling [127] should be preferred, as the TIM layer is removed, providing direct contact between the base plate of the power converter and the coolant. In order to further enhance heat transfer capabilities, recent advances in liquid cooling systems include double-sided cooling structures [128, 131], where new assembly and interconnection technologies must be developed (i,e. suppression of wire bonding). Regarding cold plate technologies, modifications on structure and materials can be followed, increasing the surface area and improving the heat transfer. Two examples of these developments are the microchannel [132, 133] and pin-fin [134, 135] cold plate technologies.

(b) The substitution of the power converter cooling loop by a high performance air cooling architecture that makes use of the air flow generated during vehicle movement [22, 129, 136–139]. For example, this alternative can be effectively implemented for in-wheel power electronics/electric machine solutions [140]. It must be taken into account that, although optimized, the heat dissipation capabilities of air cooling are lower than those of liquid cooling.

Both solutions are valid for the reduction of the system complexity and cost, as pumps, coolant lines, remote heat exchanger fans, and coolant fluid can be partially or totally removed from the vehicle [22, 141]. As a drawback, the operation temperature of the power semiconductor devices is increased, leading to possible

reliability problems. This future thermal management scenario justifies again the introduction of WBG technologies, because they have lower power losses and better thermal conductivity than silicon based devices [30, 142, 143], leading to lower junction temperatures on the power switches.

Thus, once the selection of the semiconductor technology has been justified through the influence of the HSEMs (section 1.3.3) and thermal management constraints (section 1.3.4), it is important to analyse the real possibilities that these technologies offer. For this reason, this thesis presents a review of the available *Si*, *SiC* and *GaN* solutions in the market.

1.3.5 Electromagnetic interference constraints

The intrinsic characteristic of HEV/EV electronic systems constitute them as sources of both radiated and conducted electromagnetic emissions (EMI). On the other hand, those systems also suffer from EMI[1] that may affect their integrity [144]. Concerning HEV/EV vehicles using WBG technology, there are specific researches that review their EMI issues [145, 146]. The usage of WBG semiconductors implies that power devices operate at higher frequencies [145, 146]. Consequently, rise (t_r) and fall (t_f) times become shorter than for *Si* technology. Thus, the dv/dt and di/dt derivatives increase the number and order of harmonic components, and introduce high frequency currents that are distributed thorough the elements of the whole propulsion system.

The main sources of EMI, which are common to any type of electronic system, are the following [147]:

- Common mode interferences.
- Common ground.
- Capacitive coupling.
- Inductive coupling.
- Radiated and conducted electromagnetic fields.

To deal with the aforementioned issues, designers should follow PCB design guidelines for EMC (Electromagnetic Compatibility), and also check possible conducted and radiated EMI considering EMC regulations. The applicable regulation for HEV/EVs is the UNECE Regulation 10 [148]. Besides, IEC 61967 [149] (150 kHz to 1 GHz) and IEC 61851 [150] should also be considered.

[1]The EMI affects HEV/EV low voltage equipment such as Electronic Control Units (ECU) and Battery Management Systems (BMS), and also high voltage electronics such as power converters and their corresponding driver circuitry.

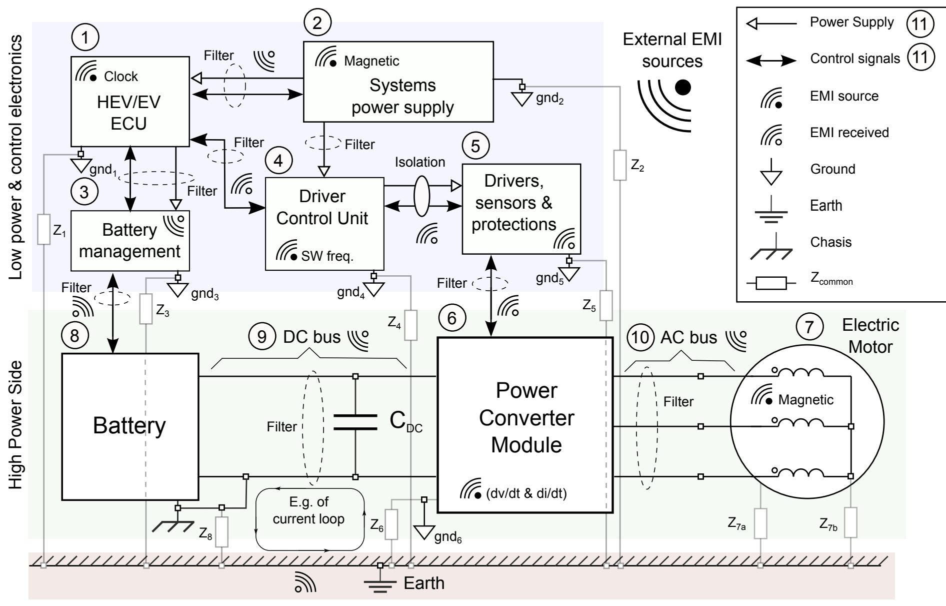


Figure 1.5: Identification of EMI sources in HEV/EV applications.

Figure 1.5 shows the main sources and mechanism of EMI in HEV/EV traction systems. There are many techniques that can be used to deal with the different types of radiated and conducted EMI [147], such as the minimization of the size of current loops, the usage of uniform impedance reference ground plane without cuts to avoid common ground issues, shielding techniques of PCB and/or wires to minimize the radiated magnetic and/or electric fields, the minimization of the length of the wires and tracks, the usage of shielded wires and ferrite beads in power supply, signal and control lines, or CM filtering at both ends of wires to diminish the radiated and conducted interferences. As a summary, table 1.3 lists the specific EMI protection techniques that are applicable to HEV/EV electronic systems.

1.4 Objectives

Taking into account the implementation prospects presented by automotive market with HEV/EV applications where improvements are necessary to solve new challenges, as well as the efforts that are being made in the development of new materials (WBG) and power module optimization, this thesis aims to address the following objectives:

Table 1.3: HEV/EV subsystems, EMI interferences and EMC techniques.

Block of figure 1.5	Subsystem	Main sources and EMI mechanisms	EMC specific techniques	Refs.
①	Electronics Control Unit (ECU)	• Radiated and conducted EMI of CPU main clock frequency and harmonics.	• Digital filtering in the ADCs.	[151–154]
②	Low power supply	• Magnetic fields in unshielded inductances of switched DC-DC converters and filters	• CM power line filtering or ferrite beads at both ends • Use toroidal or shielded inductances	[155–158]
③	Battery management	• Commom EMI issues	• EMI filtering	[155, 156] [159]
④	Drivers Control Unit	• Interferences from the dv/dt and di/dt.	• Layout design	[160–162]
⑤	Driver	• Radiated and conducted from the dv/dt and di/dt. • Insuficient isolation produce electric coupling EMI.	• Minimum track clearance adjusted to the maximum voltage levels and the electrical strength of the PCB or DBC substrates. • Control signals in differential mode (DM) • Optocopled control signals • Fiber optic for control signals	[163–167]
⑥	Power module	• Specially in WBG devices EMI from dv/dt and di/dt of the PWM switching frequency and harmonics. • Power devices feedback loops with self resonant frequencies cause oscillations in the power ramp-up of the devices. • Distributed parasitic inductances and capacitances in the power and control lines.	• Snubbers. RC filters and RF tramps for attenuation of the overshooting frequencies and damping the transfer response of feedback loops within the power devices. • Modulation techniques for harmonic suppression. • Substrates with higher electric strength. • Increase the thickness of PCB conductive layers and tracks to improves the current distribution and reduce the parasitic distributed impedances.	[160–162] [168–176]
⑦	Motor	• Electromagnetic fields produced in the winding	• Winding techniques and stator configuration	[177]
⑧	Battery	• Commom EMI issues	•EMI filtering	[155, 156] [178]
⑨	Power DC Bus	• Discontinuous load currents. • Voltage drops in the wires due to their equivalent series resistance. • Coupled or radiated EMI into the wires. • Current density distribution in conductors.	• Voltage ripple reduction with capacitors and filtering. • Filtering inductances shielded or with toroidal cores. • Type of wires: laminated or multifilar) • Laminated bus structure minimize distributed inductance and equivalent bus resistance.	[163] [179–181]
⑩	Power AC Bus	• EMI coupled or radiated into the wires	• RLC filtering for overvoltage suppression. • Type of wires (laminated, multibifilar)	[163, 177]
⑪	Control and power wires	• Commom EMI issues	•Twisted wires. •Ferrite beads in the wires.	[163]

1. Analyse the technology of the current power modules based on silicon (*Si*) power semiconductors in order to know the main limitations of this technology.
2. Analyse the current situation of new material devices (WBG) and their implementation in HEV/EV applications. Studying the availability to develop automotive power modules based on this technology and market trends.
3. Determine a specific design criteria in order to develop an automotive power module. Providing a detail answer to the concepts of symmetry and parallel design application.
4. Apply the proposed design criteria in power circuits based on printed circuit boards (PCB) in order to check the results of applying specific design concepts on a power circuit.
5. Propose and develop a power module for HEV/EV according to automotive requirements needs, new challenges and design criteria extracted from previous steps. Obtaining its characteristic parameters, electrical and thermal behaviour in order to validate the improvements of applying the concepts and methodology of the defined design process.

1.5 Document structure

This thesis consists of eight chapters and two appendix. In addition to this introductory chapter, the content of the document is divided as follows:

2 **Silicon (*Si*) power semiconductor technology.**
In this chapter, the most relevant silicon (*Si*) semiconductor for power electronics is analysed, the IGBT (*Insulated Gate Bipolar Transistor*). This thesis is based on the implementation of new materials (WBG) for automotive power module development. However, it is considered pertinent to analyse the current silicon semiconductor technology because IGBTs are a proven technology and the market leader. Thus, a review of IGBT evolution and technological advances is presented. In this analysis, IGBT structure is divided in two main parts: the cathode side (IGBT cell) and the anode side (IGBT vertical structure). Moreover, according to the technological processes applied to each IGBT part (cell or vertical structure), many device architectures appear in the market. These main IGBT architectures are explained, focusing on device static, dynamic and thermal behaviours, showing their advantages and disadvantages, and comparing architectures each other.

3 ***Wide bandgap* (WBG) technology.**
As it is indicated previously, the *Si* material is a mature and reliable technology, but it presents some limitations which can be solved with the usage of new materials, so called *wide bandgap*. In this chapter, new WBG materials are presented, specially silicon carbide (*SiC*) and gallium nitride (*GaN*) are noted for their implementation in power electronic application where *Si* technology is not enough. These semiconductors are used due to their higher blocking voltage, thermal conductivity and higher switching frequencies compared to *Si*. Thus, an study of commercial *SiC* and *GaN* devices which can be implemented in HEV/EV power modules is presented, explaining their advantages and disadvantages. As it is shown, the study provides a general and updated vision of voltage and current ranges, sort out by type of device and manufacturer. Moreover, in the case of *SiC* technology, where there are further developments, the main device characteristic parameters of discrete devices and full *SiC* power modules are included and explained.

4 **Parallelization of power semiconductors.**
In order to provide power density requirements, semiconductor parallelization must be implemented. In this chapter, the fundamentals of semiconductor parallelization are presented taking into account the static and dynamic behaviour of semiconductor, the driver connections and the power layout. In this context, typical semiconductor parallelization problems are identified, providing a overall view to implement parallelized connections and the basic techniques which reduce device imbalance effects. All this, with the aim of implementing these recommendations into a power module based on parallelized power semiconductors.

5 **Analysis and definition of the power module design criteria.**
Starting from HEV/EV application view, developing a power module based on WBG devices is an interesting option to meet the new market requirements and challenges. Taking as references the two-level branch as constituting element for conversion topologies (chapter 1), the semiconductor knowledge (chapters 2 and 3) and semiconductor parallelization premises (chapter 4), a complete and detailed design criteria is synthesized in order to constitute an automotive *SiC* power module. In this chapter, commercial and innovative literature solutions are collected, analysed and processed in order to propose correct and detailed criteria, where symmetric connections and other strategies try to balance the parallel semiconductor connections and reduce layout stray inductances.

6 **Parallelization of power converter circuits (PCC) according to the proposed design criteria.**
Taking into account the design criteria defined in chapter 5, they are implemented in three power circuits in order to validate their effectiveness. In this chapter, a power switch composed of 4 IGBTs in parallel, a *SiC* half-bridge converter and DC bus are proposed and simulated, extracting their equivalent parasitic impedances, electrical behaviour and current density distributions. All these data show that current imbalances and parasitic inductances are reduced using the concepts extracted, developed and explained previously in the defined design criteria.

7 ***SiC* half-bridge module development based on the proposed design criteria.**
The simulation data extracted from the basic circuits (chapter 6) verify the usage of the proposed design criteria (chapter 5). These two items are founding basis knowledge in order to get enough experience for the implementation of a *SiC* power module according to thesis design criteria. In this chapter, two proposals of a *SiC* half-bridge (two-level branch topology) are presented, detailing the application of criteria in each power module part. The extraction of equivalent impedances and layout electrical behaviour show the effects of applying symmetry and other mechanism to balance and reduce parasitic inductances. These type of electrical studies are similar to electrical analyses of chapter 6 for PCB substrate, but in this cases the PCB is replaced by a hybrid solution substrate (PCB + DBC). Additionally, the thermal behaviour of a power module is fundamental to know its reliability, therefore thermal results of each proposed power layout are extracted and validated according to an specific simulation methodology also defined in this thesis (appendix B).

8 **Conclusions and future work.**
This chapter presents the conclusions drawn from this thesis, as well as the main contributions of it. Moreover, the publications derived from this work are described and several lines of research proposed by the author are listed to give continuity to the work addressed in this thesis.

A **Extraction of parasitic elements from the designed power electronic modules.**
In this appendix, the extraction method in order to get equivalent parasitic elements from a circuit is explained, focusing on the usage of *S-parameters*. This method is typically used in radio-frequency applications and their design software, as *Keysigh* ADS^{TM}. This RF software is used for electrical simulations in this thesis due to the increment of semiconductor switch-

ing frequencies. Moreover, the basic mathematical equations of Moment Method (Momentum) are presented to extract the circuit equivalent electromagnetic model which defines the electrical behaviour. Finally, these circuit simulations require a high computational load, so that the usage and communication with a distributed computational platform is implemented. For this reason, the main technical characteristics of clubster used in this thesis, *Arina* (UPV/EHU), are presented.

B **Thermal 1D and 3D simulations for driving cycle profiles.**
Aside from the electrical behaviour, the thermal response of power modules is fundamental. These designs are based on different layers assembly, where extracting the temperature distribution according to real operation conditions can solve design process mistakes, reliability problems and increment circuit development. In this appendix, the hybrid methodology based on 1D (Matlab-Simulink) and 3D (COMSOL Multiphysics) simulations is presented in order to extract the power module thermal behaviour according to driving cycle profiles of automotive industry.

Chapter 2

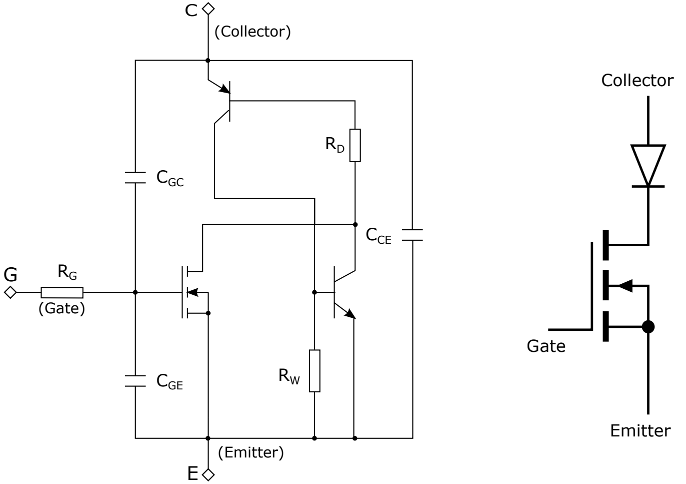
Silicon (*Si*) power semiconductor technology

2.1 Introduction

The IGBT (*Insulated Gate Bipolar Transistor*) was invented in the United States by Wheatley and Becke around 1982 [182]. Approximately 10 years after its invention, IGBTs were introduced to the market through manufacturers in Japan and Europe. In a short period of time, the IGBTs gained great relevance in power applications, replaced bipolar power transistors and became an alternative to VDMOS technology [183].

The IGBT was born as a hybrid between the MOSFET and BJT transistors, providing the advantages of both devices. The equivalent circuit is shown in the figure 2.1(a), where the device intrinsic capacitances are identify, the figure 2.1(b) shows its darlington representarion. This device is controlled by voltage, has a high input impedance and an output characteristic that allows it to drive high current densities. The frequency ranges in which the power IGBTs operate can be around 10 kHz (even reaching 100 kHz [184]). They are also capable of driving currents in the range of hundreds of amperes and blocking voltages in the range of 600 V to 6 kV. The device switching to *on* and *off* state is straightforward, it provides low losses and exhibits short switching times.

The figure 2.2(a) shows a classification of the power devices and their applications according to their voltage and current ranges [185, 186]. Figure 2.2(b) also or identifies the most common application frequency ranges.



(a) IGBT with the parasitic elements. (b) Darlington circuit.

Figure 2.1: IGBT equivalent circuit representations.

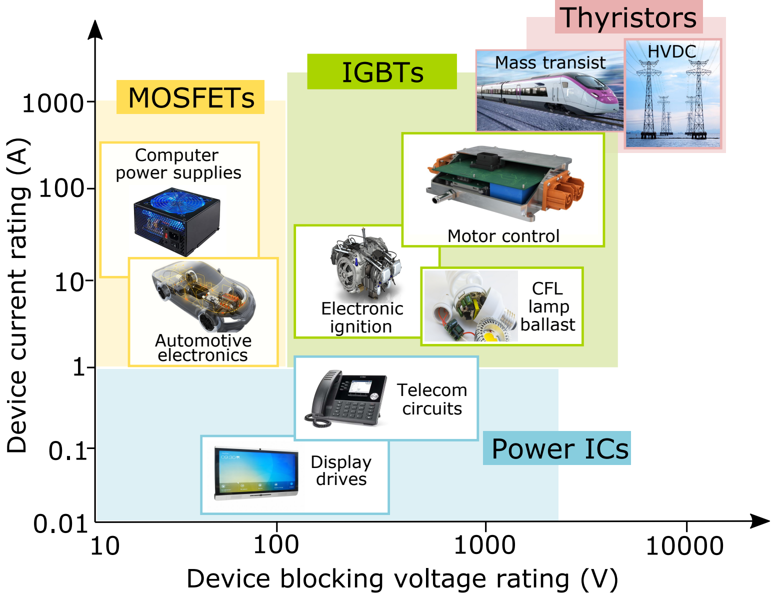
Nowadays, the main IGBT innovations are focused on the reduction of static and dynamic losses, improving the low forward voltage ($V_{ce_{sat}}$) and fast switching behaviour, as well as improving the robustness of these devices[1].

At the same time, the manufacturing costs of the devices must be reduced, based on the size reduction of *die*[2]. This reduction is against the goals of device robustness and shortcircuit capabilities [187]. Therefore, there is a compromise among the reduction of power losses, the price and the robustness must be maintained.

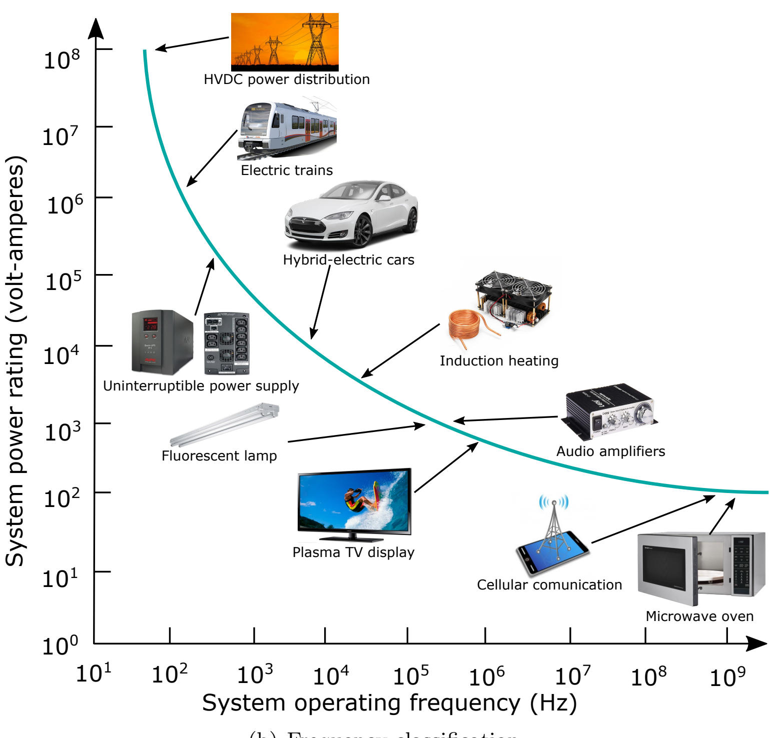
At present, IGBTs are a proven technology with an extend device portfolio that covers the requirements of different applications. In this context, there are many IGBT manufacturers in the market such as Infineon, Semikron, Fuji, Mitsubishi, ABB, Hitachi, Dynex and others. Thus, *Si* IGBTs become the main option in order to develop power modules for medium power ranges such as HEV/EV and traction. Taking into account the relevance of this power device, this chapter has the aim of analysing *Si* IGBT technology, checking its technological evolution and its available options in the market.

[1] Specifically, the overcurrents during turn *off* process and the capacity to withstand shortcircuits.

[2] It is the small semiconductor block on which the device is built. For IGBTs, the silicon block on which the device is built.



(a) Voltage and current ranges classification.



(b) Frequency classification.

Figure 2.2: Power electronics applications.

2.2 IGBT technology and evolution

With the aim of understanding and classifying the technology of silicon IGBTs, in this chapter the IGBT design concepts are analysed taking into account the two main parts (section 2.3) which constitute this power switch:

- IGBT cell: it is the transistor top side where the emitter and gate terminals are located. The variety of architectures, which compose this device part, can be named as cathode technology.
- IGBT vertical structure: it consists on the drift region, the optional buffer layers and collector terminal. The configurations and options, which compose this area, can be named as anode technology.

The evolution of the IGBT cell and vertical structure is shown in the figure 2.3 [188] with the most relevant IGBT topologies. Firstly, the vertical structure using planar cells showed a major development, finding innovations on the thin wafer technology such as *punch through* (PT) and *non punch through* (NPT). From the fusion of both technologies (PT and NPT), the *field stop* (FS) topology emerged. Later, the *trench* cell technology was applied over vertical structure innovations, emerging the *trench field stop* (Trench FS). Finally, the present IGBT development is focused on the evolution of Trench FS topology through the mix of technological concepts, finding new vertical layers and combining *trench* technology with new planar innovations, such as carrier stored or hole barrier layers.

The figure 2.4 shows the electric fields and the layer structure of the IGBT technologies. The details of IGBT architectures are analysed in the following sections, focusing on their electric field generation, their voltage and current ranges and their static-dynamic behaviours, where understanding the temperature influence is fundamental. Apart from this general classification, the most important enhanced architectures of IGBTs, SPT$^+$ and CSTBT (figure 2.5), also are studied.

2.3 Cell and vertical structure technologies

The low power losses, both in conduction and switching, have made IGBTs increasingly attractive for the industry. The power losses and robustness (shortcircuit capability) improvements are mainly due to the carrier concentration and the control of its lifetime through the implementation of new structures [189–191].

The improvement of carrier concentration try to enhance the electron injection in the chip top (emitter side), minimizing the back injection of holes. The idea is to produce a vertical flow of electrons and holes, reducing the forward voltage drop and increasing the *latch-up* current [183]. The minimization of carrier lifetime

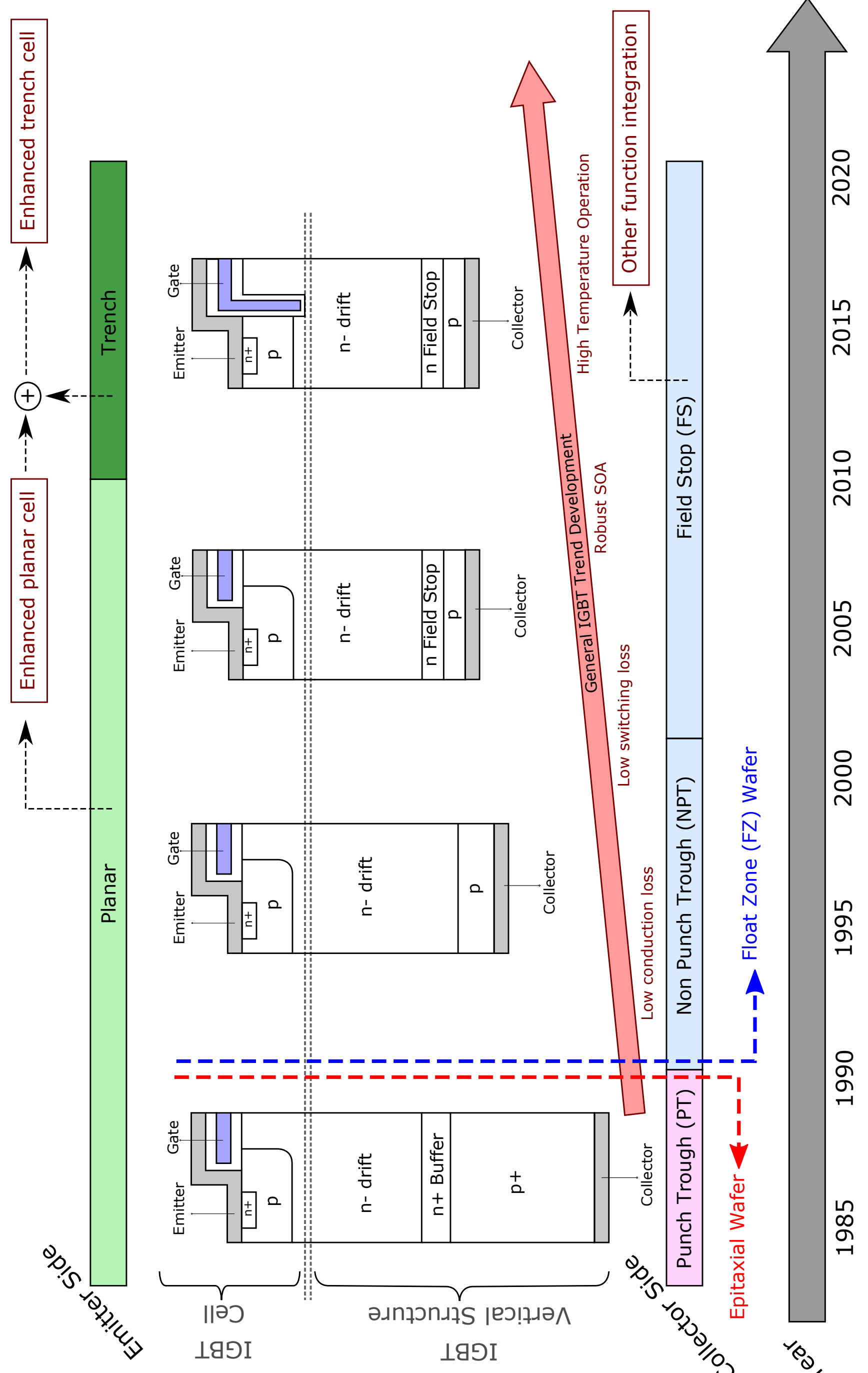


Figure 2.3: IGBT development with the main advances.

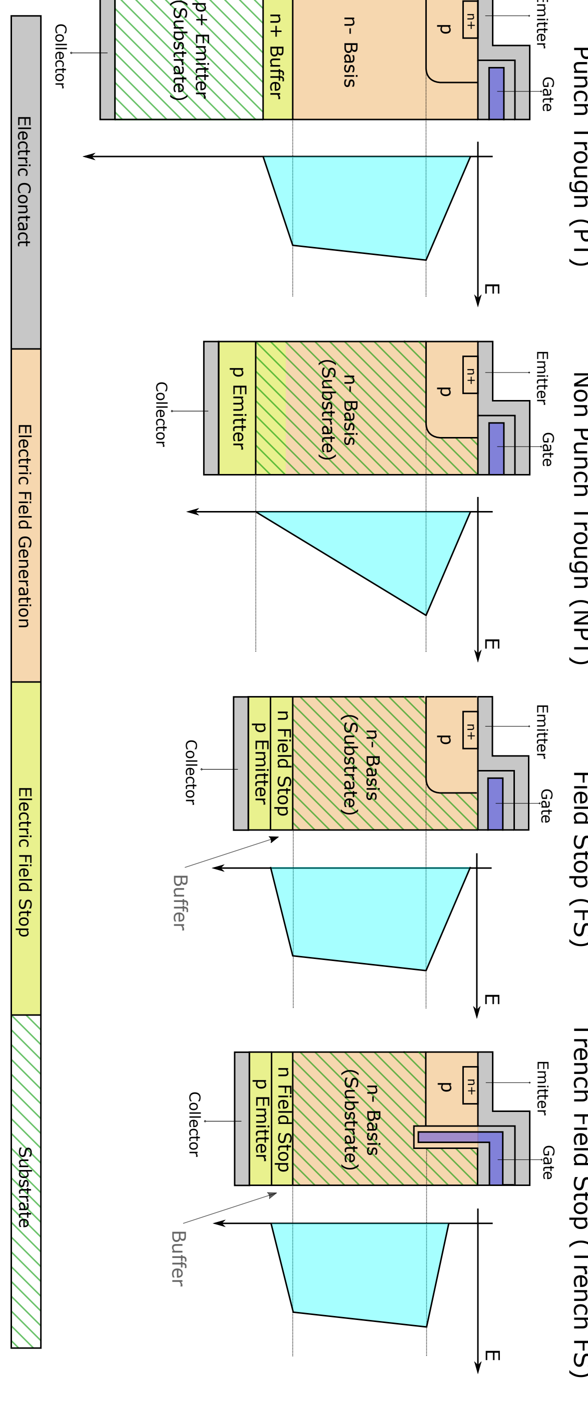
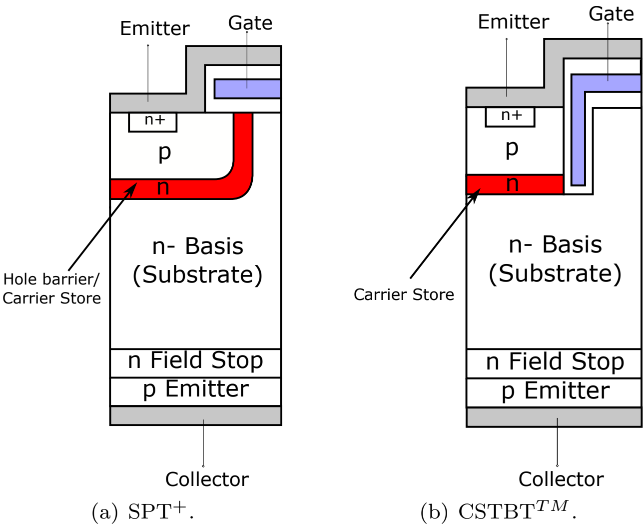


Figure 2.4: Main IGBTs topologies with their electric fields and layer structures.



(a) SPT$^+$.
(b) CSTBT^{TM}.

Figure 2.5: Enhanced IGBT structures.

produces an increment of carrier recombination, which is equivalent to reduce the tail current during turn *off* process, so switching losses are improved [192]. In this context, the problem is to find a balance between both the concentration and the lifetime, because a high concentration of carriers in the chip top could result in longer turn *off* time, as the excess of carriers cannot be removed fast enough [193], thus increasing turn *off* losses.

In general, the manufacturers get these improvements (low forward voltage and fast turn *off* process) through innovations in various parts of the IGBTs. These innovations could be classified according to the two main parts of the IGBT architecture: the chip top surface (IGBT cell) and the vertical structure (drift and other optional layers), as the figure 2.6 shows.

2.3.1 IGBT cell: planar and *trench* technologies

The IGBT cell technology can be classified in two types:

(a) Planar: the first IGBT topologies presented a planar DMOS top surface. This structure consists of a vertical power MOSFET constructed on a layer doped by *p*-type impurity [188]. The conventional planar cell (figure 2.7(a)) offers high forward voltage drop ($V_{ce_{sat}}$). In order to reduce the conduction losses, the designers focused on the optimization of the cell dimensions and the doping profiles [194].

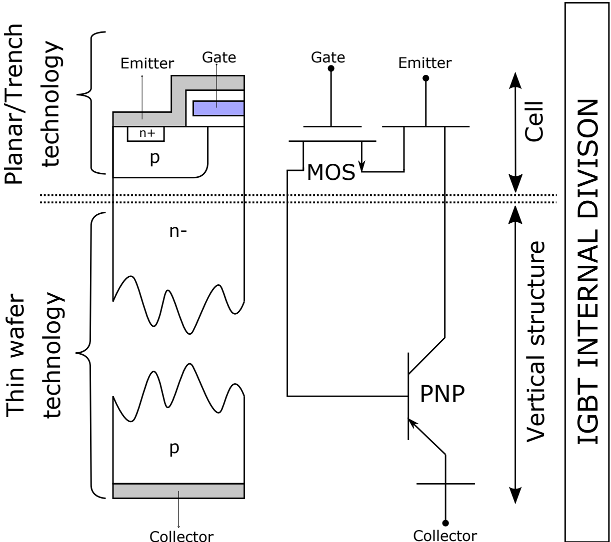
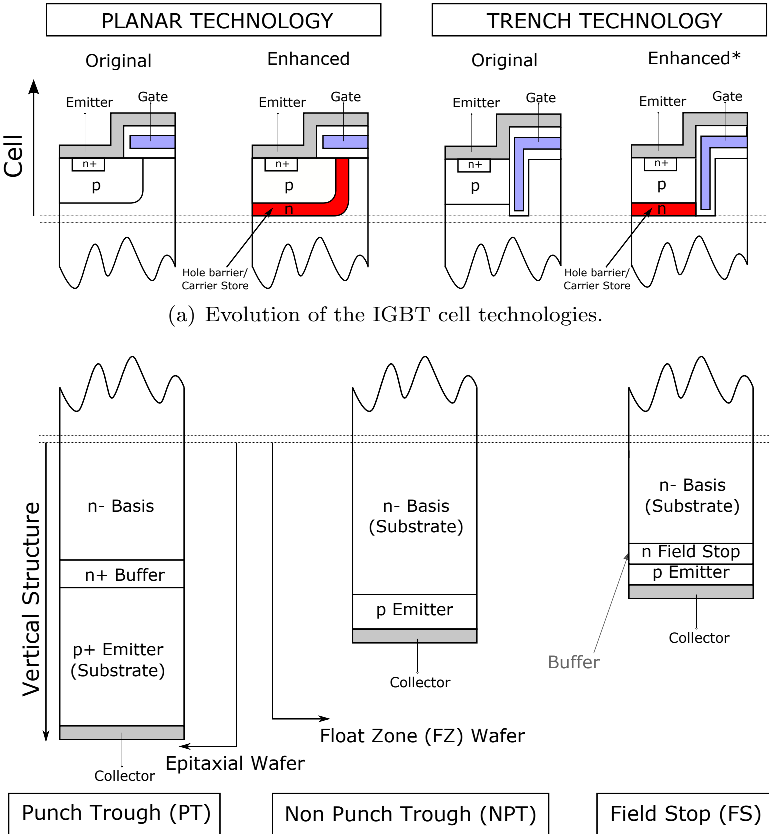


Figure 2.6: IGBT internal structure and Darlington equivalent circuit.

An important evolution of planar technology was the implementation of a lightly doped n layer, whose name is hole barrier or carrier store (figure 2.7(a)), in order to reduce the JFET effect in planar power MOSFETs. This method increases the plasma density near the emitter and reduces the forward voltage drop (figure 2.8 [194]). In this sense, a reduction of up to 30 % in conduction losses was obtained compared with the conventional planar devices, apart from a higher robustness in the turn *off* and shortcircuits. However, the main drawback is the possible reduction of the IGBT voltage blocking capability due to an inadequate layer depth [194]. This enhanced of planar cell technology is applied to the HiGT [192] (Hitachi) and SPT^+ [195] (ABB) where this kind of cell can be a rival for *trench* cell designs [194].

(b) *Trench*: this cell architecture (figure 2.7(a)) has constituted a milestone in the limitations of planar technology, which do not allow to have enough carrier conductivity in the emitter, reducing conduction and switching losses. This carrier concentration on the emitter side is possible to be analysed in the figure 2.9. The *trench* technology integrates a vertical MOS channel to flow holes and electrons vertically, allowing to reduce the forward voltage drop (reducing the conduction losses in a 30-40 % [196, 197] in comparison with the original planar architectures) and increase the current *latch-up* [183, 184, 198].



(a) Evolution of the IGBT cell technologies.

(b) IGBT thin wafer technologies.

(*) Combination of *trench* and planar technologies.

Figure 2.7: Cell and vertical structures technologies.

The insertion of the MOS channel into an IGBT required many efforts in order to obtain a *trench* structure. The first solution of this technology combined the injection enhancement effect with a planar IGBT structure, resulting in a IEGT [199] (Toshiba). This *trench* technology is conditioned by the geometric dimensions. The width and separation of *trench* structures directly influences the forward voltage drop, causing a conductivity variation in the upper part of the layer *n-drift*, because of the accumulation of carriers [196], as figures 2.10(a) and 2.10(b) shown [189, 200].

Finally, the recent IGBT designs are combining both the concepts, the advance planar technology and the *trench* technology. This is possible to see in the figure 2.7(a), where the hole barrier or carrier store layer is added to the

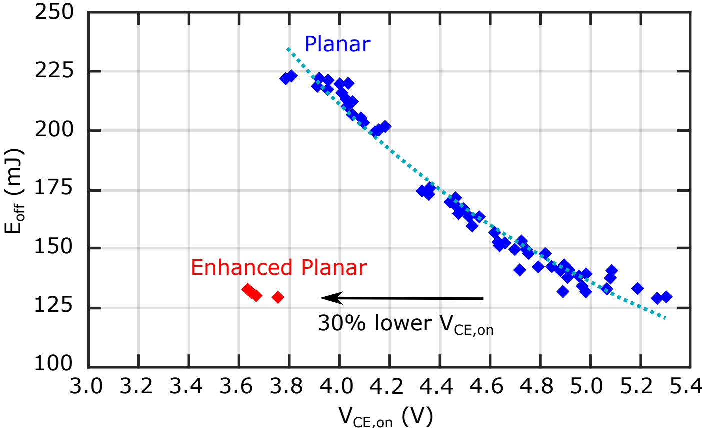


Figure 2.8: Improvement of planar cells with hole barrier/carrier store layer.

trench cell in order to improve the carrier concentration in the emitter. This carrier concentration of electrons and holes must be balanced, since an excess of carriers requires more time for the recombination process, increasing the turn *off* losses [193]. This enhanced *trench* topology is used in commercial IGBTs as the CSTBT (Mitsubishi), which will be studied in the following sections.

2.3.2 IGBT vertical structures: thin wafer technology

The other IGBT advances are focused on the technology of the IGBT vertical structure where the thin wafer technology has experimented many changes. The IGBT collector side can be designed with two kind of substrates: Epitaxial Wafers and Float Zone (FZ) wafers, as the figure 2.7(b) shows.

The epitaxial wafer technology was employed in PT structure which increases the expenses on silicon material and introduces many restrictions in order to get blocking voltage higher to 2 kV. This technology needs the control of carrier lifetime and shows a poor shortcircuit capability, with many problems for the parallelization of the devices [193].

The development of FZ wafers solved the main problems of epitaxial technology, reducing significantly the cost (less material) and increasing high voltage field (wider *n-Basis*). The Non Punch Through (NPT) structure is the first example of FZ wafers, improving the withstand capability and no control of carrier lifetime [193].

The next step in the thin wafer evolution was to join the advantages of PT and NPT technologies in order to improve power losses. Thus, an improved vertical

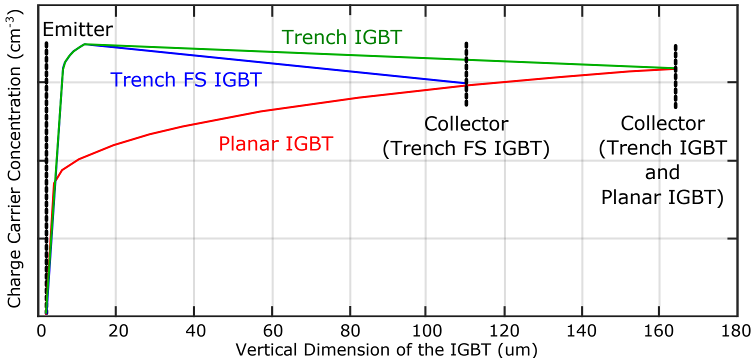
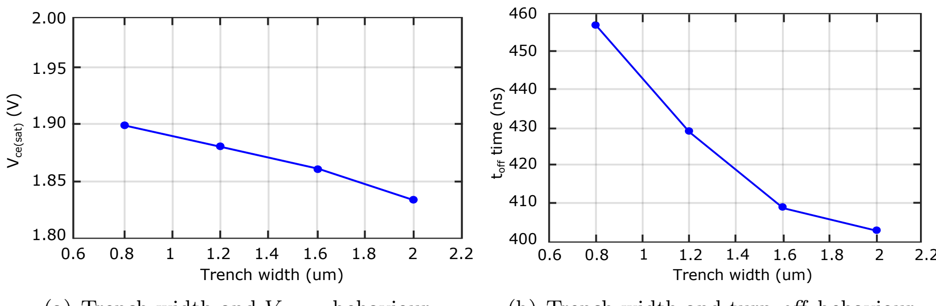


Figure 2.9: Comparative of the carrier concentration for the IGBT topologies.



(a) Trench width and $V_{ce_{sat}}$ behaviour. (b) Trench width and turn *off* behaviour.

Figure 2.10: Conduction and turn *off* behaviour of *trench* IGBTs according to *trench* cell width.

structure emerged, whose name is *Field Stop* (FS) or also called *Soft Punch Trough* (SPT of ABB) [194] or *Light Punch Through* (LPT of Mitsubishi) [184], depending on the manufacturer. The FS is the evolution of conventional PT and NPT. In this process of improvement, the design of the *n-* basis layer (figure 2.7(b)) has been fundamental to obtain low losses, high SOA and highvoltage blocking capacity, as well as the implementation of a layer of *n-buffer* [194].

According to the temporal evolution and development of the IGBTs (figure 2.3), the present developments are focused on the combination of *trench* cell technology with the most recent evolution of FS architecture (Trench FS and CSTBT). Moreover, thin wafer technology is focused in adding new capabilites, such as the reverse blocking (RB) IGBT or reverse conducting (RC) IGBT. In the following sections, the main characteristics of the IGBTs are explained in more detail.

2.4 *Punch Trough* technology: PT IGBT

The PT topology with planar cell configuration constitutes the beginnings of IGBT technology [201]. Initially, it was designed for breakdown voltages lower than 600 V, where the layer $n^+ - drift$ acts as *buffer* to prevent from expanding the area of electric charge. With the technology evolution, the voltage range of these devices has been growing without exceeding 1700 V, since it is difficult to obtain a little doped epitaxial layer. In case of exceeding this voltage range, the layer would be very thick and expensive, being inefficient (there are other topologies for higher voltage ranges).

In this structure the charge space region, doped slightly with n, extends through the base region and exhibits a distribution of the electric field with a trapezoidal shape. The n *buffer* layer (located between the n base and the p^+anode) is necessary to prevent the charge space zone from reaching the anode [202]. The structure of this PT technology, as well as its electric field can be seen in the figure 2.4.

The main characteristics presented by PT technology can be summarized according to the following behaviours:

(a) Static: in this device the tail current is reduced by the application of an irradiation process during manufacturing, obtaining voltages of the intrinsic diode (figure 2.1(b)) lower than in other topologies [203]. However, this technique produces an increase in the recombination speed, which results in an increment forward voltage drop. This means that it is necessary to reach a commitment at the time of manufacture between reducing the tail current and increasing the voltage drop [183].

    The PT technology allows the IGBT to withstand shortcircuits for several microseconds. This functionality is due to the current limitation because of the saturation of electrons speed in the MOS channel, and to the transition to the active region of bipolar transistor in the IGBT equivalent circuit. The saturation current is adjusted by the geometry used in manufacturing. However, improving the shortcircuit capacity increases the forward voltage drop, which involves a compromise between these characteristics according to the application [183].

(b) Dynamic: regarding switching losses, the PT presents lower losses than other architectures as the NPT. However, the main disadvantage is the increment of the current tail with the temperature, increasing the losses. Unlike in the NPT, it has a stable behaviour against temperature. In addition, these losses are very different between devices of the same architecture, mainly due to the variable losses of the intrinsic diode (figure 2.1(b)) [204].

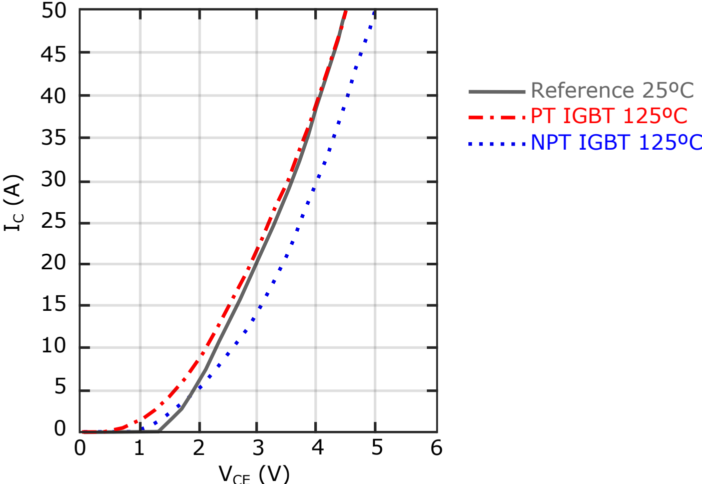


Figure 2.11: Behaviour at different temperatures of the voltage $V_{ce_{sat}}$ over the current I_c for the PT and NPT IGBTs.

(c) Thermal: the PT IGBT devices are known to have both temperature coefficients (positive and negative), depending on where the operating point of the device is located, how the device is doped and the lifetime settings used [184]. The semiconductor substrate has a negative temperature coefficient. When the temperature increases, the intrinsic charge of the n carrier concentration increases, causing the reduction of the semiconductor resistance.

In summary, the $V_{ce_{sat}}$ is reduced, when the temperature increases. This means that the PT technology has a negative temperature coefficient and, in many cases, the change from the negative to the positive temperature coefficient does not occur until the nominal current is exceeded [184]. Moreover, it is possible and common to found a change of the temperature coefficient in the same polarization curve [205].

Taking these into account, it becomes more difficult to connect several PT IGBTs in parallel. If these IGBTs are not correctly coupled[1], significant current differences can be produced between the IGBTs, causing the failure of the power converter. In this way, the parallelization of the PT devices can be feasible, but their classification or preselection is necessary to carry out according to the $V_{ce_{sat}}$, in order to choose those devices more similar of the lot. In the figure 2.11, the behaviour of the PT IGBTs are shown as a function of the temperature [184].

[1]A temperature variation of less than 15°C can be assumed between the IGBTs connected in parallel [184].

2.5 *Non Punch Trough* technology: NPT IGBT

Initially, the NPT technology was designed to work in voltage ranges higher than 1200 V, overcoming the technological limitations presented by the PT devices, with respect concerning high voltages. Although, the advances in recent years have improved the behaviour of this technology at lower voltages[1] [205]. In this sense, NPTs with good performance are obtained in the range of 1000 - 1200 V, under this circumstances, PT structures present generally better performances [183].

The NPT technology is based on the realization of the union $p^+ - n^-$ of collector with a very thin p^+ layer. This causes an injection of holes in the base regardless of the temperature and current levels. The thickness of the substrates (region n) must be wide enough (thicker than PT structure) to avoid that the space charge zone reaches the layer p^+, causing a shortcircuit [183] and the *latch-up* phenomena[2]. The figure 2.4 shows the basic structure of an IGBT with NPT technology with a n base thickness more extensive than the space charge area, causing a triangular electric field distribution [202].

On the other hand, improvements in the manufacturing and handling processes of the wafers are making possible the attainment of devices with smaller thickness for the same blocking voltages [202]. The main features of this technology compared to PT technology are the following:

(a) Static: the conduction losses are greater than in the PT devices, due to the wider thickness of the base layer (figure 2.4) that produces an increase in resistivity. In order to reduce such losses, it is necessary to improve the behaviour of the intrinsic diode. This diode has a higher forward voltage drop than PT devices, because the NPT device does not present the *buffer* layer [205]. Therefore, for the same size of *die* the NPT devices have a higher $V_{ce_{sat}}$ than the PT.

(b) Dynamic: the tail current produced during the turn *off* process is not so high, but it lasts much longer compared to the PT technology [205]. This causes higher switching losses due to the length of the tail current, comparing with the PT devices [202].

    A virtue of the NPT is that the switching losses are similar between one device to another of the same NPT architecture (not as in the case of PTs,

[1] The NPT technology has been improving its performance, obtaining good results even in voltage ranges of 600 V, natural niche of the original PT devices.

[2] The parasitic thyristor turns *on*, causing the loss of control in the device and its possible breakdown.

Table 2.1: PT and NPT technology comparative.

Parameter	PT	NPT
Silicon substrate	$p^+/n/n^-$ epitaxial	n^- Float Zone (FZ)
Electronic irradiation	Yes	No (only some cases)
Current	Increase or decrease with T	Decrease with T
Turn *off* time	Increase with T	Constant with T
Voltage range	600 - 1200 V$^{(1)}$	1200 - 1700 V$^{(2)}$
Reproducibility	Medium	High
Shorcircuit colletor	No	Possible

Table notes:
(1) The present ranges of this technology are 300-1700 V.
(2) The present ranges of this technology are 600-4500 V.

where the difference between devices of the same PT technology differs considerably). In this sense, the NPT technology allows reducing the dispersion of electrical characteristics between manufacturing batches, helping the process of parallelization of several devices with each other.

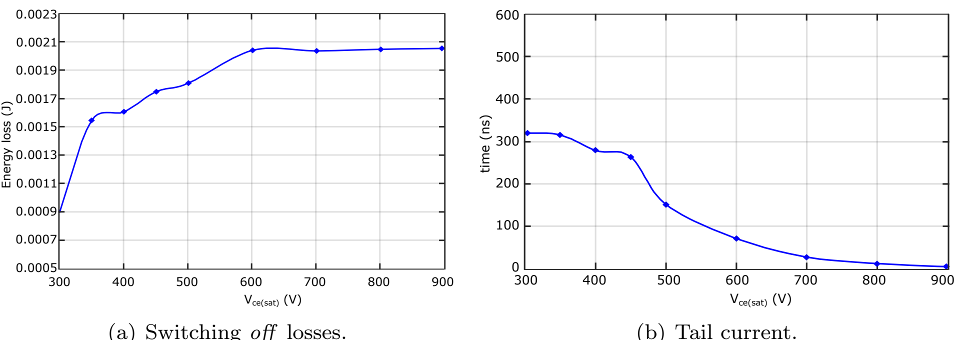
(c) Thermal: in contrast to the PT IGBTs, the NPT presents a positive temperature coefficient. Although this causes the increase in conduction losses, this characteristic simplifies the parallelization of these devices, presenting more stable variations with the temperature. Consequently, a self-regulation of the voltages and currents occurs, thus an IGBT detailed selection is not required, as in the case of PT [184].

In the table 2.1, a comparison of the PT and NPT technologies is shown. This comparative presents the data of the first devices in the market [183]. The comparison shown dates back to 1999, where the voltage ranges of the PT and NPT technologies present the original values.

2.6 *Field Stop* technology: FS IGBT

The investigation of power modules with IGBTs of 6.5 kV for traction applications allowed to develop the key technology to introduce the concept of the IGBTs *Field Stop* (FS) [206]. This technology emerged around 1999 with the aim of reducing the switching losses of the IGBTs. The FS combines some of the advantages inherited from the PT and NPT technologies, offering high blocking voltages and low losses.

The benefits of the previous generations of IGBTs have been based on innovations such as the improvement of the structure through a *buffer* layer and the reduction of the lifetime, as in the case of PT IGBT. They have also been based on a series



(a) Switching *off* losses.

(b) Tail current.

Figure 2.12: FS IGBT behaviour.

of optimizations to reduce the geometry of the devices, as the NPT IGBT. However, both PT and NPT technologies reached their development limit. Although studies on these two architectures are still being carried out, the new advances in the vertical structure of the IGBTs are mainly based on the FS architecture concept.

The FS structure provides a trapezoidal-shaped electric field distribution [207], more desirable than the electric field of other architectures. This provided a much thinner $n^{-}drift$ layer for the same blocking voltage, reducing the size of the device (comparing it with an IGBT NPT). Also, the reduction of the thickness of the wafer directly influences the switching behaviour of the device [208, 209]. The *field stop* and *p* collector layers make possible a fast turn *off* with a low amplitude of current tail, because the device has a low number of carriers in the conduction mode [210].

The are other two technologies, *Light Punch Through* (LPT) and *Soft Punch Trough* (SPT), that represent an evolution of the NPT structure (section 2.5), resulting in technologies equivalent to the FS IGBT. The singularities of the LPT and SPT technologies are only been developed by the manufacturer, Mitsubishi [184] and ABB [195], respectively. The behaviour presented by the devices of the FS architecture is explained below:

(a) Static: the reduction of the total thickness of the device results in the reduction of the *on* resistance, which produces a low forward voltage drop and lower conduction losses than conventional PT and NPT architectures. The reduction of the thickness also diminish the capacity to absorb shortcircuits, but this capacity can be improved by the doping conditions of the layer FS [187].

(b) Dynamic: the FS architecture presents a non-linear behaviour between the switching *off* losses and high voltage breakdown voltage (figure2.12(a)), while

in the NPT devices these losses increase linearly. The FS losses increase much slower than other architectures at high voltage operation. During turn *off*, the behaviour of the FS devices shows a short tail current with low amplitude. At high voltages, this tail current virtually disappears, as the figure 2.12(b) shows [211]. For this reason, due to its fast turn *off* process with low losses, the FS is ideal for applications that require high switching frequencies, where other conventional architectures have unacceptable switching losses. In this sense, there are devices with an optimized design of the FS layer in order to meet the requirements for high frequency.

(c) Thermal: the FS devices inherit the advantages from the NPT devices, presenting a positive temperature coefficient, which simplifies the process of parallelization IGBTs.

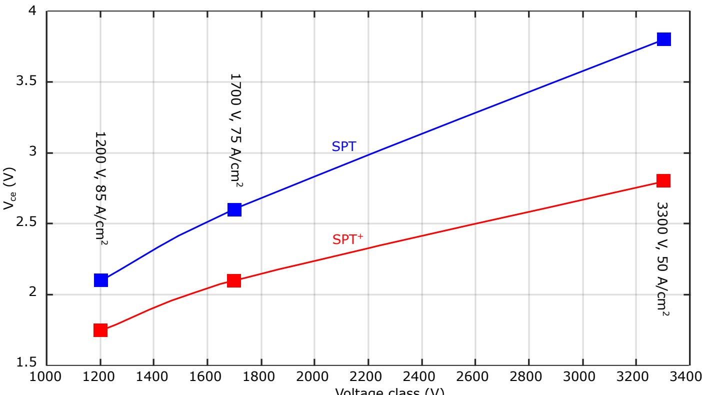
2.7 Enhanced planar technology: SPT$^+$

Nowadays, there is a continuous evolution in the structures and technologies of the IGBTs. In this sense, manufacturers develop variants of the main technologies to get IGBTs with lower power losses, higher switching frequencies, less size of *die*, higher capacity against shortcircuits and positive temperature coefficients.

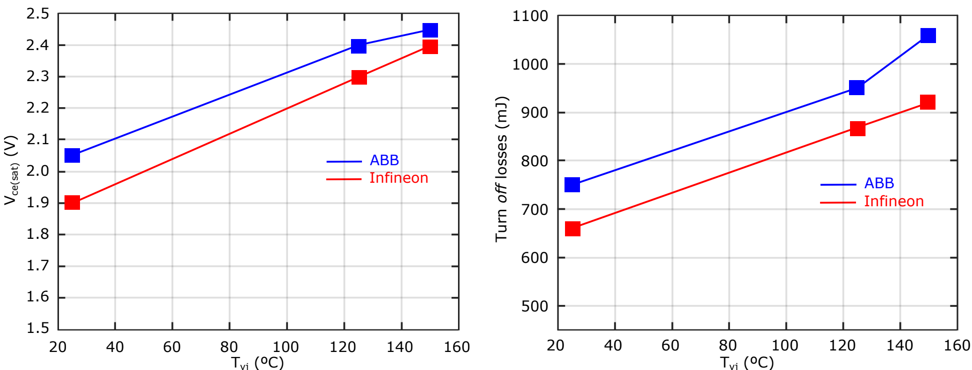
In this context, ABB presents a new enhanced architecture, the SPT^+ structure. This technology improves the standard FS technology, using and advanced planar technology to reduce the forward voltage drop ($V_{ce_{sat}}$) and preserving the robustness of the device [212]. This technology can compete with the Trench FS architecture (section 2.8) developed by Infineon and the enhanced *trench* cell (CSTBT, section 2.9) developed by Mitsubishi and based on LPT technology.

The SPT^+ variants can be seen in the figure 2.5(a). The SPT^+ structure consists of the optimization of the FS technology in order to operate at higher temperatures, for example at 175°C [213], reducing the conduction losses while keeping the levels of switching losses [212]. To do this, the advantages of obtaining an improved layer n (buffer) are combined together with the use of a enhanced layer (advance planar cell). However, the manufacturing process is extremely complicated in order to obtain such improvement of conduction losses without altering the time of the device turn *off* process [212].

The forward voltage drop in the SPT^+ is lower than in the original SPT technology due to the improvements introduced in the structure of the IGBT. The improvement in conduction losses can be seen in the figure 2.13(a). On the other hand, the SPT^+ shows higher $V_{ce_{sat}}$ compared with Trench FS (Infineon, figure 2.13(b)) due to a higher thickness of *n-buffer* [195]. The turn off losses in



(a) Comparative of $V_{ce_{sat}}$ for the SPT and the SPT$^+$ of ABB.



(b) $V_{ce_{sat}}$ of SPT$^+$ (ABB) and Trench FS (Infineon).

(c) Turn *off* losses of SPT$^+$ (ABB) and Trench FS (Infineon).

Figure 2.13: SPT$^+$ technology behaviour.

SPT^+ are higher than Trench FS architectures (figure 2.13(c)) [195]. In general, the SPT$^+$ technology shows a worst performance than Trench FS technology, but they can directly compete in the same applications [195, 212].

2.8 *Trench Field Stop* technology: Trench FS IGBT

The incorporation of a *trench* cell over an architecture *field stop* forms a new topology called *trench field stop*. This architecture has great potential to reduce conduction losses and switching losses [214]. The architecture of this type of IGBTs can be seen in the figure 2.3.

The Trench FS technology was a milestone in the evolution of the IGBTs when it appeared around the year 2000. The first development came from Infineon, although other manufacturers also used this concept in the following years. The interaction of the FS layer, which allows the reduction of the thickness of the device for the same voltage range and the use of a *trench* gate, which distributes the density of the charge of carriers in a homogeneous way on the silicon, has allowed the improvement of IGBTs devices [184]. The main features of the combination of the FS and *trench* cell architectures are:

(a) Static: the *trench* cell produces a reduction of the conduction losses thanks to the increase of carriers near the emitter (cathode) [215]. Moreover, it introduces the possibility of reducing the thickness of the substrate, close to 30 % [216] thanks to the concept *trench field stop*, allows the conduction losses to be drastically reduced for the same breakvoltage. For example, a device with a planar cell layout and a concept similar to *field stop* gate can have a 30 % more conduction losses without using a *trench* [216]. Compared to the first generation of PT IGBTs, there is a 65 % [216] reduction in conduction losses, while with the second generation of IGBTs have a 35 % of losses reduction [216].

(b) Dynamic: the introduction of the concept *field stop* reduces the losses of the turn *off* process by implementing an additional n doped layer on the back of the wafer. However, the charge stored in the device must be reduced through the optimization and control of wafer thickness, specially the FS layer and the p emitter. Therefore, the losses are lower than in a NPT device, which causes the reduction of the switching losses of the device. For medium power applications, these IGBTs have been optimized so that their switching losses are similar to those that occur in low power.

(c) Thermal: the architecture Trench FS has a positive temperature coefficient, inherited from the NPT devices, which facilitates the parallelization.

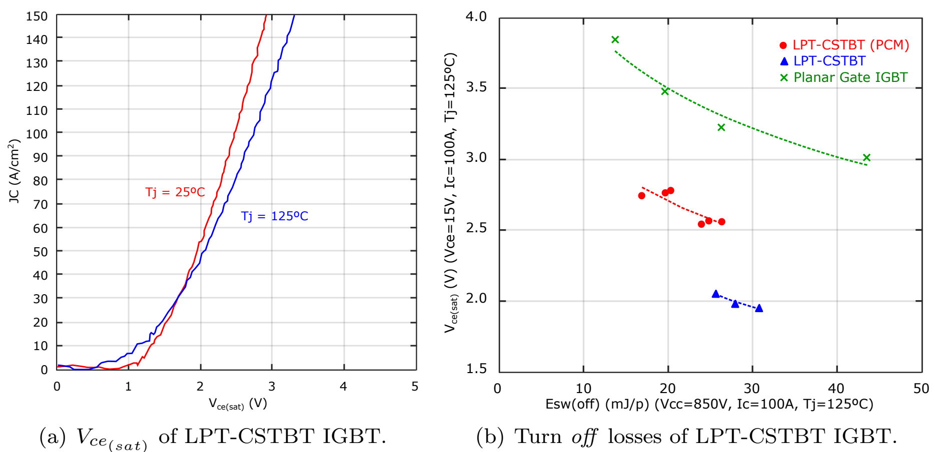
Finally, the substrate has a higher resistivity than a NPT due to the FS layer, but thanks to the technology of the device terminals, it is able to withstand high current densities and a greater charge on the substrate during the shortcircuit that can cause the destruction of the device. Therefore, it can be said that the Trench FS presents a great robustness. In this sense, if the *field stop* layer is optimized, it can support up to 40 % [216] more current density than NPT devices.

2.9 Enhanced Trench FS technology: CSTBT^{TM}

Another variant of IGBT *trench* architecture, developed by Mitsubishi Electric, is the *Carrier Stored Trench Gate Bipolar Transistor* (CSTBT). This technology is an evolution of the *trench* technology where the advanced planar cell structure is implemented, trying to solve some problems of the conventional *trench* devices such as the high cell density that causes shortcircuits and the high value of input capacity.

The CSTBT uses the Mitsubishi structure *Light Punch Trough* (LPT), which pursues an optimization of the region *n-drift*, providing a low voltage $V_{ce_{sat}}$ while maintaining the switching robustness. The buffer layer is used to ensure sufficient breakdown voltage and low leakage currents [217].

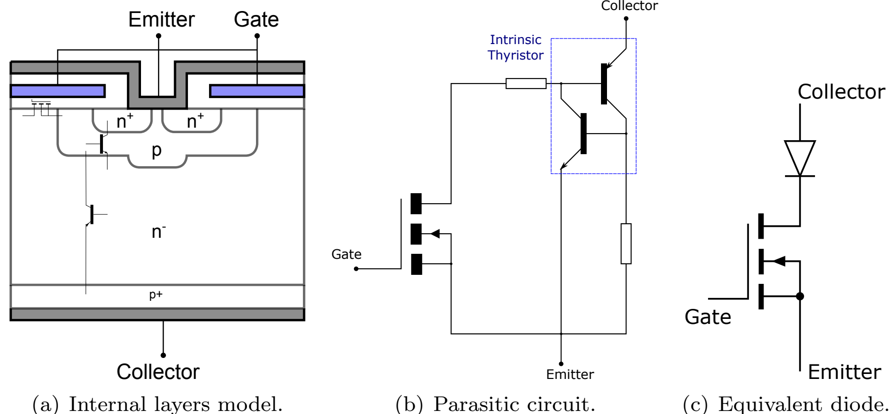
This IGBT has a specific layer (figure 2.5(b)), known as *Carrier Stored* (CS) [218], to increase the density of the charge carrier near the emitter [184]. This combination of *trench*, carrier stored layer and LPT substrate reduce the forward voltage drop (figure 2.14(a)), being compared with the traditional IGBTs (for example, PT technology). The LPT vertical structure is similar to the FS technology, eliminating the epitaxial wafer material and providing a positive temperature coefficient, which simplifies the parallelization operation [217, 219].



(a) $V_{ce_{(sat)}}$ of LPT-CSTBT IGBT. (b) Turn *off* losses of LPT-CSTBT IGBT.

Figure 2.14: Comparative of CSTBT IGBTs with planar PT IGBTs.

As far as the switching losses are concerned, the improvement of the turn *off* process is achieved by using a smaller area of silicon (controlling the carrier lifetime



(a) Internal layers model. (b) Parasitic circuit. (c) Equivalent diode.

Figure 2.15: IGBT intrinsic diode.

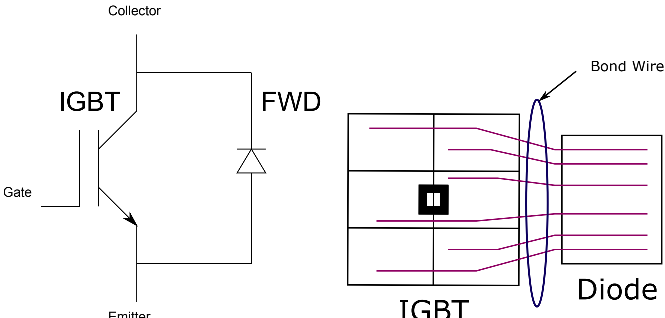
with the buffer layer). An LPT-CSTBT cell achieves a better behaviour (improvement of a 25 %) with respect to the turn *off* losses (figure 2.14(b) [217, 220]), but diminishing the area entails reducing the capacity to withstand shortcircuits [219]. One of the detrimental effects of the adjustment of the lifetime is the increase of the forward voltage drop, which causes an increase in conduction losses [221].

Mistsubishi's CSTBT technology continues to evolve, emerging new generations of devices. Their evolution technique consists of improving the CS layer and the structures *trench* of the device to obtain better behaviours of the power losses [222].

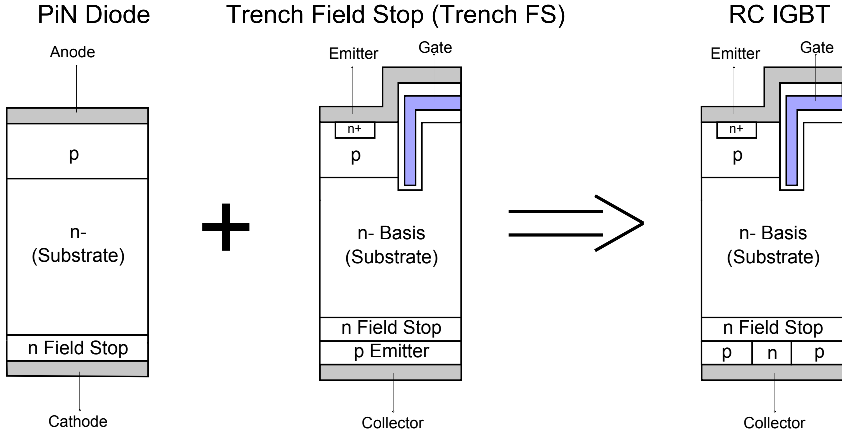
2.10 IGBT with antiparallel diode: RC IGBT

IGBTs, especially in applications with inductive load, require a diode in antiparallel to the IGBT, which is called *freewheeling* (FWD). Moreover, the internal structure of IGBT also presents a parasitic diode. Thus, the differentiation of the diode placed in antiparallel with the intrinsic diode is fundamental.

(a) Intrinsic diode: in the process of manufacturing the IGBTs, where the gate behaviour of a MOSFET is combined with the conduction behaviour of a bipolar transistor, an intrinsic diode is formed. The IGBT presents a structure similar to a MOSFET with an additional area p^+ of a high doping in the collector area. The figure 2.15(a) shows the layers of an IGBT with its intrinsic devices that are formed between the junctions of layers. The equivalent circuit of the intrinsic components appears in the figure 2.15(b), where



(a) IGBT circuit and FWD diode. (b) Junction of IGBT and diode.



(c) Combination of the IGBT with the FWD diode.

Figure 2.16: RC IGBT structure and external FWD diode.

the structure of an internal parasite thyristor [184] is observed.

The equivalent circuit (figure 2.15(b)) can be simplified to a MOSFET and an intrinsic diode (figure 2.15(c)). The losses that occur in the IGBT, mainly, depend on the quality of this intrinsic diode.

(b) Antiparallel diode (FWD): for certain applications, especially in inverters, the IGBTs are accompanied by an antiparallel diode that protects the IGBT and allows the circulation of the reverse current to the IGBT. The circuit formed by these two devices can be seen in the figure 2.16(a), the process of joining both devices can be done by several techniques, according to the manufacturer's technology, some of them are: *chip soldering*, *system solder-*

Table 2.2: Size of chip and thermal impedance.

Chip type	IGBT/FWD (total)	RC-IGBT
Active area(1)	0.64/0.36 (1.00)	1.00
Chip size(1)	0.62/0.38 (1.00)	0.91
Thermal resistance(2)	0.24/0.40	0.15/0.15(3)

Table notes:
(1) arbitrary unit (a. u.).
(2) $R_{th(jc)}$ of conventional package (K/W).
(3) IGBT operation / FWD operation.

ing, *ultrasonic bonding* (figure 2.16(b)), etc [184]. Therefore, the FWD is an additional and independent element to the IGBT itself.

The *recovery conducting* IGBT (RC IGBT[1]) device implements the two semiconductors (IGBT and FWD diode) seen in the figure 2.16(a) [184] on the same silicon wafer, not being a simple connection between two independent semiconductors.

The RC IGBT is a device based on Trench FS technology. The figure 2.16(c) shows [184] an example of a combination of Trench FS IGBT with a diode to obtain an IGBT RC device.

In order to integrate the antiparallel diode into the IGBT structure and achieve a RC IGBT device, the anode p of the diode is divided into several sections and the cathode n is integrated into the emitter of the IGBT. Additional processes should be used to control the lifetimes and ion photo-implantation [223]. In this way, the antiparallel diode uses the same silicon as the IGBT [224]. On the one hand, the use of extra silicon is not necessary but, on the other hand, the diode can not be optimized independently of the IGBT, so that the diode presents a worst behaviour.

Some manufacturers assemble this new RC IGBT device on a compact package to reduce the thermal impedance compared to a conventional assembly. This allows to increase the semiconductor reliability [223]. The table 2.2 [223] shows the advantages of RC IGBT technology in terms of integration and thermal resistance, compared to a conventional assembly where a separate IGBT and FWD diode are available and linked together by some technique. These data show the advantages of this new integration technology where the device can conduct the same current densities at a lower temperature.

In addition to the losses, it is equally important to pay attention to the type of

[1]Many manufacturers offer the IGBT RC technology but with different nomenclatures. For example, ABB builds *Bi-mode Insulated Gate Transistor* (BIGT), Infineon has the variant for resonant RC IGBT applications and for *hard switching* RC-D IGBT, and Mitsubishi uses the name RC IGBT to refer to this technology [184].

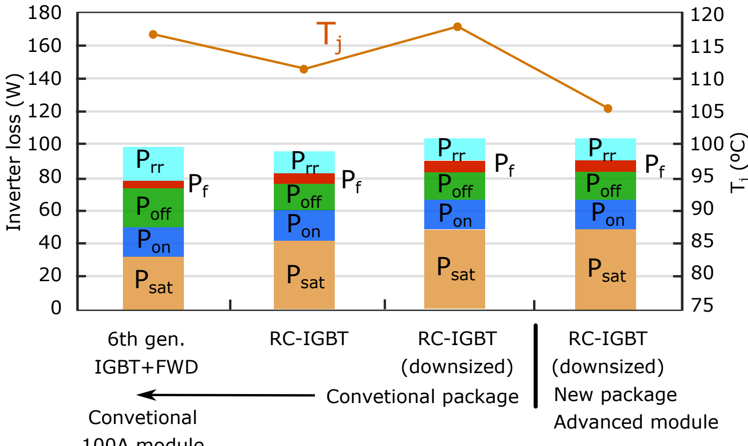


Figure 2.17: Losses of the RC IGBT and the IGBT + FWD assembly of an inverter.

encapsulation of the device. In this sense, the figure 2.17 [223] shows the junction temperature in the IGBT next to its FWD, in the RC IGBT using conventional package and in the RC IGBT using optimized encapsulations. As it can be seen, although the losses in the device are of the same order of magnitude, the temperature of the joint is considerably lower in the case of the RC IGBT with advanced encapsulation. This means that the RC IGBT (which is a chip 7 % smaller than the architecture composed of IGBT + FWD diode) can support a current density 35 % higher than an IGBT + FWD assembled and encapsulated conventionally [223].

2.11 Conclusions

The IGBT study, made in this chapter, provides a vision of the device technological evolution of this semiconductor, the main material properties and the internal device architectures. After these analyses, the IGBT can be said to be clearly the *Si* semiconductor that meets better the power train automotive requirements (chapter 1) such as application voltage, nominal and maximum currents, switching frequencies, nominal operation and others.

According to the internal IGBT structure, the device can be divided in two parts, the emitter side or IGBT cell and the collector side or IGBT vertical structure. In the IGBT cell, there are two main technologies in order to improve the emitter carrier conductivity: planar and trench structures. In the IGBT vertical structure, three main technologies are identified: PT (epitaxial wafer), NPT (FZ wafer) and FS (FZ wafer).

Both the PT and NPT IGBTs were the initial developments and they used a planar cell architecture. The PT IGBTs presents better conduction and switching losses than NPT devices. However, they only were used initially for the voltage range of 600-1200 V. In the case of he NPT device, they were used in voltage range of 1200-1700 V and they are easier to manufacturer than PT. Moreover, NPT devices show a negative coefficient with the temperature, instead of the positive and negative coefficient of the PT devices.

A relevant improvement in IGBT evolution was the combination of both PT and NPT structures, generating the FS architecture (planar cell). This development takes the advantages of both previous devices. Specifically, FS device improves the conduction and switching losses of NPT due to the usage of the PT buffer layer concept and they also present a negative coefficient of temperature, an important characteristic for the semiconductor parallelization. Moreover, other FS-based developments with some internal enhances were developed as SPT^{+}.

The next step of IGBT evolution was the implementation of trench cell over the planar cell devices. As it is mentioned, the FS topology presents the best behaviours among the main vertical structures, so that the major trench cell implementations were realised on the FS structure, generating the Trench FS IGBT or other similar variants as the CSTBT.

Nowadays, the most modern developments are based on Trench FS, using advanced planar and trench concepts, in addition to integrate new functionalities as *freewheeling* diodes. The evolution of the IGBT technology is focused on the power loss reduction and thermal behaviour improvement in order to take the full advantages of *Si* qualities. These developments mean that the *Si* IGBT is a technology where better static, dynamic and thermal behaviours are possible to find in the next years, but no substantial improvements.

The manufactures continue trusting and betting on *Si* IGBT technology, because the *Si* represents the alternative with the greatest maturity and proven technology, but the material presents some limitations such thermal conductivity and switching frequencies whose overcoming is difficult. In this context, the WBG technology appears as an interesting future option for HEV/EV applications.

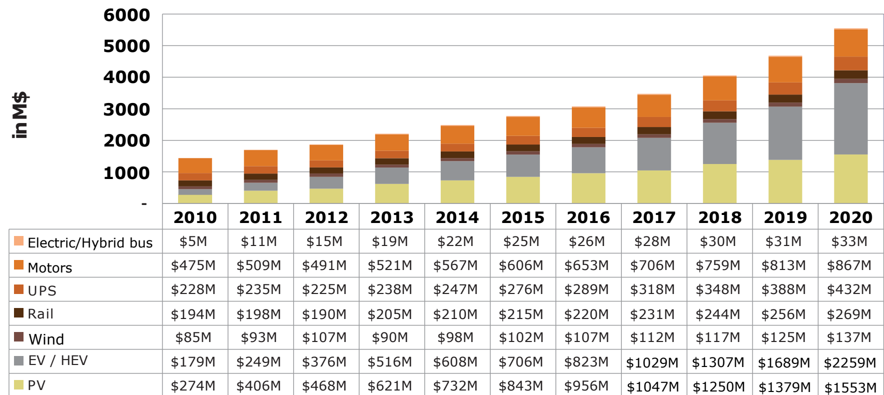
Chapter 3

Wide bandgap (WBG) technology

3.1 Introduction

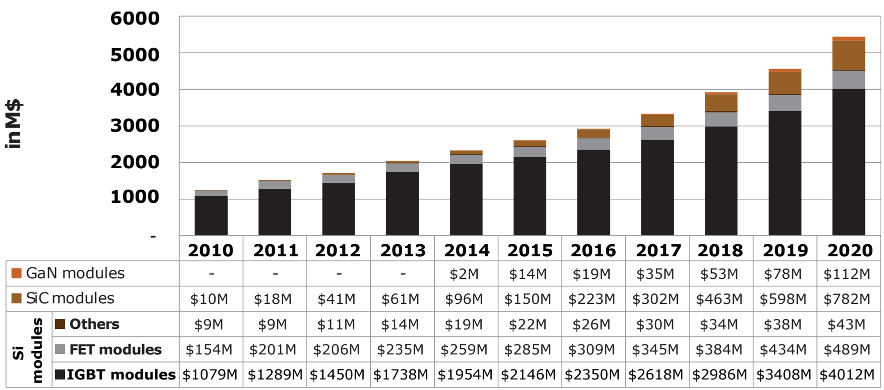
Over the years, an evolution on the silicon (*Si*) devices has been achieved through the appearance of new IGBT architectures, starting from the first architectures such as PT or NPT until the more complex architectures such as Trench FS or CSTBT. The emergence of a new generation of power devices, named *wide bandgap* (WBG), is improving the performance of power converters based on semiconductors of traditional materials (*Si*). Moreover, this demand of power applications is continuously increasing, being the automotive market (HEV/EV) the fastest growing sector (figure 3.1(a) [225]).

With the development of new power applications, the WBG semiconductors are gaining popularity and higher implementation levels, as figure 3.1(b) [225] shows. The introduction of WBG materials in the growing HEV/EV market is assuming an strong impulse of these materials in power electronics. Silicon Carbide (*SiC*) and Gallium Nitride (*GaN*) devices are considered the most matured technologies, although other semiconductor materials such as Diamond and Gallium Oxide (Ga_2O_3) exhibit a high potential, and are currently under investigation in many laboratories [226, 227]. These new materials solve some well known *Si* limitations concerning blocking voltage, operating temperature and switching frequency, which are related with the main physical parameters involved in power device design: critical electric field, bandgap energy, charge carriers saturation



	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Electric/Hybrid bus	$5M	$11M	$15M	$19M	$22M	$25M	$26M	$28M	$30M	$31M	$33M
Motors	$475M	$509M	$491M	$521M	$567M	$606M	$653M	$706M	$759M	$813M	$867M
UPS	$228M	$235M	$225M	$238M	$247M	$276M	$289M	$318M	$348M	$388M	$432M
Rail	$194M	$198M	$190M	$205M	$210M	$215M	$220M	$231M	$244M	$256M	$269M
Wind	$85M	$93M	$107M	$90M	$98M	$102M	$107M	$112M	$117M	$125M	$137M
EV / HEV	$179M	$249M	$376M	$516M	$608M	$706M	$823M	$1029M	$1307M	$1689M	$2259M
PV	$274M	$406M	$468M	$621M	$732M	$843M	$956M	$1047M	$1250M	$1379M	$1553M

(a) Power modules market, split by application.



		2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
GaN modules		-	-	-	-	$2M	$14M	$19M	$35M	$53M	$78M	$112M
SiC modules		$10M	$18M	$41M	$61M	$96M	$150M	$223M	$302M	$463M	$598M	$782M
Si modules	**Others**	$9M	$9M	$11M	$14M	$19M	$22M	$26M	$30M	$34M	$38M	$43M
	FET modules	$154M	$201M	$206M	$235M	$259M	$285M	$309M	$345M	$384M	$434M	$489M
	IGBT modules	$1079M	$1289M	$1450M	$1738M	$1954M	$2146M	$2350M	$2618M	$2986M	$3408M	$4012M

(b) Power modules market, split by technology.

Figure 3.1: Market trend in WBG technology.

velocity and thermal conductivity [30, 142, 143, 228–233]. Concerning these parameters, figure 3.2 compares the *SiC* and *GaN* potential regarding blocking voltage, switching speed and high temperature operation, when compared to *Si*. Figure 3.2 includes Diamond's parameters, which is considered the ultimate semiconductor material. It is also worth to remark that, from a technical point of view, packaging aspects could limit the maximum ranges achievable by the semiconductor device itself as, for example, specific packaging solutions allow *SiC* devices to operate in the -150°C to +300°C range [234]. On the other hand, the design complexity of WBG technology increases, because it introduces new technical challenges that were less relevant in *Si* technology. The circuit parasitic capacitances [162] and inductances [161] become more critical, as higher switching speeds and faster turn *on*/*off* transients generate interferences and oscillations that are source of EMI [146, 235], producing higher harmonic con-

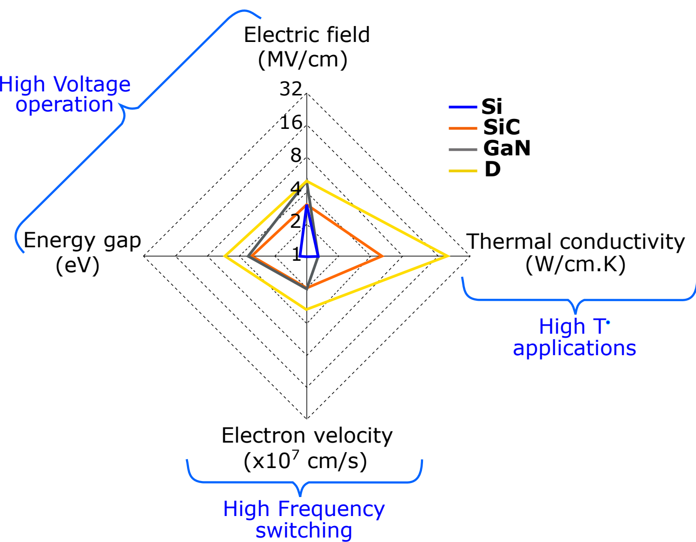


Figure 3.2: Current status of potential *wide bandgap* materials.

tent [168], cross-talk effects [236] and interaction between the converter and the load [237].

Today, there is no quality *GaN* substrate that can achieve the material expectations, being necessary a higher development. The present *GaN* technology is focusing on high frequency applications of medium voltage, being its thermal conductivity (similar to *Si* material) an important drawback for some power applications. For all this, *SiC* is considered the best option to replace *Si* in the short time due to its properties and commercial maturity, because the substrates are of such high quality that many companies are offering wafers and epitaxias[1] of 100 mm diameter [238].

This chapter is particularly focused on the state of the technology of the *wide bandgap* devices (figure 3.3), specifically the *SiC* and *GaN* devices that are in a higher degree of maturity. For this reason, the device main properties such as internal structure characteristic parameters, voltage and current levels are analysed and focused on meeting the application requirements, specifying what *SiC* and *GaN* semiconductors are more relevant for their implementation in HEV/EV applications.

[1]Also called epitaxial growth, it is one of the processes in semiconductor manufacturing. Epitaxy refers to the deposition of a crystalline overcoat on a crystalline substrate.

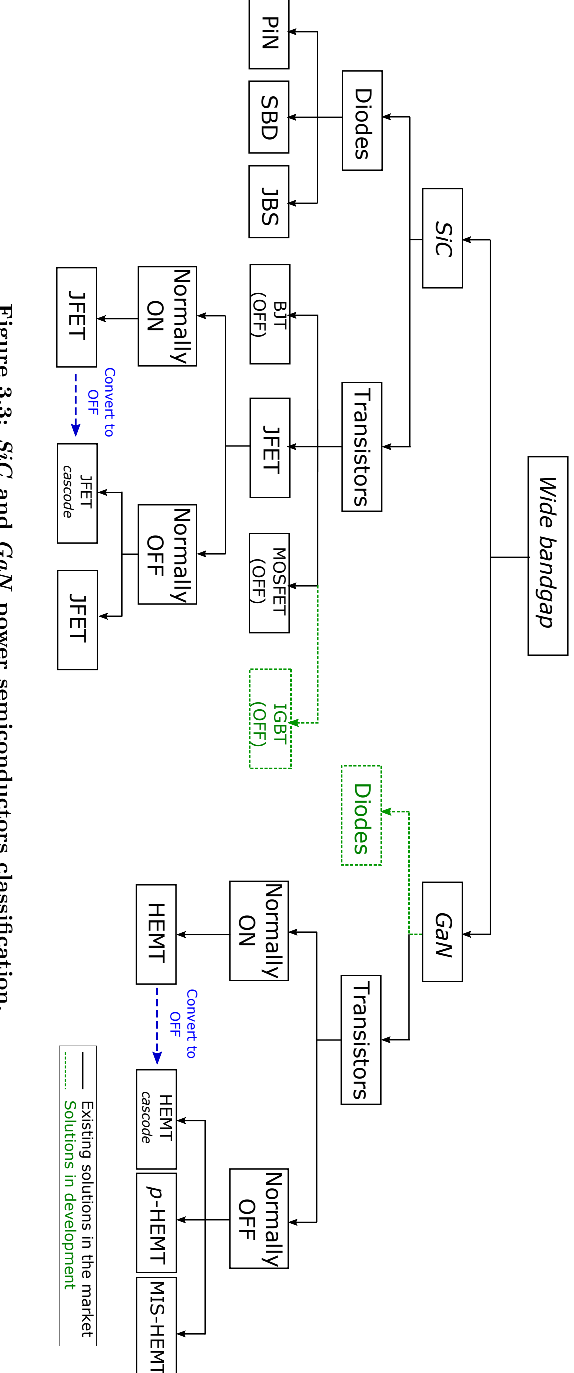


Figure 3.3: ***SiC* and *GaN* power semiconductors classification.**

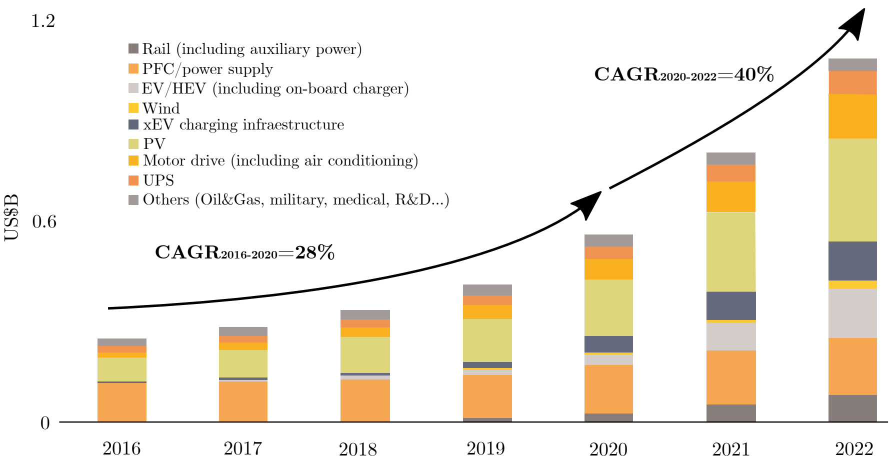


Figure 3.4: Current *SiC* market status and future prospects.

3.2 Silicon Carbide (*SiC*) devices

During the last few years, Silicon Carbide (*SiC*) has gone from being a promising technology to being an alternative to silicon (*Si*) technology in power electronics applications. Although the *Si* devices dominate the market, the situation is changing, being *SiC* an alternative for the improvement of power converters [30, 229]. The reasons that encourage the incorporation of *SiC* technology in power electronics applications with respect to *Si* devices are:

- Higher voltage ranges.
- Lower forward voltage drops.
- Higher maximum temperatures.
- Higher thermal conductivity.

Thus, they constitute a solution for medium-high voltage/medium-high power applications, since *SiC* physical material parameters allow the construction of smaller chips with lower device parasitic capacitances and fast switching speed capabilities [28]. The power electronics industry also promotes the introduction of this new technology, as it can be confirmed from the available market data and future prospects (figure 3.4 [239]), apart from many *SiC* developments by semiconductor manufacturers [29].

The currently available *SiC* technologies are presented and analysed (figure 3.3), selecting the best possible option to be applied in HEV/EV appliations. The main internal structures of the *SiC* devices is presented in the figure 3.5. Aside from

their internal structures, the figures 3.6 and 3.7[1] show their voltage and current levels, while figures 3.8, 3.9, 3.10, 3.11 and 3.12 identify the most significant parameters of a portfolio of current *SiC* devices for power modules. In this comparative study, almost all the analysed devices are encapsulated in TO-247 or D3PACK packages, with similar junction-to-case thermal resistance values. Based on the chosen parameters, the charts provide the performance of the devices and the scope of their parameters, which can be summarized as follows:

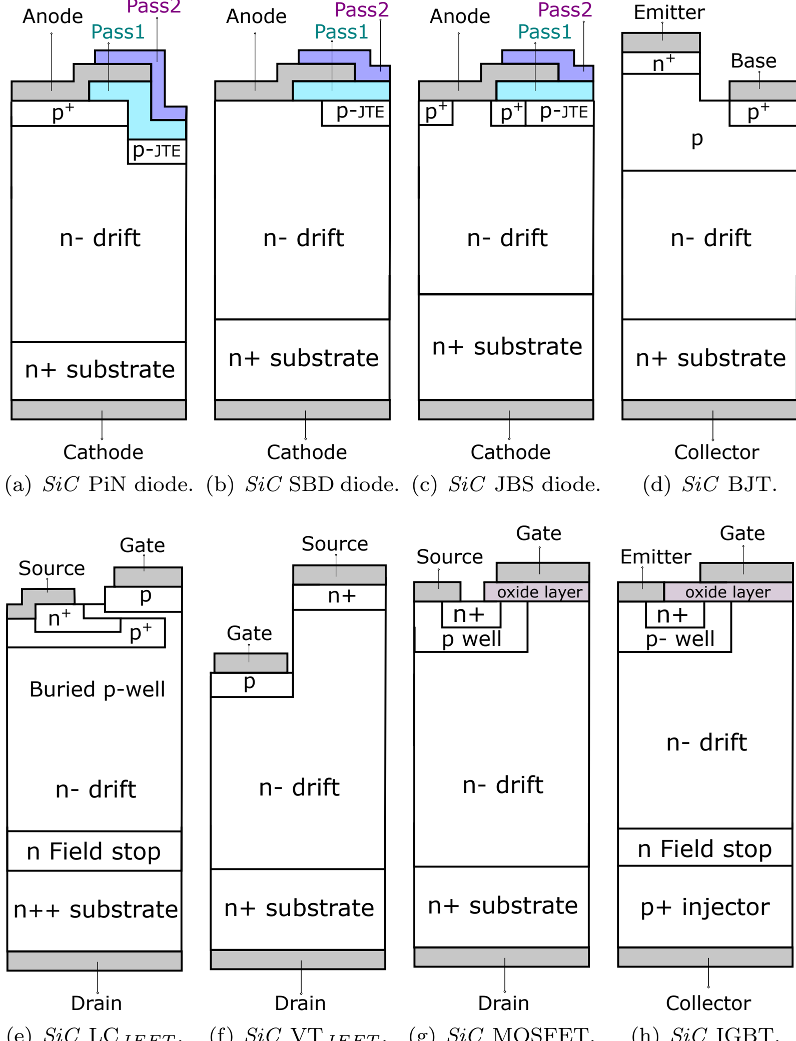
- V_{block} (V), maximum blocking voltage of the power device during the *off* state. This parameter refers to $V_{DS_{max}}$ (maximum repetitive drain to source voltage) for MOSFETs, JFETs and BJTs, and V_{RRM} (maximum repetitive reverse voltage) for diodes. This voltage must be higher than the maximum HEV/EV battery voltage, including a given security margin (typically a 1.5x or 2x factor) due to voltage peaks produced across the devices during commutations.

- I_{max} (A), maximum current of the semiconductor during the conduction state. This parameter refers to I_D (continuous *on*-state DC drain current), provided by manufacturers for MOSFETs, JFETs and BJTs, and I_S/I_F for diodes. This parameter and the total current per phase of the power converter will define the number of power semiconductor devices to be paralleled for each switch of the inverter. Mainly, I_{max} is thermally limited, and it depends on the junction-to-case thermal resistance of the device.

- T_{jmax} (^{0}C), maximum operation junction temperature. This parameter determines the maximum allowable junction temperature of the device, and it is determined from manufacturers reliability data. Exceeding this temperature seriously decreases the device lifetime [182]. The power module must be electrically and thermally designed in such a way that the maximum application temperature is lower than T_{jmax} and T_{vop} (which is maximum temperature under switching conditions of the semiconductor).

- R_{dson} ($m\Omega$), drain to source *on*-state resistance. This parameter refers to the R_{DSon} indicated by manufacturers for unipolar devices: MOSFETs and JFETs. Some BJT manufacturers neglect the collector-to-emitter offset voltage drop and provide also an equivalent R_{DSon} value as a main conduction parameter. This parameter, together with the instantaneous conduction current, defines the power conduction losses of the device. Tar-

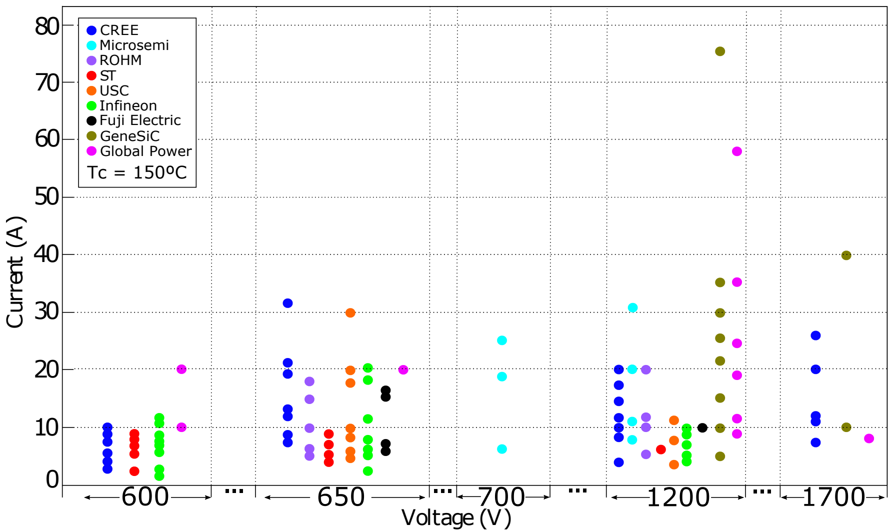
[1] The present work only considers discrete semiconductors, and lefts aside bare dies, because manufacturers do not provide homogeneous specifications for the later. Consequently, a comparison of their parameters requires complex post-processing of the supplied data. Besides, discrete semiconductors are usually made of bare dies. Thus, the provided comparison would be enough for generic frameworks.



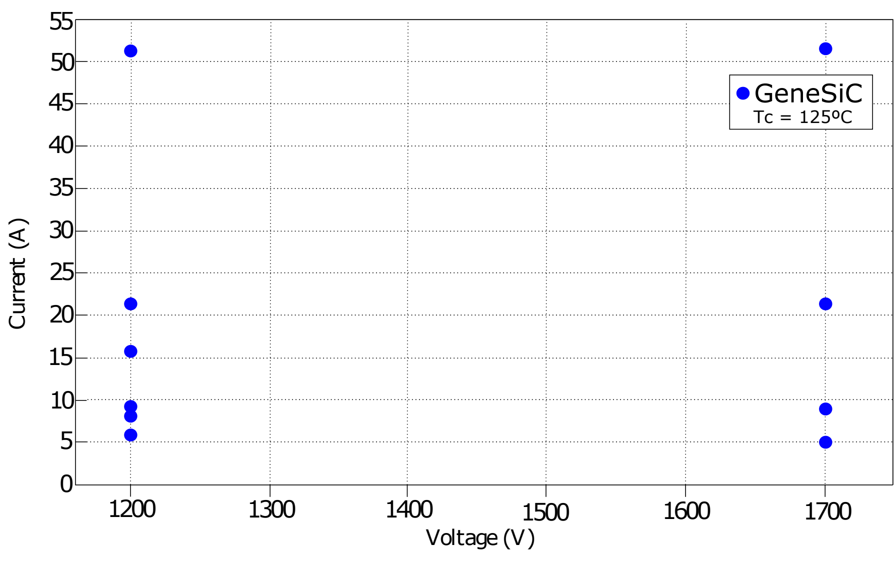
(a) *SiC* PiN diode. (b) *SiC* SBD diode. (c) *SiC* JBS diode. (d) *SiC* BJT.

(e) *SiC* LC_{JFET}. (f) *SiC* VT_{JFET}. (g) *SiC* MOSFET. (h) *SiC* IGBT.

Figure 3.5: Internal structure of *SiC* devices.

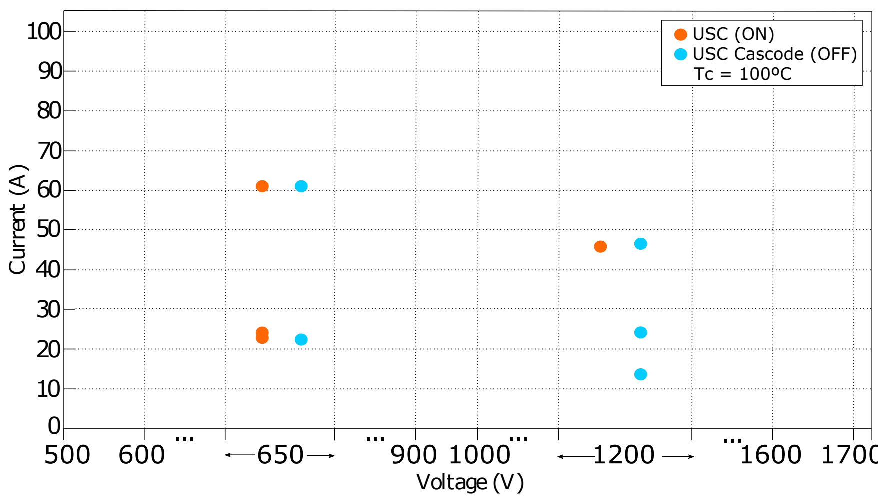


(a) *SiC* diodes voltage and current ranges.

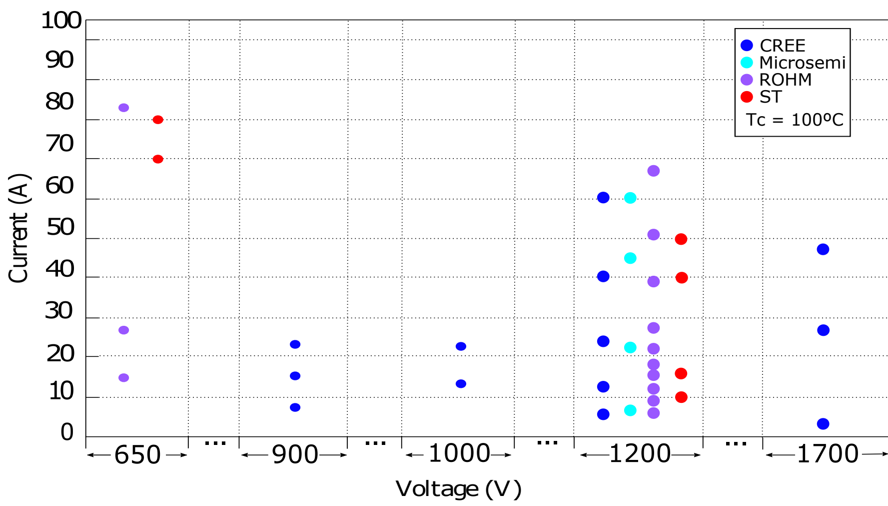


(b) *SiC* BJTs voltage and current ranges.

Figure 3.6: Voltage and current ratings of *SiC* devices available on the market (I).

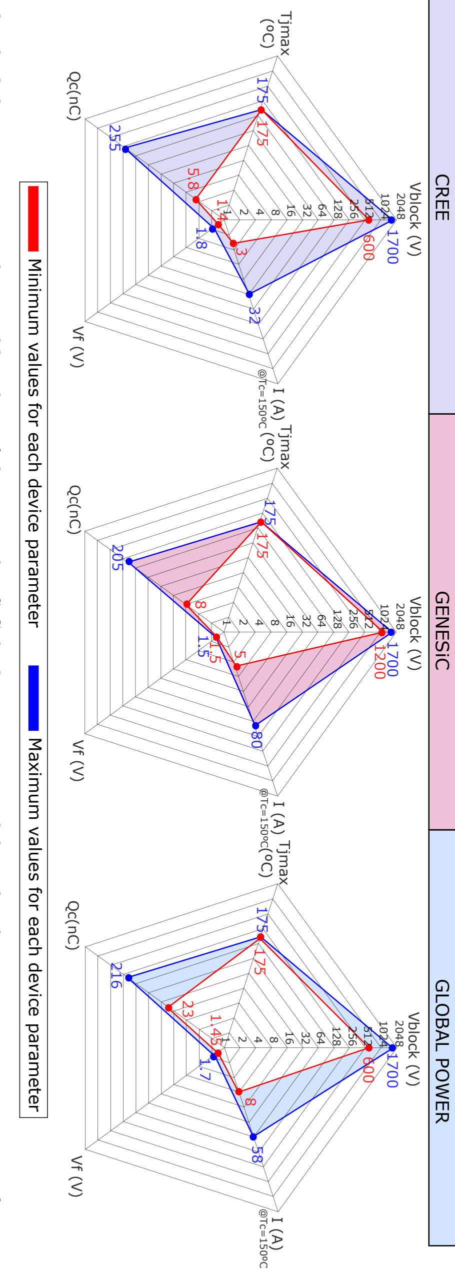


(a) *SiC* JFETs voltage and current ranges.



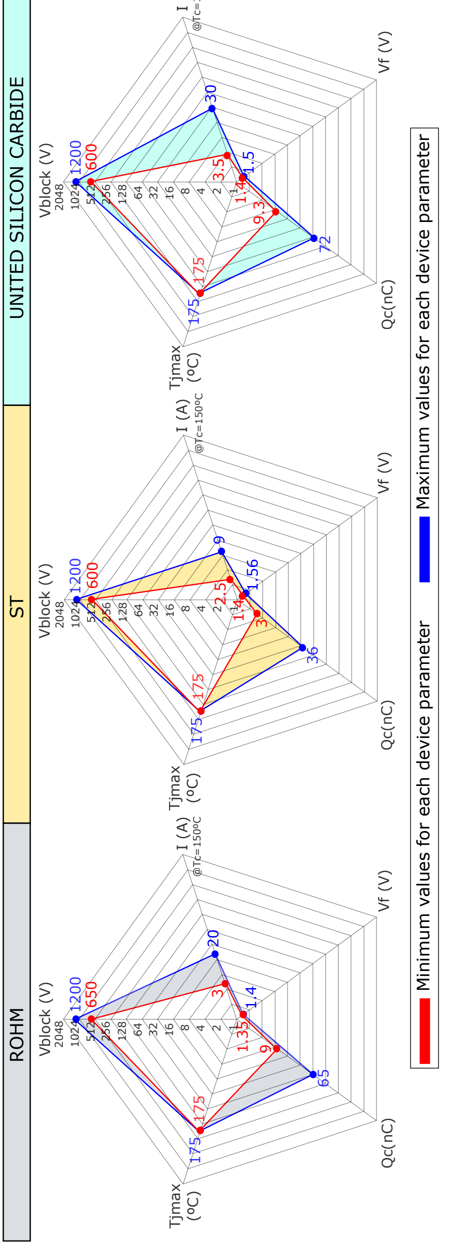
(b) *SiC* MOSFETs voltage and current ranges.

Figure 3.7: Voltage and current ratings of *SiC* devices available on the market (II).



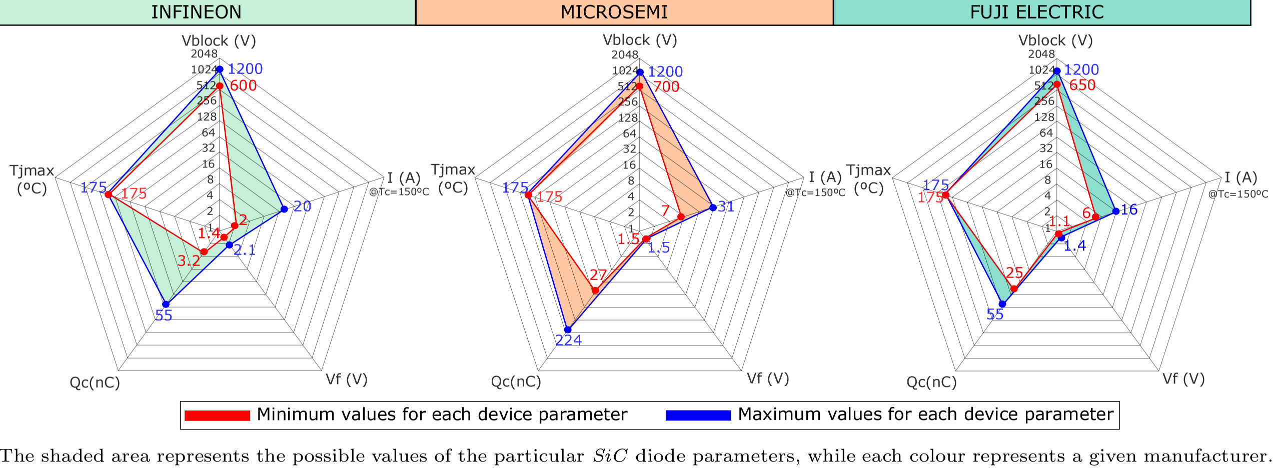
(*)The shaded area represents the possible values of the particular *SiC* diode parameters, while each colour represents a given manufacturer.

Figure 3.8: Maximum and minimum values of the most significant parameters of *SiC* diodes (I).



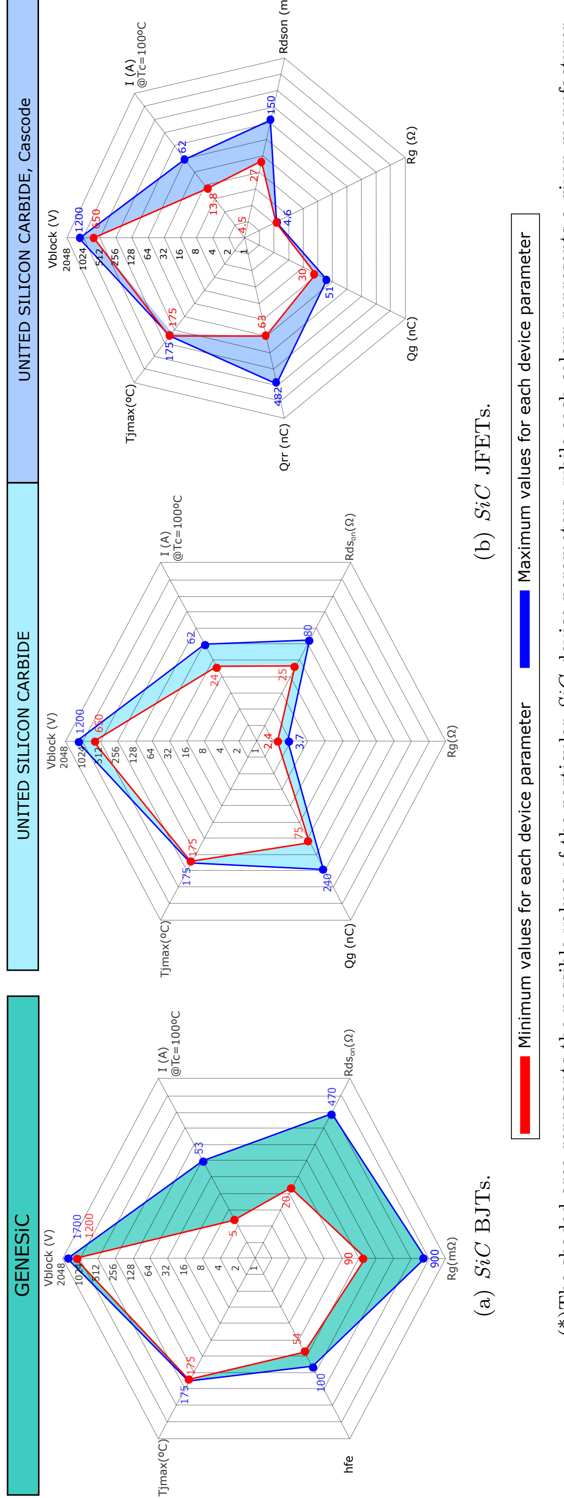
(*)The shaded area represents the possible values of the particular SiC diode parameters, while each colour represents a given manufacturer.

Figure 3.9: Maximum and minimum values of the most significant parameters of SiC diodes (II).



(*)The shaded area represents the possible values of the particular SiC diode parameters, while each colour represents a given manufacturer.

Figure 3.10: Maximum and minimum values of the most significant parameters of SiC diodes (III).

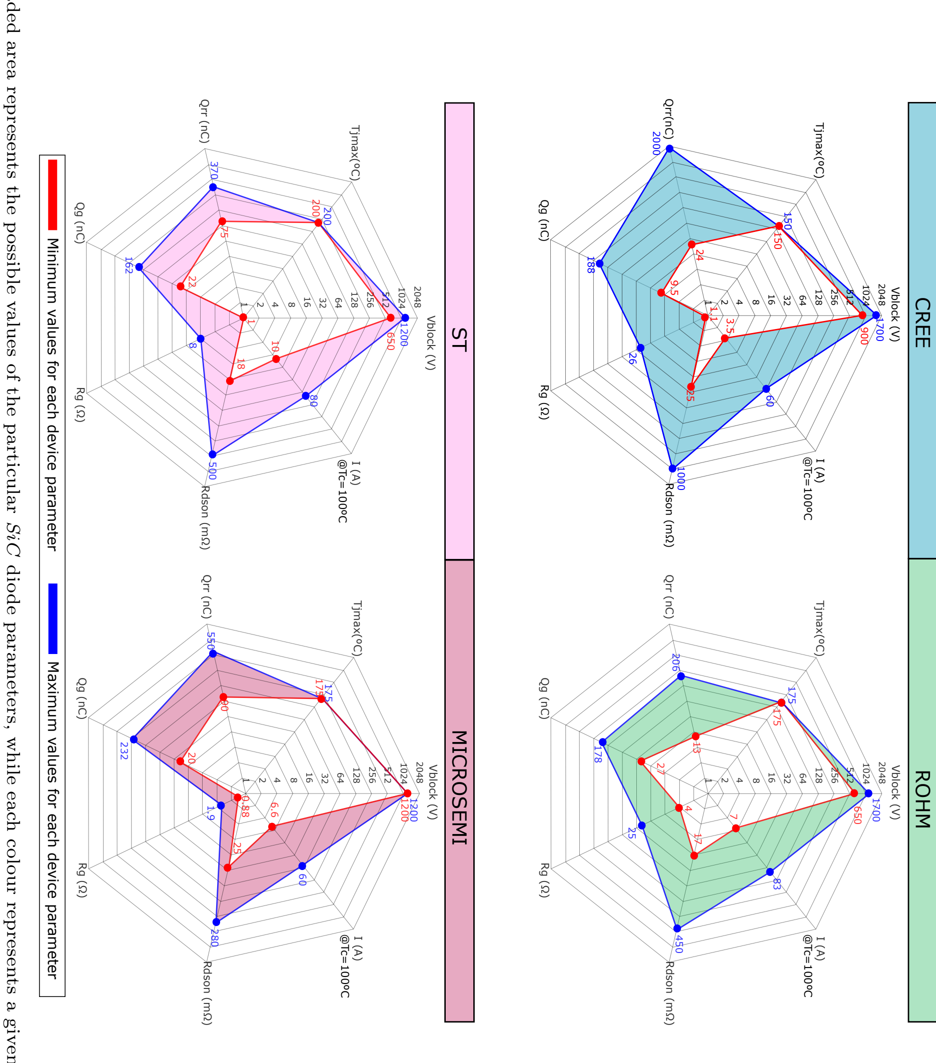


(a) SiC BJTs.

(b) SiC JFETs.

(*)The shaded area represents the possible values of the particular SiC device parameters, while each colour represents a given manufacturer.

Figure 3.11: Maximum and minimum values of the most significant parameters of SiC BJTs and JFETs.



(*)The shaded area represents the possible values of the particular *SiC* diode parameters, while each colour represents a given manufacturer.

Figure 3.12: Maximum and minimum values of the most significant parameters of *SiC* MOSFETs.

geting a balanced current distribution per each semiconductor in parallel, the thermal coefficient of R_{DSon} must be positive.

- R_g (Ω), internal gate resistance. The manufacturers of MOSFETs, JFETs and BJTs provide this parameter as $R_{g_{int}}$. It depends on the semiconductor size, where a higher size is equivalent to a higher resistance value. For the same current, the *SiC* semiconductor area is smaller than for *Si*. On the other hand, gate devices must have a minimum gate resistance value to avoid their destruction, so an external resistance ($R_{g_{ext}}$) is commonly included in order to solve this problem. Both resistances $R_{g_{int}}$ and $R_{g_{ext}}$ have direct influence in other parameters such as in the switching speed and the switching losses.

- V_f (V), the forward voltage drop. This parameter applies to diodes and bipolar devices. It is provided in datasheets at fixed current and temperature values, as it strongly depends on both variables.

- Q_g (nC), total gate charge. This parameter specifies the charge stored in the parasitic input capacitances between gate and source terminals, and it affects to the dynamic behaviour of the device. Moreover, this parameter determines design aspects of the driver, as it must provide enough power for switching (3.1). For *SiC* devices, Q_g does not depend on temperature. Thus, this technology is more stable than *Si* during switching.

$$P_{g_{drv}} = Q_g \Delta f_{sw} V_{drv^{on}_{off}}. \tag{3.1}$$

- Q_{rr} (nC), reverse recovery charge of a diode (total stored charge). This is the charge level required to complete the semiconductor turn *off* process. The parameter refers to Q_{rr} for bipolar junctions such as the MOSFET body diode and Q_c for Schottky (unipolar) diodes. This charge causes a current overshoot in the turn *on* transition of the complementary transistor of the inverter, producing additional power losses.

3.2.1 *SiC* diodes

Nowadays, the main applications of the *SiC* diodes are the power factor correction circuits (PFC), power sources and photovoltaic inverters (PV) [240]. Their main advantages when compared with their *Si* counterparts are their low reverse recovery charge (Q_{rr}, figure 3.13) and low recovery current (I_{rr}), which produce lower switching power losses [240, 241]. In addition, *SiC* diodes also show a positive conduction thermal coefficient [30, 240, 242], which is critical for device parallelization to increase current capacity of power modules (also an important

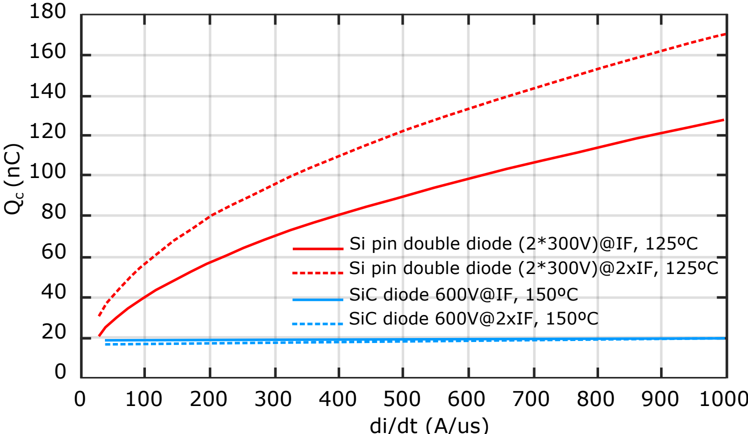


Figure 3.13: Charge comparative of *Si* and *SiC* diodes.

requirement for HEV/EV applications). Additionally, when comparing *Si* and *SiC* diodes of the same size and thickness, blocking voltages are 10 times higher for *SiC* diodes.

Current *SiC* diodes can be classified into three groups [28, 30, 243, 244]:

(a) PiN diodes (figure 3.5(a)): These bipolar devices are designed for high voltage operation, typically above 3.3 kV. They exhibit a low voltage drop during *on* state when compared to *Si* for such breakdown voltages, with a very small forward voltage drop (V_f). However, they have a higher Q_{rr} than unipolar diodes, so their use in HEV/EV applications would decrease system efficiency, where high voltage values are not necessary. In addition, bipolar *SiC* devices are affected by a material degradation mechanism during forward current conduction associated with a kind of lattice defect called stacking fault. Recent improvements on material manufacturing have almost suppressed this limitation in practical applications [245].

(b) *Schottky Barrier Diodes (SBD)* (figure 3.5(b)): These unipolar devices also feature a low *on* state voltage drop and zero reverse recovery charge (Q_c), which produces a virtually null reverse recovery current (I_{rr}), allowing to switch very fast from *on* to *off*. However, the leakage current is larger than for PiN diodes and increases quickly with temperature. Schottky diodes withstand much lower surge currents than PiN diodes.

(c) *Junction barrier schottky (JBS) or Merged PN Schottky diode (MPS)* (figure 3.5(c)): This *SiC* diode has a hybrid structure. It combines the benefits of a low *on* voltage drop and a low reverse recovery current of SBD diodes with the high surge current capability and low leakage currents of PiN diodes [241].

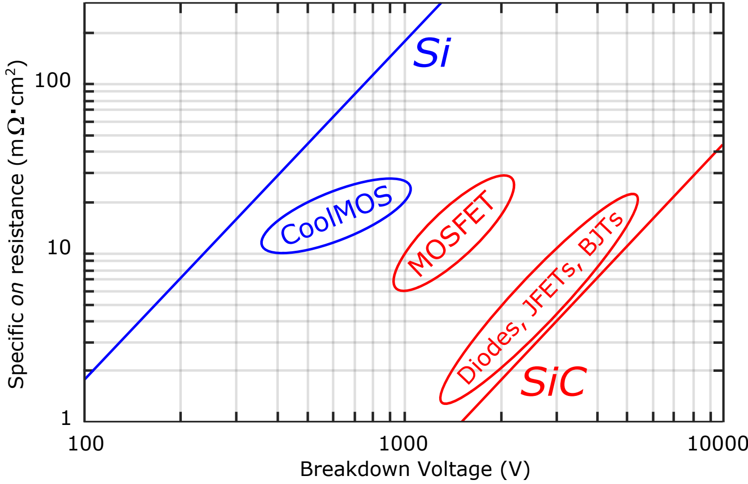


Figure 3.14: Breakdown voltages and *on* resistance of *SiC* devices.

For these reasons, the JBS diode is the common solution for most commercial *SiC* power semiconductor manufactures. Typical voltage and current ranges of such devices are shown in figure 3.6(a), highlighting 600 V, 1200 V and 1700 V standard voltage ratings with a current range between 10 A and 50 A. Figures 3.8, 3.9 and 3.10 highlight key advantages of JBS diode technology, such as low reverse recovery charge (3 nC@30 A-370 nC@50 A), low forward voltage (1.35 V@30 A-4 V@25 A) and relatively high maximum operation temperatures (175^{0}C). Thus, JBS diodes can be considered, among current solutions, as the best alternative for their application in automotive power converters.

On the other hand, the use of ultrafast *SiC Schottky* diodes as *freewheeling* (FWD) in switching devices is gaining more and more integers, especially if the power densities require high switching frequencies [242]. When this combination is not enough, other types of solutions are used as a power MOSFET with a serial diode connecting a *SiC* diode in parallel. However, this solution is more expensive and reduces dynamic losses at the expense of increasing driving losses [242].

3.2.2 *SiC* BJT

The *SiC* BJT is a bipolar device that operates normally *off* (although for the electronic community this fact is obvious, this qualification is exposed due to the fact that certain WBG devices are normally *on*), including high blocking voltage ranges (1200 V-1700 V) and wide current ranges (3 A-160 A) (figure 3.6(b)) [29].

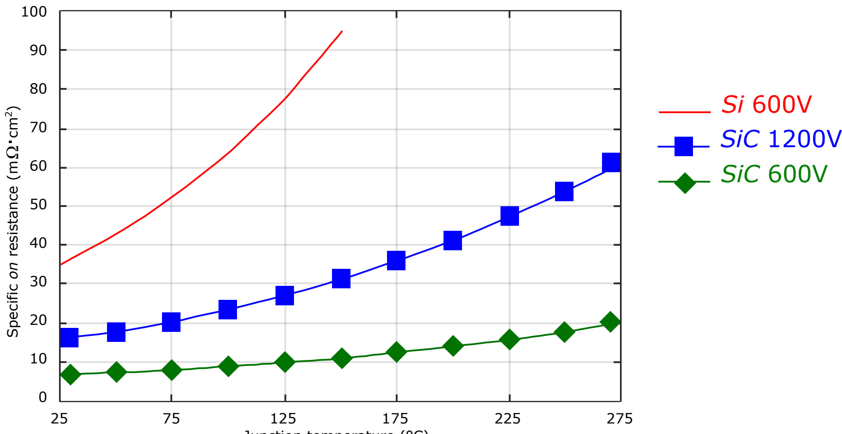


Figure 3.15: Variation of *on* resistance with the temperature over *SiC* JFET devices and *Si* technology.

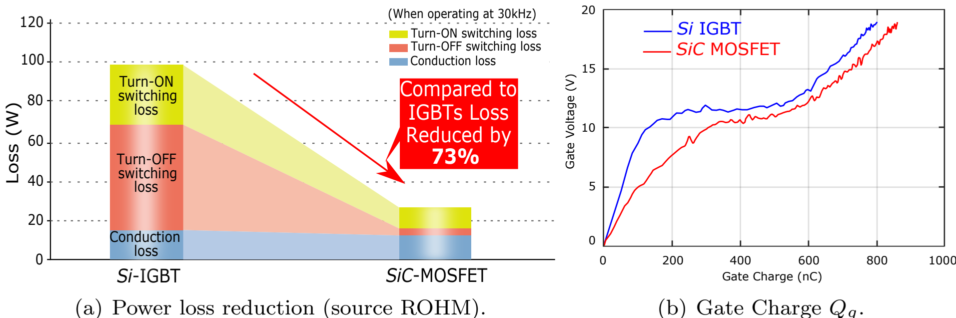
These devices have low conduction voltage drops, thanks to an equivalent low *on* state resistance (10 $m\Omega$-470 $m\Omega$), a positive R_{on} temperature coefficient and fast switching capabilities [238, 246] (figure 3.11(a)). The structure of this device can be seen in the figure 3.5(d).

Besides, this device exhibits good behaviour at high voltages (figure 3.14) and at high temperatures [247], being extremely robust [238]. However, they are current controlled devices, and have a negative current gain temperature coefficient. In addition, the design of the driver circuit becomes more complex than for voltage controlled devices in comparison with unipolar devices (JFET and MOSFET).

3.2.3 *SiC* JFET

In principle, *SiC* JFETs can be considered as an excellent alternative for HEV/EV [242], because the lack of gate oxides allows to operate at high temperatures without stability problems (which occur in MOSFETs) [246, 248]. Moreover, the threshold voltage is independent of the junction temperature, and they exhibit an ultra low *on* resistance [29, 242, 249]. The variation that the conduction resistance undergoes with the temperature is smaller than that which occurs in traditional *Si* devices. This variation can be seen in the figure 3.15.

SiC JFETs are by default normally *on* devices that are *off* when the gate-source p-n junction is reverse biased. In a similar way than for *GaN* HEMTs, normally *off* devices can be obtained by connecting a low R_{on} *Si* MOSFET in cascode configuration with the *SiC* JFET (figure 3.11(b)). Nevertheless, the same effect can be obtained by modifying the JFET gate structure in a way



(a) Power loss reduction (source ROHM). (b) Gate Charge Q_g.

Figure 3.16: Comparation of *SiC* MOSFET and *Si* IGBT.

that the channel region is interrupted (or depleted) at zero gate bias, although the subsequent threshold voltage is relatively low. Due to such a low threshold voltage, JFETs require specific driving circuits different from standard *Si* IGBT drivers. In both approaches, the price to pay for having a normally *off* behaviour increases R_{on}. Attending to the internal structure used for their design and fabrication [29, 30, 246], *SiC* JFETs can be divided into two families:

(a) Lateral channel component JFETs (LC_{JFET}, figure 3.5(e)). Although such devices are vertical, their channel shows a lateral component. They show higher *on*-state resistance than their vertical counterparts [250, 251].

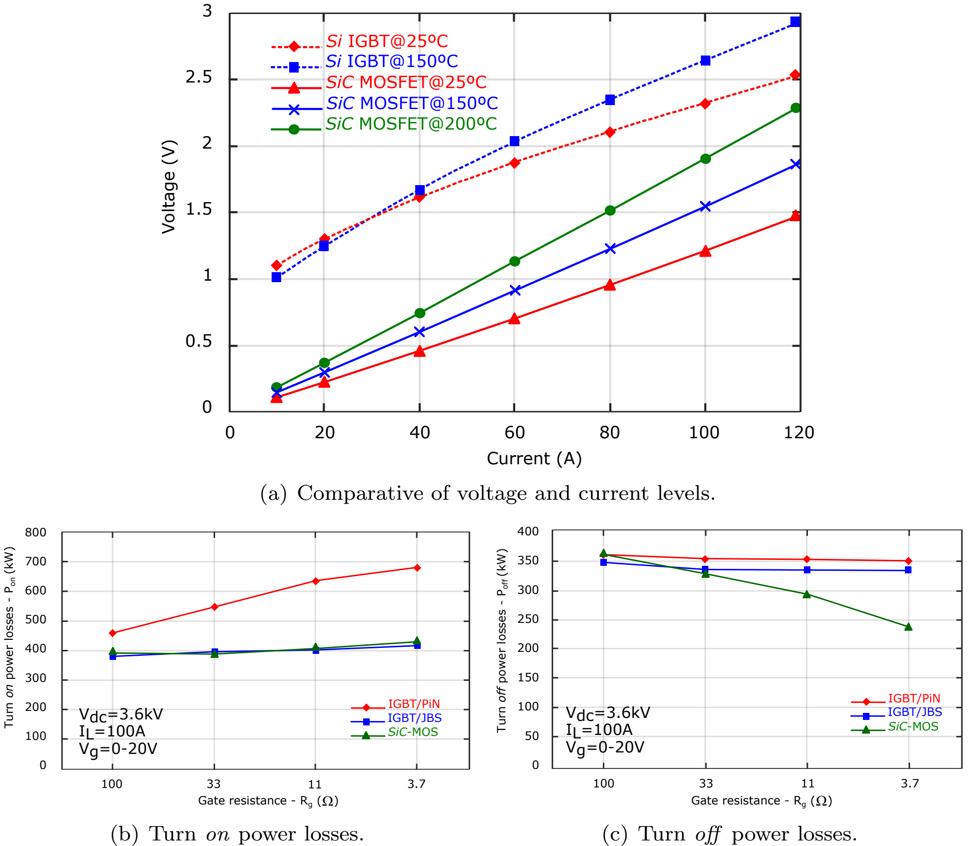
(b) Vertical trench JFETs (VT_{JFET}, figure 3.5(f)). In this technology, the conduction channel is completely vertical, allowing a much higher level of integration and a lower *on*-state resistance [252].

Overall, it can be concluded that normally *off* *SiC* JFETs are still not mature enough for HEV/EV applications. In spite of their voltage and current levels (figure 3.7(a)), high current modules have not yet been commercialized.

3.2.4 *SiC* MOSFET

These devices have the same vertical structure (figure 3.5(g)) than *Si* MOSFETs, are normally *off*, and provide a good balance between conduction and switching losses [28] due to their low *on* resistance and Q_g charge (figures 3.12 and 3.16(b)). In this context, figure 3.16(a) shows the theoretical power loss reduction that could be achieved when substituting *Si* IGBTs by *SiC* MOSFETs of similar ratings.

Another relevant feature is that they can be fired using the same driver circuitry as for *Si* IGBTs (the referent for current power converters in HEV/EV propulsion systems), making the transition between both technologies easier. Additionally,



(a) Comparative of voltage and current levels.

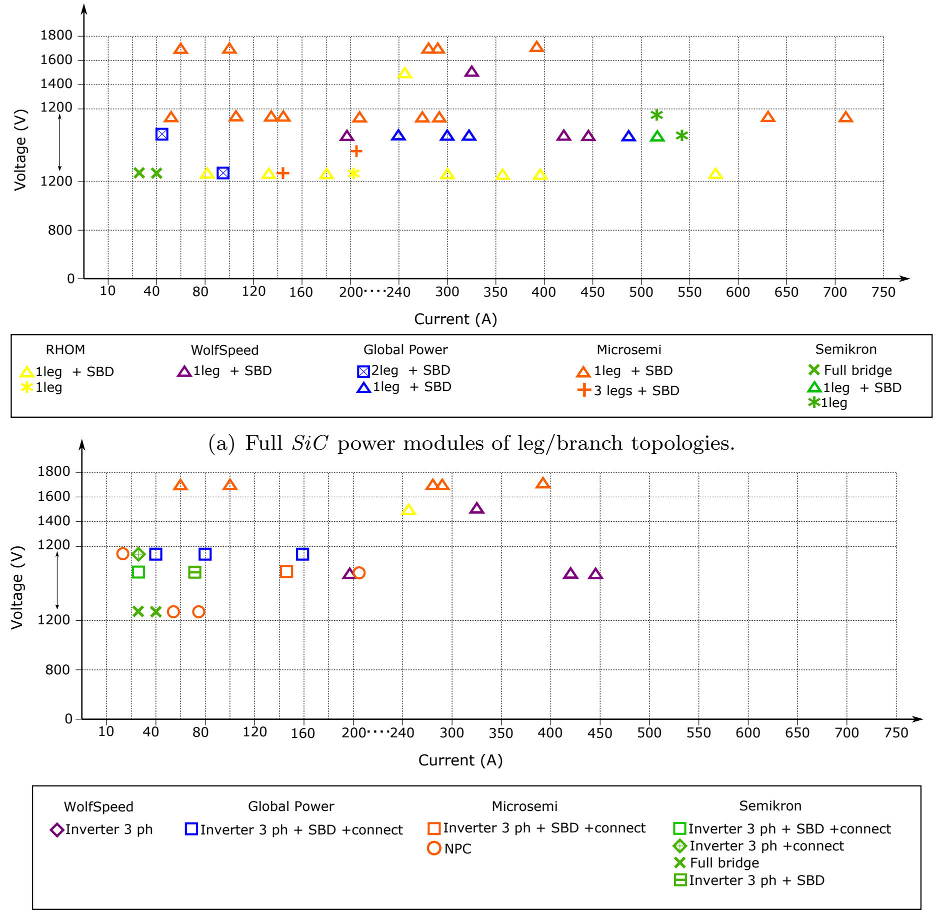
(b) Turn *on* power losses.

(c) Turn *off* power losses.

Figure 3.17: Comparative of *SiC* MOSFET and *Si* IGBT.

they can operate without an external antiparallel diode, due to the body diode present in the transistor structure [28, 253, 254]. Nevertheless, this solution must be analysed for each application, because better results will be probably obtained with external and optimized JBS diodes. Charge (Q_{rr}) values are very similar to the gate MOSFET charge (Q_g) (figure 3.12). In general, *SiC* MOSFETs are at this moment the devices receiving more research efforts for medium and high power applications (for example, for improving the long term threshold voltage stability) and significant improvements are continuously reported. For example, a major breakthrough was the introduction of the ultra-low R_{on} *SiC* MOSFETs based on a trench gate structure [238, 244, 248].

Regarding voltage and current ratings of such devices (between 400 V-1700 V and 2.6 A-100 A, figure 3.7(b)), their implementation in HEV/EV propulsion



(a) Full SiC power modules of leg/branch topologies.

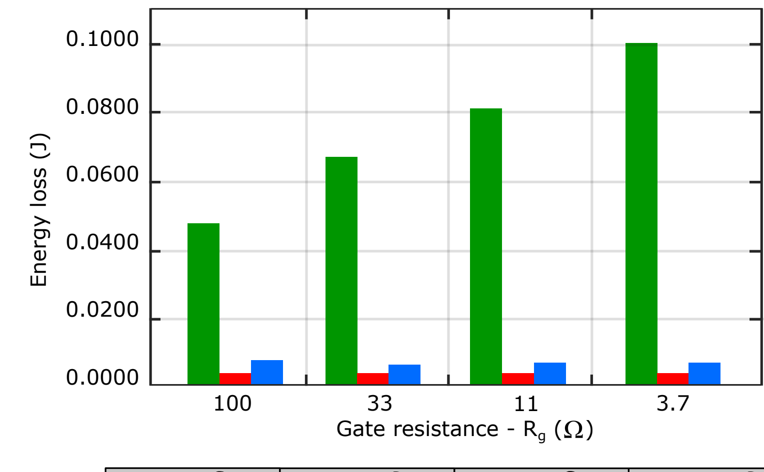
(b) Full SiC power modules of inverter topologies.

Figure 3.18: Commercial full SiC power modules.

applications [255] is feasible using the devices with the higher current range. In this sense, a number of manufacturers are producing full SiC MOSFET modules[1].

An example of SiC full power module, the figure 3.17(a) shows a comparison of the conduction performance of an inverter based on SiC MOSFET technology and its equivalent Si IGBT. The figures 3.17(b) and 3.17(c) [255, 256] show a comparison between of switching losses according to the gate resistance. As it can be seen, the conduction behaviour and switching losses are improved using

[1]These modules include SiC JBS diodes in anti-parallel to the transistors in order to improve the properties of the module, as the performance of the body diode of a SiC MOSFET is inferior than the performance of the JBS [256].



	100 Ω	33 Ω	11 Ω	3.7 Ω
6.5kV PiN	0.0488 J	0.0713 J	0.0860 J	0.1023 J
6.5kV JBS	0.0051 J	0.0029 J	0.0028 J	0.0028 J
10kV JBS	0.0061 J	0.0053 J	0.0051 J	0.0051 J

Figure 3.19: Comparison of *freewheeling* diodes with *Si* IGBT respect to gate resistance (R_g).

SiC technology. Finally, the figures 3.18(a) and 3.18(b) show the voltage and current ranges of the main full *SiC* commercial solutions available in the market.

3.2.5 *SiC* IGBT

The *SiC* IGBT is a device in experimental phase [257, 258]. The manufacturing techniques and processes have not been yet standardized [258–261]. The device benefits are far from *SiC* substrate properties are expected. The biggest problem is focused on the electron and hole concentrations that must optimized [262]. The proposed structure [261] for this *SiC* device can be seen in the figure 3.5(h).

On the commercial level, when they refer to *SiC* IGBT devices, they are really last generation *Si* IGBTs with the *SiC* diode (FWD). The incorporation of these diodes causes a significant improvements, using for this purpose the *SiC* JBS [260]. By incorporating the *SiC* diode, the losses are reduced by approximately 37 %, as shown in the figure 3.19.

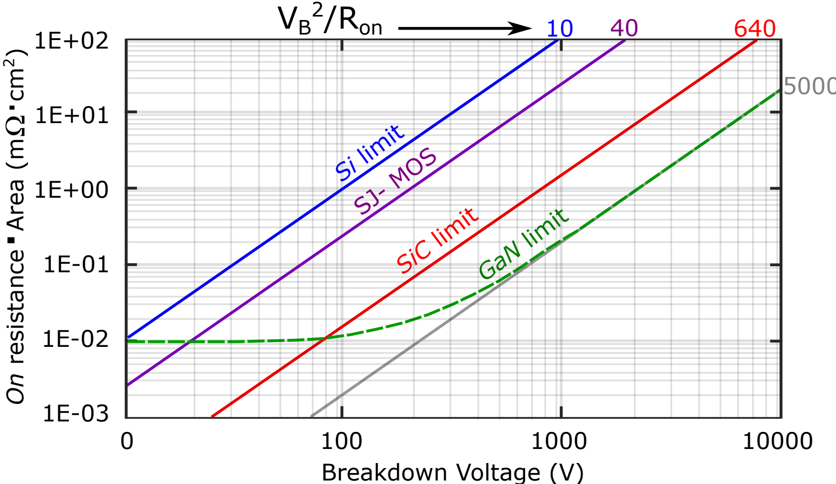


Figure 3.20: Comparison of breakdown voltage and *on* resistance for semiconductor material alternatives.

3.3 Gallium Nitride (*GaN*) devices

The Gallium Nitride is of interest in the use of devices for high voltages at high frequencies due to its *wide bandgap*, its large area of electric field, the high mobility of electrons and its reasonable thermal conductivity.

Better behaviours can be achieved through *GaN* power transistors instead of *Si* IGBTs. It is expected that the switching devices manufactured in *GaN* have an approximate behaviour of 100 times higher than the devices based on *Si*, and 10 times higher than the devices manufactured with *SiC* [143]. In this sense, the power electronics based on *GaN* will improve two key aspects: the conduction resistance (figure 3.20) and the switching speed, achieving a significant reduction in conduction and switching losses, respectively [143].

Current *GaN* devices are based on *GaN* and *GaN* alloy thin layers epitaxially grown on various substrates (sapphire, *SiC* and *Si*), since high quality GaN mono-crystalline wafers are not yet available [263, 264]. The interface between such layers presents a very low resistance sheet, known as the 2-D electron gas (or 2DEG) layer, which allows optimum lateral electrical conduction due to a very high electron mobility. All these advantages convert the *GaN* (heterogeneous structure) into an interesting technology for the automotive, since great improvements are required in terms of losses, temperature and greater integration of the systems [228, 265].

However, it is real that there are technological problems [228, 265], the current ranges and reliability are insufficient for the current application in automotive

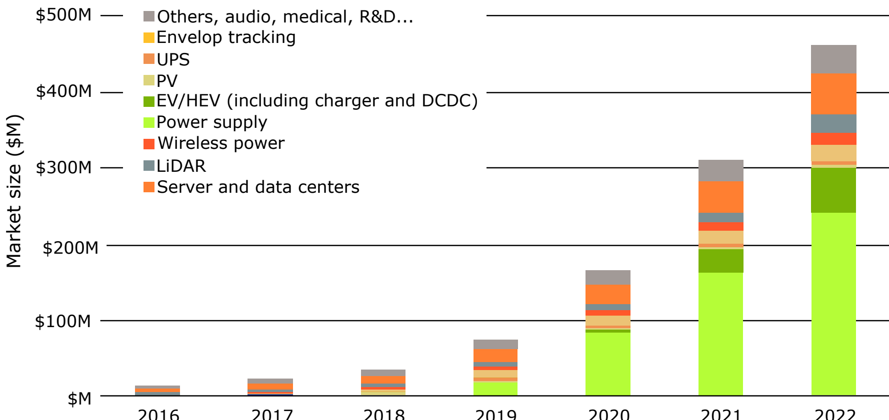


Figure 3.21: Current *GaN* market status and future prospects.

propulsion inverters. Despite such drawbacks, *GaN* technology has high potential. In recent years, there have been various acquisitions/associations [266] between traditional *Si* power semiconductor manufacturers and high-tech and smaller companies specialized in *GaN* technology. This fact highlights the interest of the industry in *GaN*. To name some examples, Infineon has acquired International Rectifier, Fujitsu has done the same with Transphorm, Rhom has acquired *GaN* Systems, and ST Microelectronics has partnered with Leti CEA. Current technological applications for *GaN* are diverse, as they cover lighting systems (opto-LED), consumer equipments (opto-laser, power supplies, etc.), radio-frequency, aerospace and defence, health and virtual reality (figure 3.21 [266]). Regarding power applications, there are several *GaN* technology companies (EPC, Exagan, GaN Systems, ST Microelectronics through Leti CEA, NTT, Panasonic and Transphorm) involved. In some references [264, 267–269], it is stated that *GaN* will be competitive with *Si* and *SiC* for future HEV/EV applications which will demand higher switching frequencies at medium voltage. However, currently commercial devices of a few tens/hundreds of kW are nonexistent[1].

Thus, it can be said that *GaN* technology is still not a valid option for HEV/EV application. However, the great expectations on the material and its development keep hope like a future alternative to IGBTs in traction applications such as hybrid and electric vehicles.

[1]As an example, EPC offers devices with 350 V@6.3 A; and 90 V@90 A; GaN Systems reaches 650 V@120 A; TI 600 V@12 A; Panasonic 600 V@10 A; and, finally, Transphorm reaches 600 V with a drain current of 20 A. Commercial *GaN* multichip power modules are not available.

Next, the main devices based on *GaN* technology are briefly explained. It is important to indicate that some of them are in the experimental phase or in the first steps of their commercialization. In this sense, the figure 3.3 summarizes the commercially available *GaN* device options, showing the most relevant for the automotive market [30, 228, 270].

3.3.1 *GaN* diodes

The *Schottky* diodes of *GaN* power are in experimental phase, presenting a lateral or quasi-vertical structure. The quality of the material is crucial in the design of this type of semiconductors because the defects that can be produced directly affect the *Schottky* barrier and, therefore, the maximum blocking capacity available to the device.

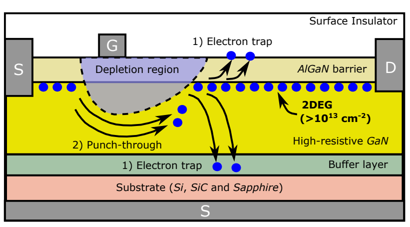
Another problem with these devices is the high cost of the *GaN* substrate, which means that diodes of other cheaper materials are used for various applications. Another option to try to take advantage of the properties of *GaN* material is the development of diodes in heterogeneous structures. That is, combining the *GaN* with another substrate such as: *Si*, *SiC*, even, sapphire [270].

The breaking voltages of the lateral *GaN* diodes on sapphire substrates are around 9.7 kV, but the forward voltage drop is still high. Also, by means of the availability of substrates *GaN* HVPE (*Hydride Vapour Phase Epitaxy*) have been able to start up *GaN Schottky* diodes of 600 V that could compete in the market with *SiC* diodes. Also, it is expected that the *GaN* JBS diodes can improve the behaviour of power rectifiers in the range of 600 V to 3.3 kV [243].

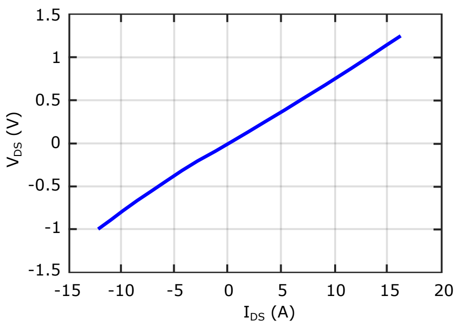
3.3.2 *GaN* transistors

Up to date, the only commercially available *GaN* power devices are the High Electron Mobility Transistors (HEMT, figure 3.22(a)), which are based on such effect using *AlGaN/GaN* thin layers grown on *Si* wafers (*GaN*-on-*Si* technology), the result being a suitable technology for medium power applications and in the range of 1300 V [271–273]. They are normally *on* by nature, and their working principle is based on interrupting the 2DEG low resistance channel between Drain and Source terminals by acting on a third control or Gate terminal. It highlights the advantage of driving current in both directions, showing its potential as active *freewheeling* (figure 3.22(b)) or as a converter switch for matrix converters [274, 275].

In recent years, it has also been possible to manufacture the device on *SiC* substrate, that is, the *GaN* HEMT transistor is composed of *GaN/SiC* obtaining



(a) *GaN* HEMT internal structure.



(b) Active *freewheeling* capability.

Figure 3.22: *GaN* HEMT transistor.

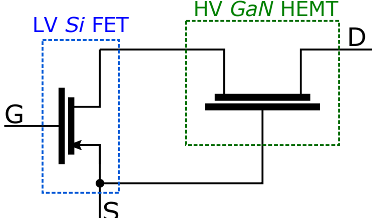
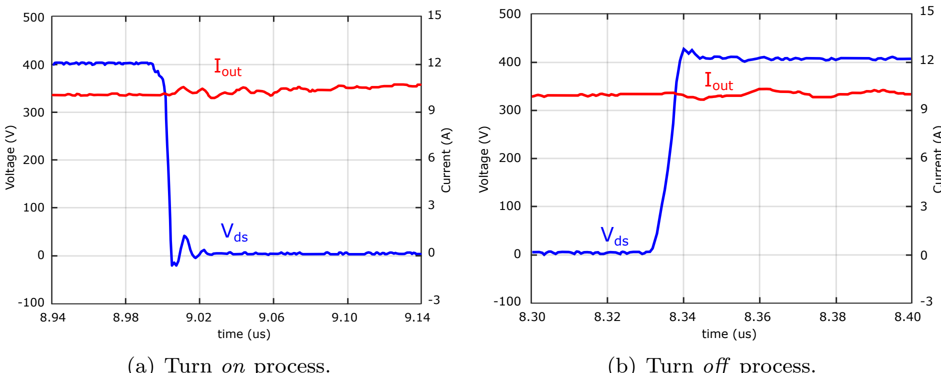


Figure 3.23: Cascode configuration of *GaN* HEMT transistor to get normally *off* operation.

values of lower conduction resistance 2 mΩ· cm^2, while the initial devices of *GaN*/*Si* had resistances around 2.8 mΩ· cm^2 [276].

Many efforts have been addressed to obtain normally *off* switches, because the safety requirements of HEV/EV applications make extremely important to rely on such kind of switches for the propulsion inverter [277]. One solution consists of connecting, inside the same package, the normally *on* *GaN* HEMT with a normally *off* low voltage *Si* MOSFET in cascode configuration (figure 3.23) [276, 278–280]. The main problems of this solution are the addition of the *on*-state resistances of both devices in series, and the maximum operation temperature limitation introduced by the *Si* MOSFET. The behaviour of this type of device has been analyzed in [279]:

- ❒ Turn *on* (figure 3.24(a)): the turn *on* and *off* of the device depend mainly on the *Si* MOSFET device, which is used as a cascode switch. This MOSFET transistor usually has voltage ranges of 30 V and current of around 10 A (for temperature of 70°C). The total switching load is around 4.2 C, causing a delay in the turn *on* process to be around 8.2 ns, the rise time being about 11 ns. All this indicates an excellent behaviour in the turn *on* process, comparing with IGBTs of similar characteristics.



(a) Turn *on* process. (b) Turn *off* process.

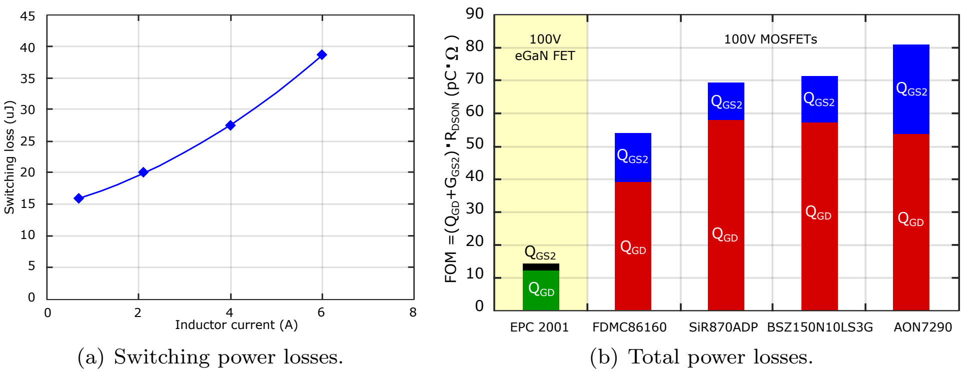
Figure 3.24: Turn *on* and *off* processes of cascode *GaN* HEMT transistor.

- Turn *off* (figure 3.24(b)): to turn *off* the *GaN* HEMT transistor, the *Si* MOSFET must be *off*. When using a low-voltage MOSFET device, the charge stored between the gate-source junction is very low, ensuring a fast turn *off*. Also, being a MOSFET is not necessary to apply a negative voltage, in fact, applying a negative voltage can be counterproductive because an accumulation of gaps in the gate can occur. The optimal solution is to apply a voltage of 0 V to avoid problems of storing load and of increasing conduction resistance. As with the turn *on* process, the delay depends on the transistor *Si* MOSFET. In the example shown [279] the device has turn *off* delays of about 15 ns and a decay time of about 7 ns. Note that since there is no physical diode in the *GaN* HEMT device, the device has low power losses during the turn *off* process.

Considering the switching characteristics of the *GaN* HEMT cascode device, it has a behaviour that resembles a *Si* power MOSFET. Comparing a *GaN* HEMT device of 100 V and several *Si* MOSFETs, the *GaN* device reduces the power losses up to 50 % [281], as the figures 3.25(a) and 3.25(b) show.

Another approach for obtaining a normally *off* HEMT consists of including additional gate structures in the device, depleting the conductive channel at zero gate bias. So far, nowadays there are two main technological approaches to do that. The first solution is based on a *p*-*n* junction structure between the gate and source, leading to the so called *p*-HEMT family of transistors [282–284]. The second option is based on the introduction of a metal-insulator-semiconductor (MIS) structure at the gate level, leading to the MIS-HEMT family [285–287].

In principle, the very low *on*-state resistance ($\sim$25 $m\Omega$) and fast switching speed achieved by 650 V *GaN* devices could make such devices good candidates for certain HEV/EV applications [143]. Nevertheless, HEMTs are lateral devices



(a) Switching power losses. (b) Total power losses.

Figure 3.25: Power losses of cascode *GaN* HEMT transistors.

with very narrow gate fingers to ensure their blocking capability (either for normally *on* and *off* devices, or for *p*-HEMTs and MIS-HEMTs). These structural characteristics lead to two facts that determine the behaviour of *GaN* HEMTs. Firstly, the narrow gates, the lateral current conduction scheme and the not too high *GaN* thermal conductivity are less favourable for heat dissipation (higher thermal resistance) than the common scenario found in vertical devices [288], limiting the maximum current ratings of *GaN* HEMTs. Secondly, the blocking voltage between drain and source must be withstood in the device surface (not in the semiconductor volume, as is the case in vertical devices). Due to the surface defects, the maximum theoretical breakdown voltage related with *GaN* properties cannot be achieved [278]. In addition, the breakdown mechanism in such lateral devices is destructive (another difference with vertical IGBTs and diodes), significantly limiting their reliability. Important research efforts are now being carried out in order to obtain high quality *GaN* substrates, allowing the development of vertical devices (*GaN*-on-*GaN* technology) [263, 264].

3.4 Conclusions

Considering the electric operation conditions for the power train of HEV/EV applications mentioned in chapter 1, their power converters could be manufactured by an affordable parallelization of modules, discrete devices and dies. The usage of WBG power semiconductors are an interesting alternative in order to overcome the *Si* limitations, specially in applications where high voltage operations, high switching frequencies and high temperatures are required.

Regarding the WBG materials, the *SiC* and *GaN* are the most important technologies with a higher development level. From the literature review, it can be concluded that *SiC* devices offer better features of voltage (600-1700 V)/current

Table 3.1: *SiC* semiconductor technologies, listing their most relevant advantages and disadvantages.

Device	Main advantages	Main disadvantages
SiC diodes	Lower reverse recovery charge. Lower switching losses than *Si*. Positive temp. coefficient.(1)	
PiN	High Voltage (>3,3 kV). Low leakage current (Temp. independent). Low conduction resistance.	High reverse recovery current. High reverse recover charge.
SBD	Typical voltage about 600 V. Low reverse recovery current. Low reverse recovery charge.	Higher leakage current. High variation with temperature.
JBS	Hybrid device (SBD and PiN) 600 V-3.3 kV.	
SiC BJT	Normally *off*. Low conduction voltage drop. Gate-emitter low conduction voltage. Fast switching dynamics.	Current controlled. Complexity of the driver(2).
SiC JFET (lateral, vertical)	High operation temp. Threshold voltage no temp. dependency. Vertical JFET without parasitic diode.(5) Low conduction resistance.	Lateral JFET normally *on*.(3) VT_{JFET} normally *on*.(4)
SiC MOSFET	Normally *off*. Gate charge similar to *Si* IGBTs. Same drivers as for *Si* IGBTs can be used.(6) Ratings similar to *Si* IGBTs. (7) Higher switching frequencies. Positive temperature coefficient. (1) Higher thermal conductivity.	Low robustness. (gate reliability).

Table notes:
(1) Required for easy device parallelization.
(2) Compared with the voltage controlled devices.
(3) Compromising converter safety under transistor firing control malfunctions.
(4) VTJFET normally *on* appears in cascode configuration to be normally *off*.
(5) Such parasitic diodes exhibit low performance, including high conduction losses.
(6) Simplifying the migration from *Si* to WBG power conversion technology.
(7) Taking into account that *SiC* Mosfet is compared with IGBT structure.

(approximately 10-50 A) ranges, thermal conductivity and development level than *GaN* technology for their integration on HEV/EVs.

Nowadays, the *SiC* market clearly presents a major and more appropriate device offer than *GaN* market for power electronic applications. In the case of *GaN* technology, there are many devices in development state as *GaN* diodes and normally *off* *GaN* HEMT transistors (cascode configuration, *p*-HEMT and MIS-HEMT). However, the *SiC* technology offers unipolar and bipolar devices as the table 3.1 shows, where the main features of *SiC*-based technologies are summarised. All these *SiC* devices continue with their evolution and development, as the case o f*SiC* IGBTs which continues in early research stages without being summarised.

Moreover, there are hybrid power modules which combine *Si* IGBTs and *SiC* diodes in order to improve the *freewheeling* behaviour, but there also are some full *SiC* power module solutions such half-bridge and inverter topologies. In contrast, the current *GaN* market does not offer commercial full power module solutions.

After this analysis, it can be drawn that *SiC* JBS diodes and *SiC* MOSFETs are the most adequate devices to substitute traditional *Si* FRD diodes and *Si* IGBTs. However, their ratings of discrete semiconductors are not high enough to cope with the present requirements of power train electric vehicles. Thus, parallelization through discrete elements or bare dies (constituting a power module) is mandatory in order to get higher current levels and other power requirements of HEV/EV applications. In this context, the implementation of ad-hoc power modules (using bare dies) could provide a better performance, because it will be feasible to manufacture power converters with low parasitic inductances, improved thermal characteristics and higher power densities, which are desirable features for automotive power applications. In the following chapters, the most relevant aspects regarding the design of future automotive *SiC* power modules will be studied.

Chapter 4

Parallelization of power semiconductors

4.1 Introduction

Today, power electronics applications usually require high power and current ranges.. These ranges are, sometimes, outside the ratings in which both discrete devices and power modules work. To solve this problem, power converter designs are resorted through the parallelization of:

- ❒ Power modules.
- ❒ Discrete / *bare dies* power semiconductors.
- ❒ Individual cells.

The main objective of the parallelization is to increase the capacity of current and, therefore of power, to which the converter can work. To reach this goal, the current must be balanced, that is, the total current must be distributed equally into each device or parallel module, as it can be seen in the example of the figure 4.1. This distribution must be as stable as possible in order to avoid drift of both current and temperature.

Obviously, there will be an imbalance in the current levels, but it must maintain as low as possible to achieve a correct parallelization and avoid serious design problems such as exceeding the SOA curve or the maximum junction temperature ($T_{j_{max}}$). The case shown in the figure 4.1 is ideal, in fact there are many factors

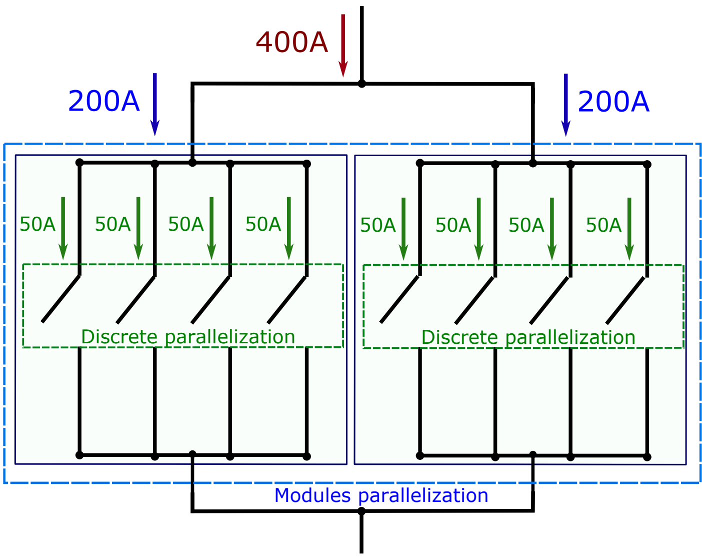


Figure 4.1: Current ideal balance in discrete parallel devices and parallel modules.

that interact between each other causing the current imbalances between discrete devices and, even, between modules. These conditions can be summarised:

- The parameters which characterize each device or module to be parallelized ($V_{ce_{(sat)}}$, $t_{d_{(off)}}$, temperature coefficient, etc) must be studied [289–291].
- The design of driver circuit, the gate impedance behaviour (Z_g) must be analysed, as well as various control strategies of common or separate gate [58, 184, 292–294].
- The design of power circuit, the layout parasitic inductance effects must be studied, particularly, the effects of emitter inductance [294–296].
- The variations in thermal circuit produced by each semiconductor[1] must taken into account in order to get a homogeneous thermal distribution.

If the aforementioned factors do not concur, the current flows into each parallel semiconductor will be different. The mentioned imbalances will be minimized through the design of all the converter stages (semiconductors, driver, power circuit and cooling system) is carried out.

[1]A thermal analysis is proposed in chapter 7, extracting thermal parameters of a power electronics design in order to check temperature variations and detect hot points due to wrong layout.

In the following sections, the most relevant aspects of parallelization are analysed through the study of the static and dynamic semiconductor characteristics and the circuit connections between driver and power layout, taking into account device thermal performances. These concepts are extracted from the parallelization of silicon discrete IGBT and power IGBT modules, taking as examples the automotive discrete AUIRGPS4067D1 IGBT rates 600 V/160 A and the power module FS800R07A2E3 IGBT rates 650 V/700 A (four times more current because of the internal parallelization of four IGBTs), both of Infineon. The parallelization concepts presented in this chapter constitute the basic knowledge for the development of *SiC* HEV/EV power module design criteria in chapter 5. The main literature of this chapter is focused in silicon solutions, consequently the chapter uses silicon IGBTs as power semiconductor of reference. However, these concepts can be extrapolated for other semiconductor technologies as it is explained in the following chapters.

4.2 Power semiconductor static behaviour

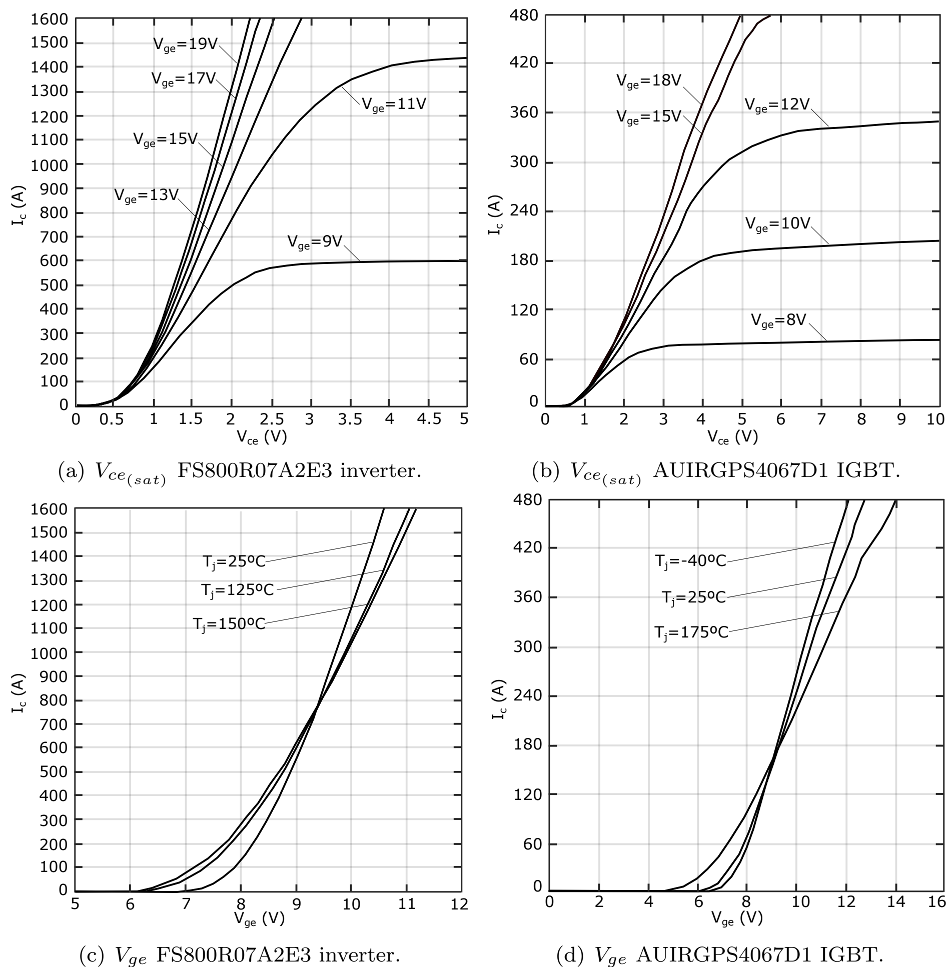
The static regime includes both the semiconductor conduction and cut-off states, being the latter irrelevant from the point of view of the parallelization [289]. The main static parameters that must be monitored to perform a correct parallelization are [290]:

- $V_{ce_{(sat)}}$, collector-emitter saturation voltage as a function of the junction temperature (T_j).
- $V_{ge_{(th)}}$, gate threshold voltage as a function of the junction temperature (T_j).
- V_{ge}, gate voltage.

The variation of the aformentioned parameters involves a current change (I_c) which flows through the IGBT or module (figures 4.2(a) and 4.2(b)). If this variation is caused by a semiconductor temperature change, both current I_c and threshold voltage $V_{ge_{(th)}}$ are affected (figures 4.2(c) and 4.2(d)). In the following sections, the influence of T_j over threshold voltage $V_{ge_{(th)}}$ and saturation voltage $V_{ce_{(sat)}}$ is analysed, as well as some design techniques to reduce current imbalance.

4.2.1 Temperature dependency on the semiconductor electrical parameters

The saturation voltage $V_{ce_{(sat)}}$ and gate voltage V_{ge}, as well as the threshold voltage $V_{ge_{(th)}}$, are the most important parameters to balance the devices connected



(a) $V_{ce_{(sat)}}$ FS800R07A2E3 inverter.

(b) $V_{ce_{(sat)}}$ AUIRGPS4067D1 IGBT.

(c) V_{ge} FS800R07A2E3 inverter.

(d) V_{ge} AUIRGPS4067D1 IGBT.

Figure 4.2: Characteristic curves of de I_c vs $V_{ce_{(sat)}}$ and I_c vs V_{ge}.

in parallel when they are in conduction state. In this sense, it is important to know the influence that temperature has on them.

The expression (4.1) provides the threshold voltage $V_{GE_{(th)}}$ according to the *Fermi* function (Φ_{FB}), a parameter (4.2) that describes the energy level and it is a function proportional to the joining temperature (T_j) [290]:

$$V_{ge_{(th)}} = -V_{ms} - \frac{Q_{SS}}{C_{OX}} + 2\Phi_{FB} + \frac{\sqrt{2\varepsilon_0\varepsilon_{si}N_{A_{max}}(2\Phi_{FB})}}{C_{OX}}; \qquad (4.1)$$

where V_{ms} is the metal-semiconductor voltage, Q_{SS} the extrinsic charge of the

energy states, C_{OX} the gate oxide capacity, $\epsilon_0 \varepsilon_{si}$ the material permittivity and $N_{A_{max}}$ the maximum concentration of the carriers in the material.

$$\Phi_{FB} = \frac{k \cdot T_j}{q} ln \frac{N_{A_{max}}}{n_i}; \tag{4.2}$$

where k is the Boltzmann constant, a the electron charge and n_i the intrinsic density of carriers.

In order to understand the behaviour of $V_{ge_{(th)}}$ with respect to T_j, the derivative is made in (4.3). The equation shows that the $V_{ge_{(th)}}$ voltage decreases when T_j increases, presenting a negative coefficient with respect to the temperature [290].

$$\frac{dV_{ge_{(th)}}}{dT_j} = \left[\frac{\Phi_{FB}}{T_j} - \frac{k}{q} \left(\frac{E_g}{2kT_j} + 1.5 \right) \right] \cdot \left(2 + \frac{\sqrt{2\varepsilon_0 \varepsilon_{si} N_{A_{max}} (2\Phi_{FB})}}{2\Phi_{FB} C_{OX}} \right) < 0; \tag{4.3}$$

where E_g is the silicon (material of the power semiconductor) band energy.

On the other hand, the collector-emitter saturation voltage ($V_{ce_{(sat)}}$) can be expressed as [290]:

$$V_{ce_{(sat)}} = I_c \cdot R_{ch} = \frac{I_c \cdot l}{z \mu_{ns} C_{OX} (V_{ge} - V_{ge_{(th)}})}; \tag{4.4}$$

where R_{ch} is the channel resistance, l the channel length, z the channel width in the perpendicular direction and μ_{ns} the carriers mobility in the channel.

The parameter of the carriers mobility in channel (μ_{ns}) decreases with the temperature T_j (4.5) [290]. Taking into account that the voltage applied during the turn *on* process (V_{ge}) is usually much higher than the gate threshold voltage $V_{ge_{(th)}}$, the expression (4.5) demonstrates that the collector-emitter saturation voltage $V_{ce_{(sat)}}$ increases with the temperature T_j according to (4.4) and (4.5).

$$\mu_{ns}(T_j) = \mu_{ns}(T_0)(T_j)^{-m}; \tag{4.5}$$

When carrying out the parallelization, a positive temperature coefficient is sought for the voltage $V_{ce_{(sat)}}$, since it facilitates the parallelization due to the fact that the shared current is self-balancing, reducing the current flowing through the device that is warmer [297]. In this sense, when talking about the temperature coefficient, this concept usually refers to the behaviour of the voltage $V_{ce_{(sat)}}$ with respect to T_j. This static behaviour is modelled in figure 4.3 for the commercial

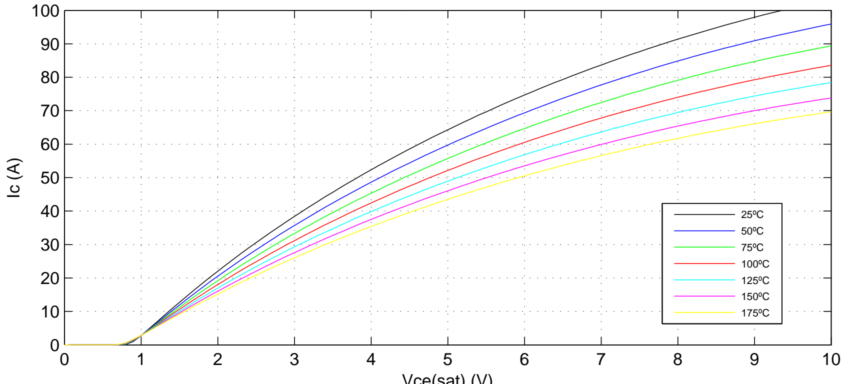


Figure 4.3: Saturation voltage positive coefficient with $V_{ge} = 18\ V$.

device AUIRGPS4067D1 IGBT. If devices with a negative temperature coefficient are used for the parallelization, the current imbalances and thermal leakage problems are more likely [298].

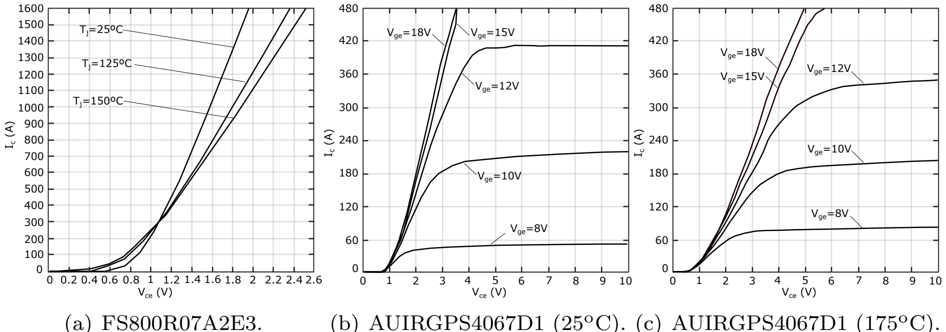
4.2.2 Current balance in conduction state

In order to get a power converter with parallel semiconductors balanced, similar characteristic curves are necessary so that all the devices provide an approximately equal current. For the particular case of IGBTs, the saturation voltage characteristic curve ($V_{ce_{(sat)}}$) versus the IGBT current (I_c) depends on the device junction temperature (T_j), as the figures 4.4(a), 4.4(b) and 4.4(c) show.

In parallel devices, all of them have the same saturation voltage $V_{Cce_{(sat)}}$, but in order to ensure they are balanced, the following conditions must be met:

1. The output characteristic curve of all devices ($V_{ce_{(sat)}}$ versus I_c) should be as similar as possible. These curves must be practically equal in all ranges of junction temperature, presenting the same temperature coefficient behaviour and being positive in all current ranges. To achieve this, the IGBTs must belong to the same manufacturer, model and, if it is possible, batch (same *code bar*). In this way, the output characteristic curve of the IGBTs will be practically the same and will exhibit the same behaviour for temperature variation [293].

2. Another requirement is that all the devices must have the same or similar as possible thermal behaviour. This implies that the parallelized IGBTs should present a thermal difference between devices practically null (4.6) [291, 299]. For this reason, a precise design of the thermal cooling circuit



(a) FS800R07A2E3. (b) AUIRGPS4067D1 (25ºC). (c) AUIRGPS4067D1 (175ºC).

Figure 4.4: Evolution of de $V_{ce_{(sat)}}$ according to T_j and I_c.

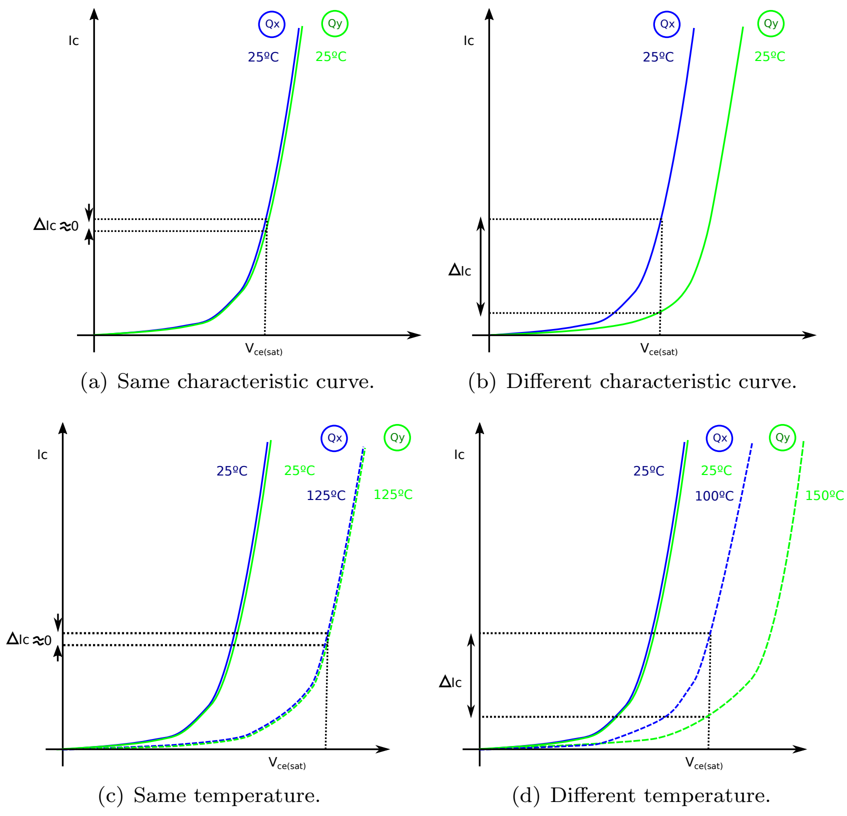
must be carried out, each semiconductor must have similar thermal resistance and transient impedances, so that the heat is distributed in the most homogeneous way possible.

$$|\Delta T_{j_{xy}}| \simeq 0^{o}C \tag{4.6}$$

If the two previous requirements are met, balancing the temperature of devices, working on the same characteristic curve is possible. In fact, it could be possible to achieve a practically zero current imbalance between the IGBTs (4.7) [291, 300]. At production level, to ease the parallelization, some manufacturers classify devices with ranges of $\Delta V_{ce_{sat}}$ less than 500 mV, allowing to limit the mismatch of currents between devices between 10-20 % [289, 300, 301].

$$|\Delta I_{c_{xy}}| \simeq 0\ V; \tag{4.7}$$

As an example, the figure 4.5 presents different cases of current balance or imbalance are presented according to the previous conditions. The figures 4.5(a) and 4.5(b) show a substantial difference between the characteristic curves of the parallel devices, regardless of the temperature, causing a large current difference in the devices. On the other hand, the figures 4.5(c) and 4.5(d) highlight that equivalent devices (same characteristic curve at same temperatures) at different temperatures present high current imbalance with the possible failure of the hottest IGBT and, therefore, the breakdown of the system.



(a) Same characteristic curve. (b) Different characteristic curve.

(c) Same temperature. (d) Different temperature.

Figure 4.5: ΔI_c between two IGBTs according their characteristic curve and T_j.

4.3 Power semiconductor dynamic behaviour

During the process of turning *on* and *off* over semiconductors, several effects can produce current imbalances. In this sense, the dynamic behaviour is increasingly important since the switching frequencies are continuously increasing in power applications. The most important dynamic parameters to be taken into account for the IGBT parallelization are (figure 4.6) [290, 302]:

- $t_{d_{(on)}}$, delay time of the turn *on* process: from 10 % of voltage V_{ge} to 10 % of current I_c.

- t_r, time of rise: from 10 % to 90 % of current I_c.

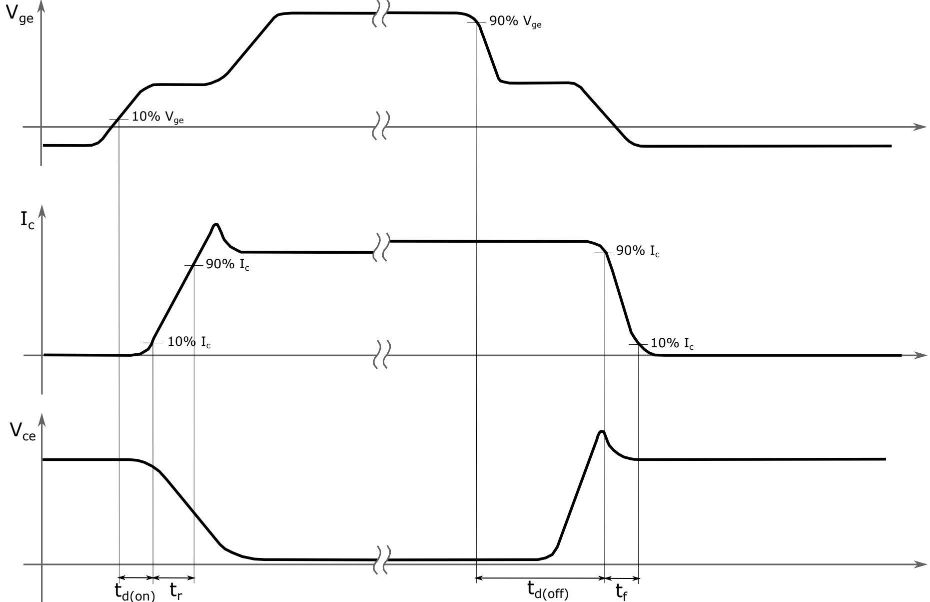


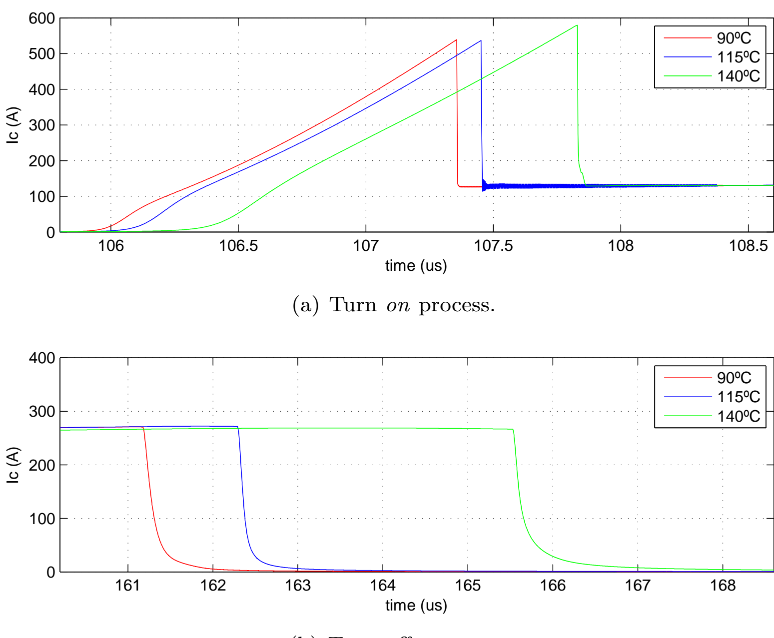
Figure 4.6: Main parameters of the dynamic behaviour.

- $t_{d_{(off)}}$, delay time of the turn *off* process: from 90 % of voltage V_{ge} to 90 % of current I_c.
- t_f, time of fall: from 90 % to 10 % of current I_c.

The temperature variation of the devices/modules in parallel is translated into a switching time variation, which produces a variation of switching losses, causing the change of the device junction temperature. When the temperature changes, the operation point is also modified and, therefore, causing a device current imbalance. Besides, the $V_{ge_{(th)}}$ voltage must be also considered, since it depends on the temperature. Thus, for various $V_{ge_{(th)}}$ of parallel devices, the delay times will be different, causing an imbalance.

4.3.1 Temperature dependency on switching time

As it occurs in the static behaviour, the temperature plays an important role in parallel devices during the switching, influencing many parameters that intervene in this operating regime. In this sense, there can be variations in the threshold voltage of the IGBT devices ($V_{ge_{(th)}}$), causing current variations during *on*/*off* processes [289]. The threshold voltage $V_{ge_{(th)}}$ influences the turn *on* delay ($t_{d_{(on)}}$) and *off* delay ($t_{d_{(off)}}$), these indirectly affect the current equilibrium of IGBTs, as shown in (4.8):



(a) Turn *on* process.

(b) Turn *off* process.

Figure 4.7: Transit variation according to temperature.

$$t_{d_{(on)}} = -\tau_1 \cdot ln(1 - \frac{V_{ge_{(th)}}}{V_{ge}}); \tag{4.8}$$

where the time constant τ_1 is:

$$\tau_1 = R_G(C_{ge} + C_{gc}); \tag{4.9}$$

and the derivative of $t_{d_{(on)}}$ respect to T_j is:

$$\frac{dt_{d_{(on)}}}{dT_j} = -\tau_1(\frac{V_{ge}}{V_{ge} - V_{ge_{(th)}}}) \cdot \frac{dV_{ge_{(th)}}}{dT_j} > 0 \tag{4.10}$$

According to the equations (4.8), (4.9) and (4.10), the turn *on* delay ($t_{d_{(on)}}$), and analogously with the turn *off* delay ($t_{d_{(off)}}$), increases with the temperature T_j. The figures 4.7(a) and 4.7(b) show the effects of the different operation temperatures during *on* and *off* processes [290].

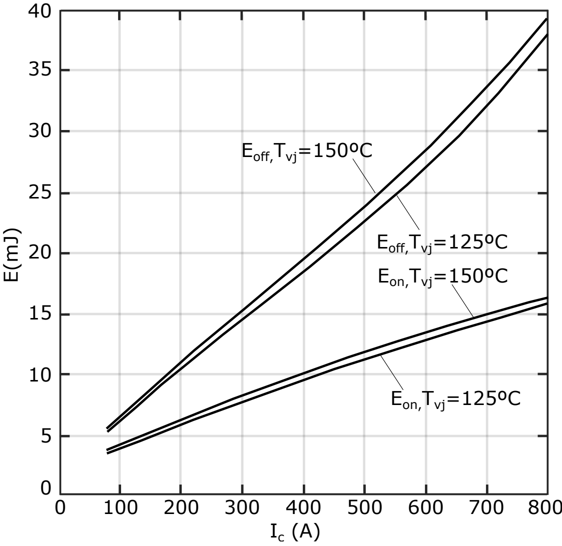


Figure 4.8: Switching losses according to T_j.

If one of the parallel IGBTs has a shorter $t_{d_{(on)}}$ or longer $t_{d_{(off)}}$, then it will flow more current. The same case will occur if the IGBT has a lower t_r or a longer t_f. In addition, by varying the delay times with the temperature, the switching losses change as the figure 4.8 shows [303].

4.3.2 Current balance during switching

During the turn *on* process, the greater temperature imbalance of the parallelized devices ($\Delta T_{j_{xy}}$), the greater current variation is. In addition, this difference is also maintained when the device is in a stable driving state [293]. However, the imbalances that occur during turn *on* are less relevant than during the turn *off* process. In fact, the temperature variations during turn *off* are critical (figure 4.9).

Therefore, eliminating or reducing the factors that generate thermal imbalances and temperature variations $\Delta T_{j_{xy}}$ during the turn *off* process are unavoidable. One way to reduce this temperature variation is through the correct design of both layout [301] and thermal design.

Taking into account that the parameters $t_{d_{(on)}}$ and $t_{d_{(off)}}$ increase their duration with the temperature T_j increment, if the IGBTs connected in parallel operate at different temperature, a current imbalance occurs due to the difference of these delays [290].

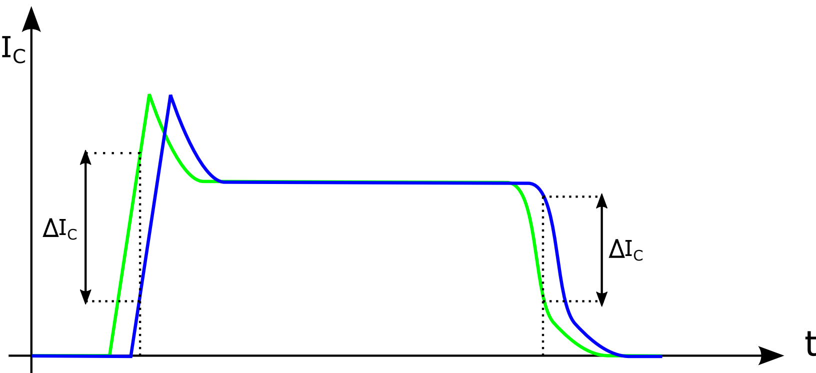


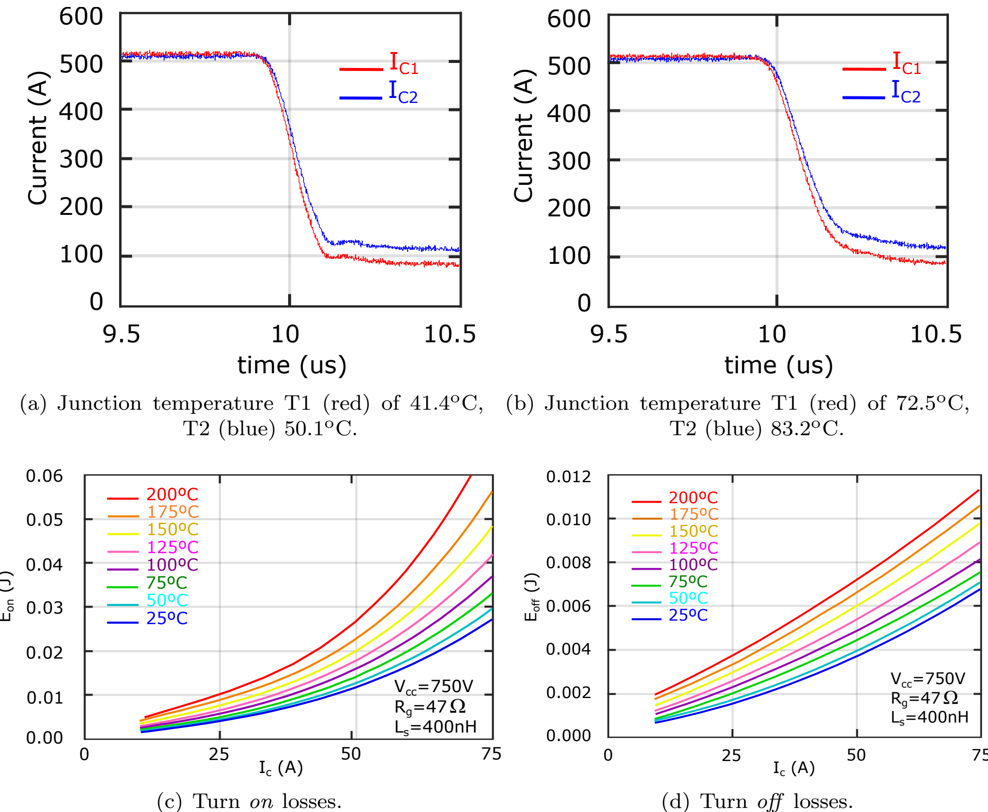
Figure 4.9: Dynamic current imbalance during turn *on* and *off*.

About the latter, in [290] a test is carried out in which a temperature difference between two parallelized IGBTs is set around 25-85°C, where the relative temperature between T_1 and T_2 (temperature of each parallelized IGBT) remains approximately fixed (8.7-10.7°C). In this test, the most relevant results are focused on the turn *off* currents, as the figures 4.10(a) and 4.10(b) show, where a temperature difference of approximately 10°C is maintained between the devices at a temperature range of 40-80°C.

It is important to highlight that current imbalances also produce imbalances of power switching losses, causing a device temperature increment, affecting the device static conditions [300]. Note that the switching losses of bipolar devices, such as IGBTs, increase with temperature (figures 4.10(c) and 4.10(d)) [297].

4.4 Control circuit: *Driver* connection

The design of the *driver* circuit gate is crucial in order to balance the current of parallel applications. For the *driver*, making a design as symmetric as possible is fundamental, since the asymmetries result in non-uniformity of the switching and, consequently, in a current imbalance. For this reason, controlling the gate resistance values (R_g), its parasitic inductances ($L_{\sigma g}$) that make up the output impedance of the *driver* (Z_g), and the gate voltage (V_{GE}) are fundamental, since they have a great influence on the current equilibrium. All these parameters are presented in the *driver* gate circuit of the figure 4.11. The use of inadequate or uncontrolled values of gate resistance or inductance may cause variations in the switching speed or variations in the gate voltage and, consequently, variations in the currents [292, 304].



(a) Junction temperature T1 (red) of 41.4°C, T2 (blue) 50.1°C.

(b) Junction temperature T1 (red) of 72.5°C, T2 (blue) 83.2°C.

(c) Turn *on* losses.

(d) Turn *off* losses.

Figure 4.10: Turn *off* process and power loss variations at different junction temperature.

4.4.1 Influence of gate impedance

When carrying out a parallelized design, the track length effect is key relevance, specially those layout connections between the *driver* and the power semiconductors. Both the switching process and the conduction state are affected by the PCB characteristics. When developing a design with asymmetries, the current imbalance increases, especially during the turn *off* process, since there are delays responsible for the current variations, which increase the losses [293].

In the literature [58, 184, 294] can be found several recommendations to reduce the imbalances, the device gates must be connected in parallel to one resistor per device and these to the same *driver* signal. In addition, the connections of each semiconductor must have the same length between *driver* and transistor

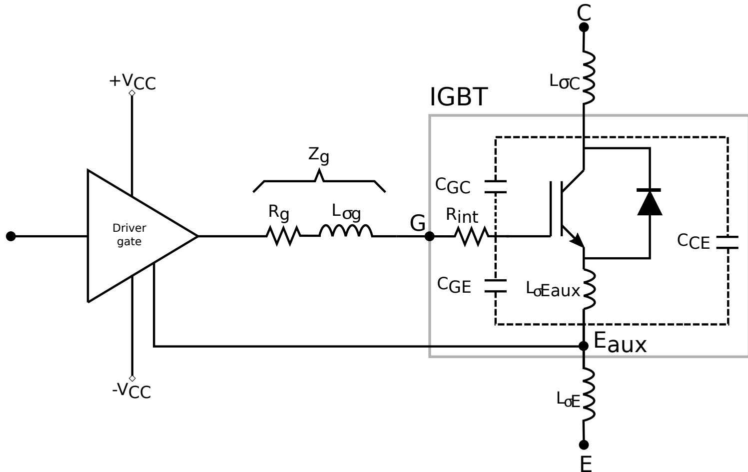
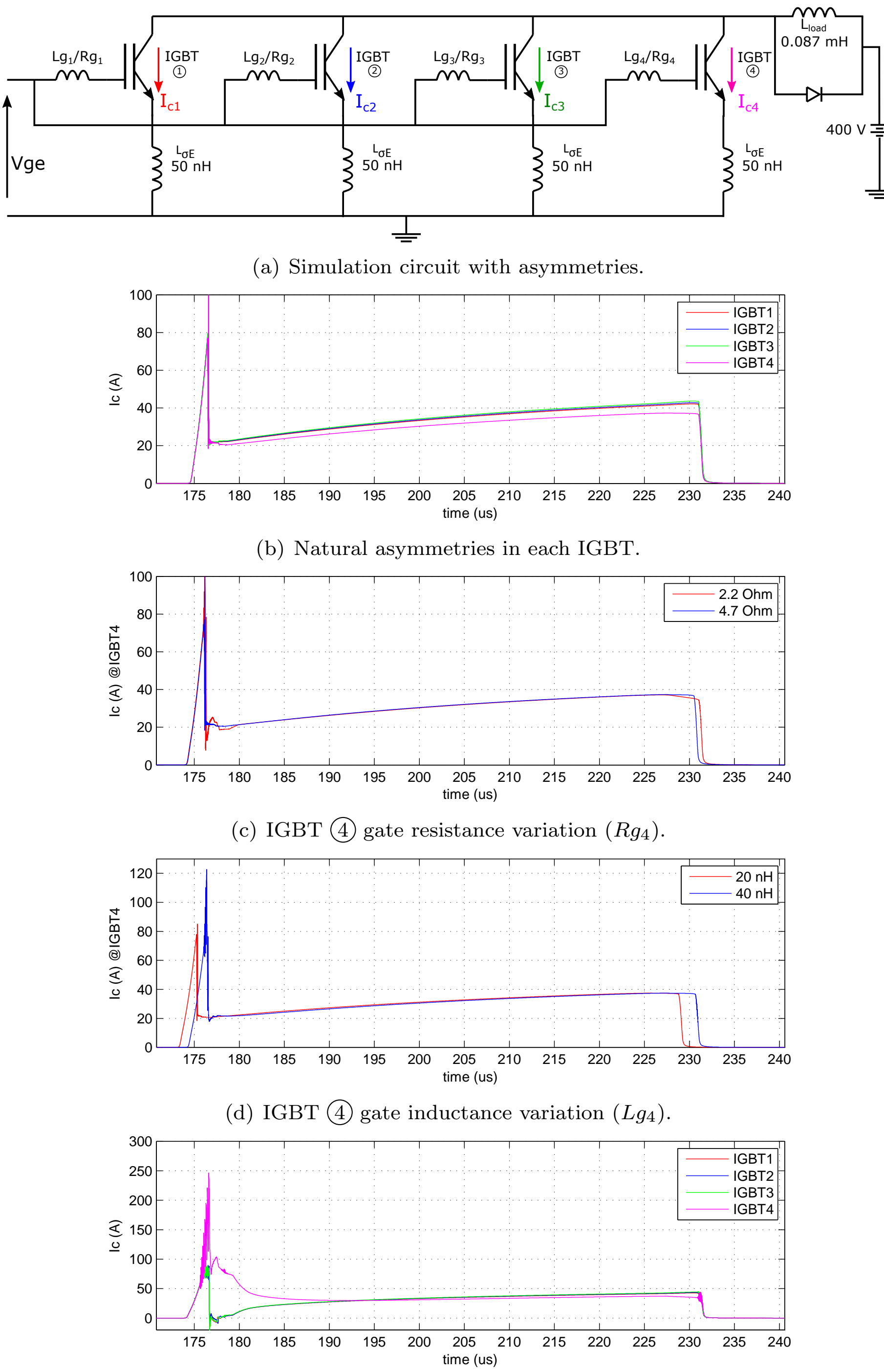


Figure 4.11: ***Driver*** **gate circuit: stray elements distribution.**

(twisted wires). It is necessary to avoid large gate impedances, making gates as short as possible, because the switches with lower resistance have a faster *on* and *off* process. However, they have the disadvantage of presenting a higher current derivative [299].

Due to the importance of the connection between *driver* and transistor gates, the following simulations try to understand the effect of asymmetries, varying the value of gate impedances in order to extract the behaviour of current. The results presented below are based on [305] (this work is considered representative with regard to this analysis). In this work, four parallelized IGBTs are used, as they appear in the figure 4.12(a). On this configuration, the gate circuit asymmetric effects that may occur in certain circumstances are studied:

1. Once the behaviour of each IGBT is known, the usage of gate resistances between IGBTs and *driver* can reduce the device deviations. By controlling the values of the resistors and the parasitic gate inductances, the voltage applied to the gate of the IGBT can be determined (4.11) - (4.12). Once the voltage is applied, the gate current is determined through the Miller capacitance (C_{gc}) and the gate-emitter capacitance (C_{ge}). If the IGBT switch to *off* state, it can produce a high dV_{ce}/dt and a current shift to C_{gc} capacitance (4.13), so a gate voltage increment and, therefore, a negative current in the gate (4.12).



(a) Simulation circuit with asymmetries.

(b) Natural asymmetries in each IGBT.

(c) IGBT ④ gate resistance variation (Rg_4).

(d) IGBT ④ gate inductance variation (Lg_4).

(e) Imbalance effects due to gate resistance (Rg) and inductance (Lg).

Figure 4.12: Asymmetries effects produce by gate connection on the current.

$$\begin{aligned} I_g > 0 : V_{ge} = V_{R_g} + V_{L_g} + V_{R_{g,int}} + V_{C_{ge}} + V_{L_e} \\ \longrightarrow V_{C_{ge}} = V_{ge} - V_{R_g} - V_{L_g} - V_{R_{g,int}} - V_{L_e} \end{aligned} \quad (4.11)$$

$$\begin{aligned} I_g < 0 : V_{ge} = -V_{R_g} - V_{L_g} - V_{R_{g,int}} + V_{C_{ge}} + V_{L_e} \\ \longrightarrow V_{C_{ge}} = V_{ge} + V_{R_g} + V_{L_g} + V_{R_{g,int}} - V_{L_e} \end{aligned} \quad (4.12)$$

$$I_{gc} = C_{gc} \cdot \frac{dV_{gc}}{dt} \approx C_{gc} \cdot \frac{dV_{ce}}{dt} \quad (4.13)$$

At the same time, the resistors must be adequate to avoid the presence of oscillations between the *driver* and the common point, as well as gate oscillations due to high frequencies [305]. If oscillations occur, they can be mitigated using special radiofrequency techniques, as RLC filters in order to dampen specific frequency components.

2. Once the natural asymmetries have been analysed for each IGBT to be parallelized, the study [305] introduces artificial elements to understand how they influence the behaviour of the circuit (figure 4.12(a)). The different tests with artificial elements added to the circuit are the following:

   ❒ Symmetrical gate resistances: the turn *on/off* behaviours are affected by small variations in the control circuit. These variations are originated on internal resistances ($R_{g,int}$) and external gate resistances ($R_{g,1-4}$) [305]. The different *on/off* gate voltage slopes produce dynamic imbalances (figure 4.12(b)) because of different voltage gate levels and delays. Moreover, the different *on/off* slopes of the IGBTs cause dynamic imbalances. These imbalances are closely related to the gate voltage, since it is heavily influenced by the IGBT turn *on* process. A high dv_{CE}/dt can cause current displacement affecting the IGBT gates and the gate current signal (4.13) [305].

   ❒ Gate resistance and inductance variation: in order to check asymmetric effects in IGBT ④ (with the higher current imbalance) gate resistance and inductance are changed and results are shown in figures 4.12(c) and 4.12(d) [305]. The figure 4.12(c) shows that a lower gate resistance produces a faster dI_c/dt, so a higher current peak. However, the asymmetric effect is very smooth. In the figure 4.12(d) can be perceived that increasing gate parasitic inductance also produces a light deviation from the original test conditions [305]. Finally, figure 4.12(e) shows that combining the effect of gate resistance and the inductance variation ($R_g = 2.2\ \Omega$ and $L_g = 20\ nH$) has higher current imbalance than the others IGBTs.

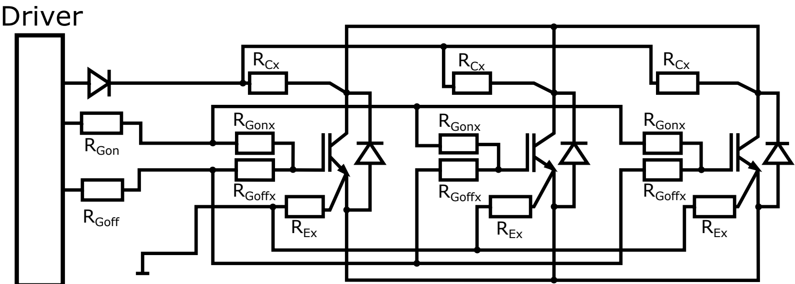


Figure 4.13: Recommended *driver* circuit for the IGBT parallelization.

4.4.2 Gate design strategies

The parallelization of powerr devices is a challenge, especially from the point of view of the gate *driver*. In many occasions, it is very complex to implement totally symmetrical designs due to the physical constraints of the gate circuit in the parallel configuration. The use of non-balanced paths for the gate signal may produce asymmetries in the switching current of the parallelized IGBTs [297]. When designing the gate connection of the IGBTs, there are two possible design strategies:

- A common gate connection for all IGBTs: this strategy substantially reduces delays and voltage levels variations, because they have a significant impact on dynamic characteristic of IGBT devices. For this reason, it is recommended a common circuit driver, as figure 4.13 shows [295]. However, the coupling between power part and control signals need to be optimized to avoid internal coupling effects between driver and power circuit [297].
- Separate gate connection for each IGBT: this technique allows to avoid coupling effects in parallel devices. However, conduction voltage levels have to be similar to prevent switching problems, since V_{CE} affects delays and operation point. For this reason, gate signal tracks, which connect each IGBT, have to be equal in all devices to avoid synchronization problems [297].

Consequently, the shared gate *driver* produces smaller power mismatches than the independent *driver* gate scenario [306], as shown in [299] (mismatch shared gate 4.5 % and independent gate 6.5 %), because the time of the gate signal is determined by the impedance of the gate connection. On the other hand, the independent trip circuits are vulnerable to the parasitic effects for each gate [300].

4.5 Power circuit: Power layout

All circuits, both driver and power layout, with parallel connections must be designed with minimum parasitic inductances and as symmetric as possible, even DC bus connection [58]. In order to achieve a symmetrical power layout, the following items must be fullfilled:

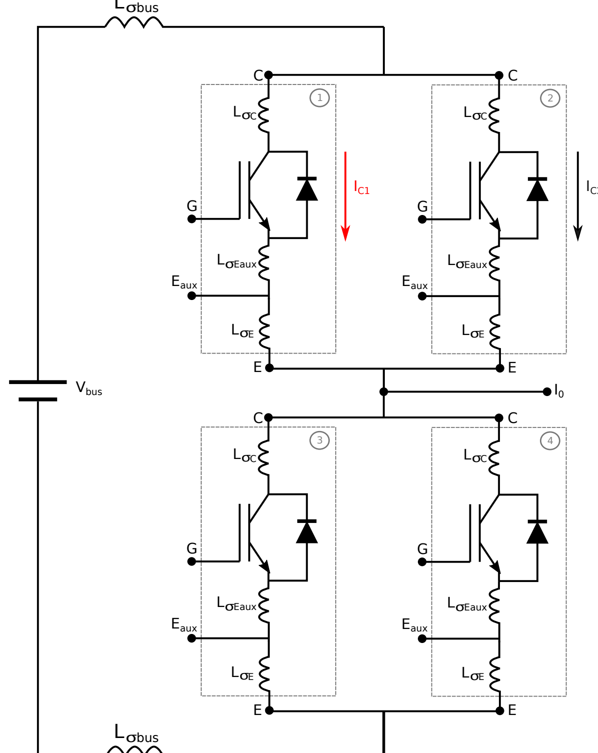
- The impedance in connections between each die or discrete semiconductor has to be identical to allow conduction and switching of current without disturbances.
- The current which flows through parallel devices should not influence in the impedance of the adjacent device [297].
- Loop inductance values and layout symmetric design have to be equal in all the power circuit.
- Parallelized power semiconductors must be as close as possible to reduce parasitic inductances [295].
- Temperature variations have to be minmized to avoid current imbalances [296].
- Internal emitter inductance effects ($L_{\sigma E_{aux}}$, with typical values of $5 - 10\ nH$), and emitter inductance ($L_{\sigma E}$, with typical values of $20 - 50\ nH$) must be analysed to obtain a low value of total parasitic inductance (L_{σ}).

The following sections give a global overview of the parasitic inductances that exist in the power circuit, as well as the effects or phenomena that influence the *driver* if a correct design is not made.

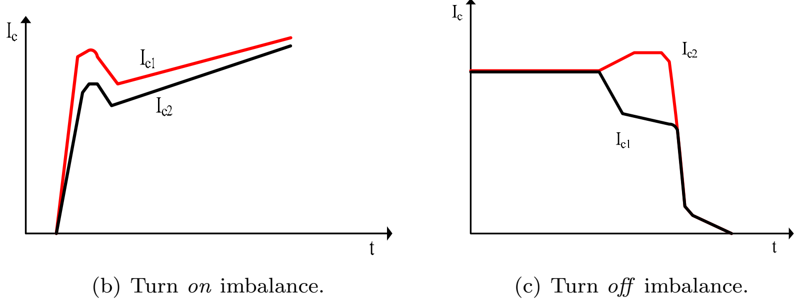
4.5.1 Parasitic inductances

All elements of the power layout design, such as DC capacitor, DC bus, mechanical interconnection and power module contribute to the equivalent parasitic impedance (Z_{σ}) of the parallel IGBTs[1]. Specifically, the inductive component of the impedance (L_{σ}) is the one more relevance. The figure 4.14(a) identifies each one of the parasitic inductances present in the switching circuit for the specific case of two parallelized IGBTs [292]. If the parasitic inductance values are different, asymmetries occur during IGBT switching causing current imbalances (figures 4.14(b) and 4.14(c)).

[1] The IGBTs are the power semiconductor used as reference in this chapter, but the concepts and ideas can be generalized for other power semiconductor technologies.



(a) Full equivalent circuit with parasitic inductances.



(b) Turn *on* imbalance.

(c) Turn *off* imbalance.

Figure 4.14: Branch of parallelized IGBT with parasitic elements and imbalance effects.

The total parasitic inductance (L_{σ}), resulting from the IGBT switching circuit, must be taken into consideration especially when carrying out a correctly balanced parallel design. The parasitic inductance (4.16) can be expressed as the sum of the external inductances of the circuit, the connections of each IGBT (4.14) and the internal inductances of the parallel IGBTs (4.15):

$$L_{\sigma_{ext}} = \sum_{n}(L_{\sigma C} + L_{\sigma E}); \qquad (4.14)$$

$$L_{\sigma_{int}} = \sum_{n} L_{\sigma E_{aux\sigma}}; \qquad (4.15)$$

$$L_{\sigma} = L_{\sigma_{ext}} + L_{\sigma_{int}} \qquad (4.16)$$

Summarising, the elements that introduce the most important parasitic inductances in the circuit current are the following (figure 4.14(a)) [58]:

- DC Bus inductance ($L_{\sigma bus}$): the analysis of this inductance is fundamental and must have the smallest possible value. This applies both to the connection of the bus capacitor and to the connection between the DC bus and the power module. In order to solve it, manufacturers of power devices make great efforts to minimize parasitic inductances, using different techniques such as a laminated DC bus structure (20 - 50 nH) [58] to balance the parasitic inductances making a series of holes on the DC bus or twisted copper tracks to get homogeneous current distributions [292].

  If the inductance value can not be reduced, snubber circuits, directly connected to the DC bus terminals of the power module, can be used to mitigate the effects of its inductance [58].

- Emitter inductance ($L_{\sigma E}$): the effects of this inductance affect both the power circuit and the *driver* circuit. Due to the fast di/dt, a voltage is added or subtracted to the gate signal (V_{ge}), which produces a feedback effect in the *driver* circuit. This effect causes an acceleration or deceleration of the process of C_{ge} capacitance charge, translating into a variation of switching times and switching losses. To minimize this effect, the devices must be equipped with a separate or auxiliary emitter control [297].

Due to the relevance of the emitter inductance, the following section analyses its behaviour.

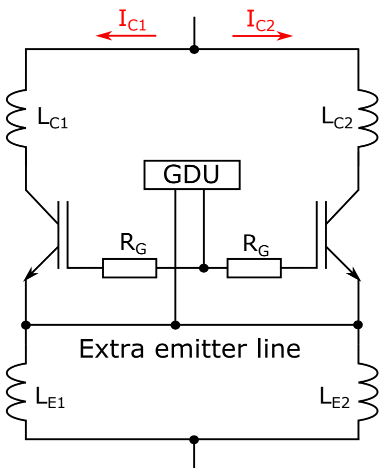


Figure 4.15: Equivalent circuit with parallel connections and its main inductances.

4.5.2 Parasitic emitter inductance ($L_{\sigma E}$)

The inductance of the switching circuit (L_σ) affects the power semiconductors on their switching *on* and *off* (generation of switching overvoltages). If the switching circuits are subjected to different inductance paths, the switching speed of the parallel IGBTs may be different, causing a dynamic asymmetry that may have higher impact than the current imbalances produced by employing parallel devices with different parameters. Even slight differences in this inductance can cause an asymmetric distribution of the switching losses and oscillations between power semiconductors [58].

The figure 4.15 shows the switching circuit with two devices in parallel with the parasitic collector and emitter inductances. When the currents I_{C1} and I_{C2} circulate through each of the IGBTs, the shared current flows through L_σ, which for this particular case is $L_{C1} + L_{E1}$ and $L_{C2} + L_{E2}$ for each IGBT, respectively. To avoid imbalances, the tracks should be as symmetrical as possible. However, even in the ideal case of having similar parasitic inductances (4.17), the difference between L_{E1} and L_{E2} causes an unbalance current [294].

$$L_{C1} + L_{E1} = L_{C2} + L_{E2} \tag{4.17}$$

Imbalances of approximately 2 % are completely acceptable without causing design problems [294]. The aforementioned imbalances are mainly due to the differences in the internal parameters presented by the IGBTs which lead, in this particular case, to a major level of static current than dynamic current [294].

In order to reduce the effect of the emitter inductance, the gate attack is carried out through the auxiliary emitter (E_{aux}), decoupling the connection of the driver with power circuit [297]. When the auxiliary emitter is used, current peaks are reduced, since the additional inductive voltage added is not applied [297]. The internal emitter inductance ($L_{\sigma E_{aux}}$) is presented when the device has the auxiliary emitter configuration. The external emitter inductance ($L_{\sigma E}$) is the inductance that appears in the connections of the IGBT emitter with the layout (figure 4.14(a))

Moreover, a combination of the internal inductance with the IGBT capacitances generates a closed loop with the *driver* circuit that can generate strong oscillations through IGBTs. Rapid changes in the emitter current induce a voltage across the auxiliary emitter inductance ($L_{\sigma E_{aux}}$). This can be counterproductive since it can influence the process of gate charge (negative feedback) or discharge (positive feedback). This is one of the most critical effects of the dynamic current distribution. Then, different examples of feedback between the power circuit and the *driver* are explained:

a) Positive asymmetric feedback (figures 4.16(a) and 4.16(e)): they show different positive feedback levels, providing that IGBT ③ has faster turn on than IGBT ①:

$$V_{ge_3} = V_{ge} + 2 \cdot V_L > V_{ge_1} = V_{ge} \tag{4.18}$$

b) Positive and negative asymmetric feedback (figures 4.16(b) and 4.16(f)): results show how IGBT ② has a positive feedback, while IGBT ③ has a negative feedback (4.19).

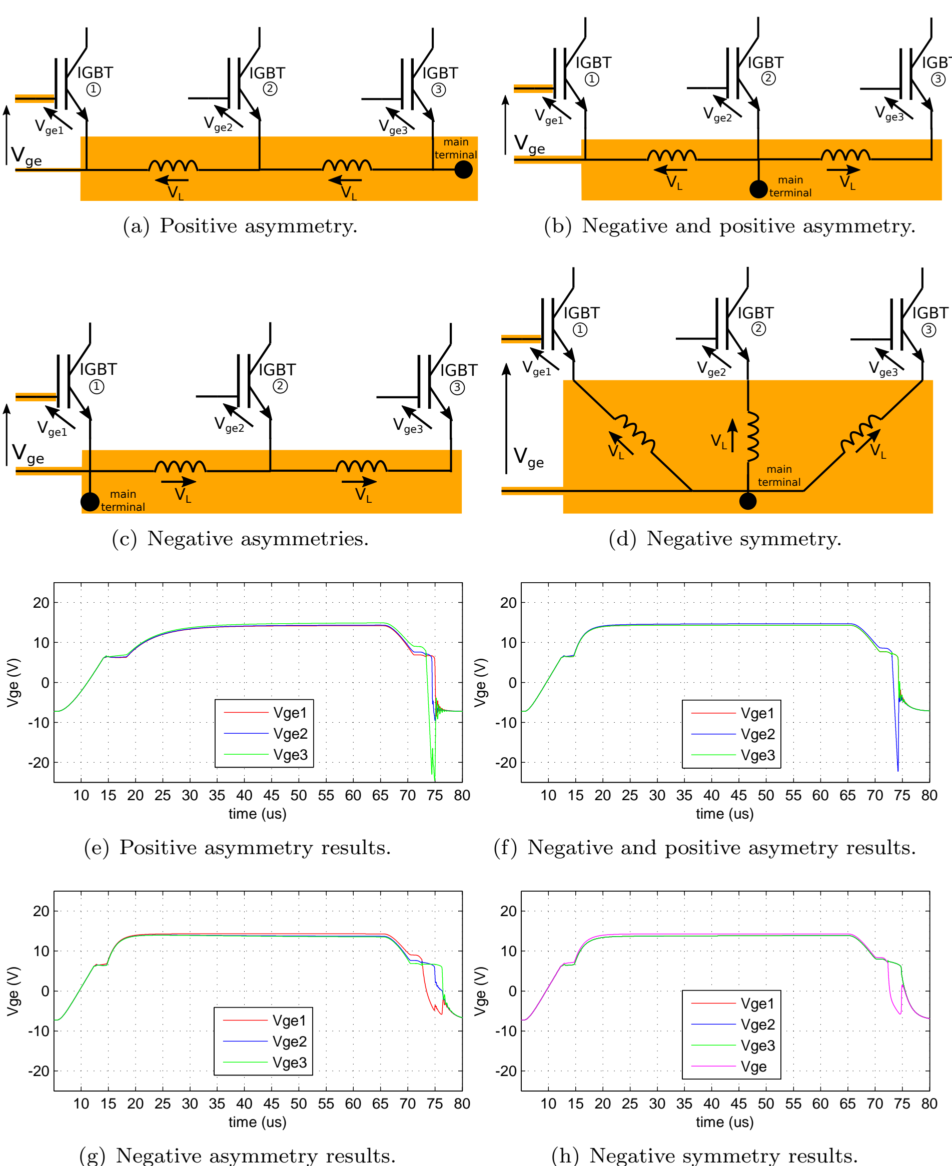
$$V_{ge_2} = V_{ge} + V_L > V_{ge} > V_{ge_3} = V_{ge} - V_L \tag{4.19}$$

c) Negative asymmetric feedback (figures 4.16(c) and 4.16(g)): different levels of negative feedback are produced, causing the IGBT ③ turns on slower than IGBT ① (4.20).

$$V_{ge_3} = V_{ge} - 2 \cdot V_L < V_{ge_1} = V_{ge} \tag{4.20}$$

d) Negative symmetric feedback (figures 4.16(d) and 4.16(h)): each IGBT has approximately the same negative feedback, allowing synchronous switching of each IGBT (4.21).

$$V_{ge_1} = V_{ge_2} = V_{ge_3} = V_{ge} - V_L \tag{4.21}$$



(a) Positive asymmetry. (b) Negative and positive asymmetry.

(c) Negative asymmetries. (d) Negative symmetry.

(e) Positive asymmetry results. (f) Negative and positive asymetry results.

(g) Negative asymmetry results. (h) Negative symmetry results.

Figure 4.16: Feedback examples between power circuit and driver.

4.6 Conclusions

This chapter summarises through literature references and circuit simulations the main tips and concepts in order to apply the parallelization of *Si* IGBTs. These devices have been taken as the semiconductor of reference, but all the ideas can be easily applied for other power semiconductors, as *SiC* MOSFETs.

With the aim to achieve a correct parallelization, the usage of devices or modules with the same or similar static and dynamic behaviour is necessary. The devices should present the same characteristic curve $V_{ce_{(sat)}}$ vs I_c, as well as the same $V_{ge_{(th)}}$, with temperature T_j. Moreover, the usage of power semiconductor with positive coefficient temperature also ease the parallel connection. This way, it is possible to reduce temperature variation $|\Delta T_{xy}|$ between devices and also reduce static current imbalance. Moreover, devices delays ($t_{d_{(on)}}$ and $t_{d_{(off)}}$), temperature (T_j) dependent, must be as equal as possible between them to avoid current dynamic imbalances. For these reasons, semiconductors or modules must belong to the same batch, which guaranties similar internal parameters and temperature variation. This tip is specially important for *Si* IGBTs which present both temperature coefficients as PT IGBTs. In the case of *SiC* MOSFETs, which have a negative temperature coefficient, is less restrictive.

In reference to driver connection circuit, it is advisable to use a common gate design in all parallel power semiconductors to reduce delays and their voltage problems, so that the gate resistance R_g and parasitic inductance $L_{\sigma g}$ values must be controlled in order to avoid current imbalances. In addition, gate oscillations can also be minimized through the control of gate stray impedance.

Moreover, the power layout requires minimize parasitic inductance effects, specially emitter parasitic inductance ($L_{\sigma E}$), since it may produce some feedback effects which imbalance, and eventually, destroy the circuit. The usage of an auxiliary emitter (Kelvin connection) for control signals helps to reduce gate impedance value and mitigate the feedbacks effects between control and power signals, which can produce device signal oscillations and EMI issues (chapter 1).

The simulation results and general concepts of this chapter show that the design must be as symmetric as possible in order to reduce imbalance effects. The application of symmetry is not trivial and is subject to multiple restrictions. However, there is a lack of information and reference solutions in order to implement correctly the symmetry concept. For this reason, in the next chapter, a design criteria to develop correctly power module is presented where parallelization and symmetry concepts are explained in more detail.

Chapter 5

Analysis and definition of the power module design criteria

5.1 Introduction

As it has been mentioned, the main scientific efforts of the HEV/EV power train industry are focused on developing architectures with improvements such as higher power density, lower conduction and switching losses, reduction of size, weight and cost, and simplification of cooling systems. In this context, the usage of WBG devices (chapter 3) instead of current *Si* IGBTs (chapter 2), acquires a higher sense in order to meet these objectives. In general, two approaches are followed by the industry to implement an automotive power converter, applying in both the parallelization technique of chapter 4:

- Discrete IGBT devices: This approach is being followed by Tesla in most of their vehicles [56], where International Rectifier discrete IGBTs (AUIR family, TO-247 package) are mounted over a power PCB. The main advantage of this approach is that the power ratings of the converter can be easily upgraded over the existing design (without significant modifications) by means of substituting the discrete devices.

- Power modules: This trend is adopted by Nissan, BMW, Audi, Toyota and Chevrolet where half-bridge or six-pack IGBT modules with their specific

Table 5.1: *SiC/Si* electric automotive inverters for HEV/EV drive systems.

Full *SiC* inverter	Power	Efficiency(1)	Power density	DC bus voltage	Refs.
EV inverter	30 kW	99.5 % peak	15 kW/l	250-800 V	[308]
EV inverter	60 kW	-	34 kW/l	400 V	[145]
EV inverter(3)	110 kVA	96.3 % mean 98.9 % peak	17 kW/l 12.4 kW/l	200-450 V	[145]
EV inverter	100 kW peak	-	34 kW/l	400 V	[309]
EV inverter	80 kW	99. %	-	800 V	[310]
EV inverter	60 kW	92.3-99.1 %	160 kW/l	800 V	[311]
EV inverter	120 kW	96.8-99.3 %	160 kW/l	800 V	[311]
EV inverter	88 kW	-	21.5 kW/l	900 V	[312]

Commercial *Si* inverter	Power	Specific power(2)	Power density	DC bus voltage	Refs.
Motor inverter for 2004 Prius	50 kW	5.68 kW/kg	5.75 kW/l	200 V	[313]
Motor inverter for 2007 Camry	70 kW	9.33 kW/kg	11.67 kW/l	250 V	[313]
Motor inverter for 2008 LS 600h	110 kW	14.86 kW/kg	17.19 kW/l	288 V	[313]
Motor inverter for 2010 Prius	60 kW	16.67 kW/kg	11.11 kW/l	200 V	[313]
Motor inverter for 2012 Nissan Leaf	80 kW	4.9 kW/kg	5.7 kW/l	380 V	[314]

Table notes:
(1) Analysed literature does not provide specific power data.
(2) Consulted commercial solutions do not provide efficiency data.
(3) 1200 V inverter based on half-bridge modules.

layout and cooling technologies [56] are developed. In the case of *SiC* MOSFET power modules, this technology will be adopted for next generation vehicles. However, Tesla has integrated a full *SiC* power converter with 24 1-in-1 power modules over a pin-fin heatsink in his Model 3 vehicle [307], validating WBG technology in automotive market.

It can be said that major automotive OEMs have generally adopted power module technology to constitute the traction inverters. In this context, table 5.1 summarizes various *SiC* and *Si* automotive inverters, highlighting some of their more relevant features.

Bearing in mind that the preferred power conversion topologies for HEV/EV applications would be based on the half bridge branch configuration (chapter 1), the power stage could be modular, i.e. made of independent or single phase modules, or and standalone power module that groups all the required converter phases. Regardless of the selected solution, both approaches share the same constituting elements.

In the present thesis, it has been appreciated that in both scientific and industrial/commercial literature there is no exhaustive and detailed information about

the design of power modules. In fact, there are scientific works that address local problems of power modules such as substrate configuration, interconnection technologies, routing of gate control signals and others. In the case of the industrial/commercial literature, this information is more restricted, being limited in most cases to the information reported in the datasheets and application notes. This information only adheres to the electrical, mechanical and thermal parameters of the power module, which can be understood as a black box or a single entity without reporting any information about its design and constituent parts.

That is why in this chapter prior to focusing on the automotive *SiC* (MOSFETs and JBS diodes) power module design process, it is important to describe and understand such constituting elements. In general, it can be stated that a bare die based power module can be divided into five key parts (figure 5.1), i.e., mechanics (encapsulation), substrate (stack-up), gate attack (for control and monitoring signals), power layout (for the power conversion) and terminals (interface of power and control). Although, apparently, such parts can be considered separated blocks, they are interrelated, and the design of each one affects the others. Thus, a global vision of the problem is required when designing the whole module. In the following sections, the most significant aspects of such fundamental parts and design criteria are developed.

5.2 Power module mechanics

The mechanical part of the module (figure 5.1-A) is related to the particular encapsulation (standard or custom) and to the layout of the power connectors and auxiliary terminals (control and monitoring signals). This part imposes the main constraints on the design of the rest of the elements, as it sets the available space and terminals placement [315].

There is a wide portfolio of standard cases in the market. Some well-known transport solutions such as PrimePACK modules rely on the placement of the power connectors in the central part of the module, while other solutions place such terminals on the edges [58] (figure 5.2). Particularly, the most of current *Si* based automotive grade power modules such as the Infineon hybridPACK and Semikron SKIM 606 and 909 families adopt the border power terminal placement, as it allows to use integrated MKP-type DC-link capacitors, significantly reducing the parasitic inductances of the capacitor/module group [316]. Such modules assemble the driver board on top of the power module, providing a compact solution.

Extreme thermal variations (ΔT_{vj}) within the module during vehicle driving

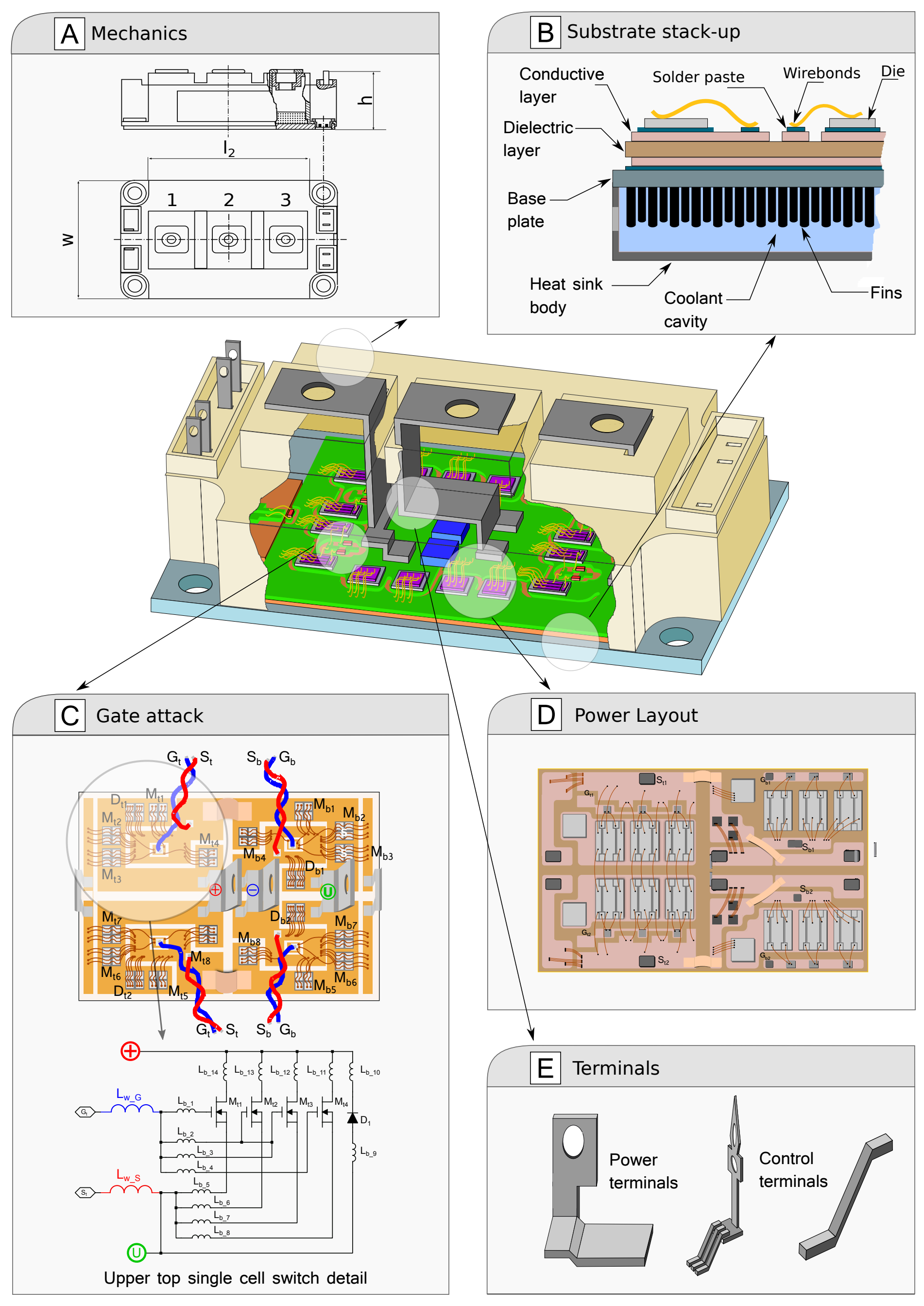


Figure 5.1: Main parts that constitute a bare die based power module.

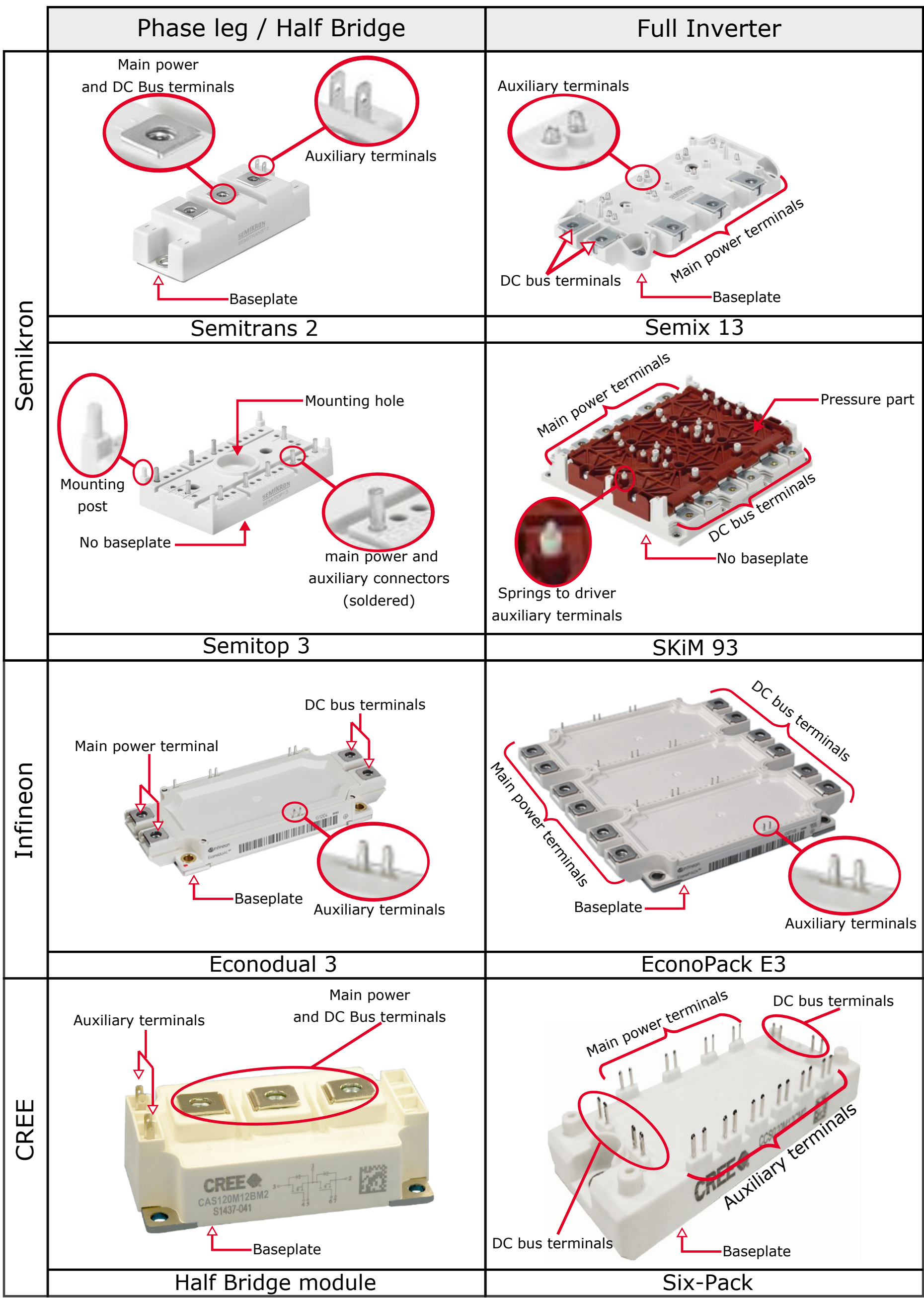
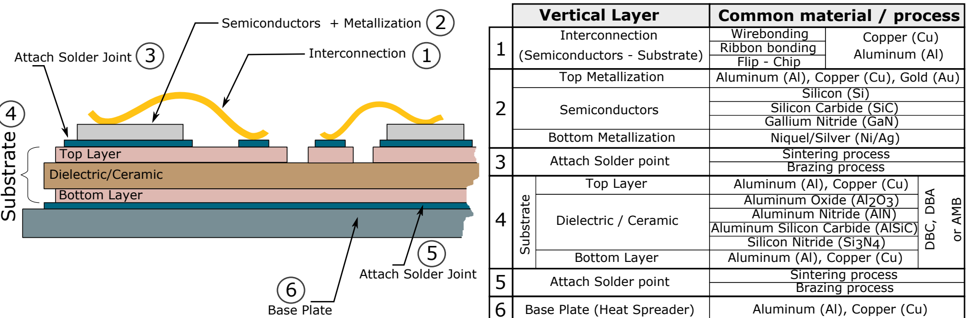


Figure 5.2: Examples of standard power module encapsulations.



		Vertical Layer	Common material / process	
1		Interconnection (Semiconductors - Substrate)	Wirebonding	Copper (Cu) Aluminum (Al)
			Ribbon bonding	
			Flip - Chip	
2		Top Metallization	Aluminum (Al), Copper (Cu), Gold (Au)	
		Semiconductors	Silicon (Si)	
			Silicon Carbide (SiC)	
			Gallium Nitride (GaN)	
		Bottom Metallization	Niquel/Silver (Ni/Ag)	
3		Attach Solder point	Sintering process	
			Brazing process	
4	Substrate	Top Layer	Aluminum (Al), Copper (Cu)	DBC, DBA or AMB
		Dielectric / Ceramic	Aluminum Oxide (Al_2O_3)	
			Aluminum Nitride (AlN)	
			Aluminum Silicon Carbide (AlSiC)	
			Silicon Nitride (Si_3N_4)	
		Bottom Layer	Aluminum (Al), Copper (Cu)	
5		Attach Solder point	Sintering process	
			Brazing process	
6		Base Plate (Heat Spreader)	Aluminum (Al), Copper (Cu)	

Figure 5.3: General substrate structure for a power application.

profiles have also a great impact in the design of the case and connectors. For example, a vehicle that is parked in extreme weather conditions (bellow -20°C) preheats its power converter cooling system to its nominal coolant temperature (of between 65°C-85°C) and, during driving, the junction temperature T_{vj} reaches high values. When the vehicle stops all the systems cool again. As a result, an extreme ΔT_{vj} of 150°C (or greater) can be easily generated. This phenomena affects the joints between elements of different materials with different dilatation coefficients. If the module design does not take all this into account, premature failures can occur within the module, although the maximum junction temperature has not been reached. In this sense, the design must ensure a minimum number of such extreme operation cycles. The innovative solution provided by Semikron for the SKIM family can be highlighted, where the connectors and the plastic elements are solderless and are hold in their position by applying an specific pressure on the module screws [58, 317].

5.3 Substrate stack-up: thermal behaviour

The substrate (figure 5.1-B) provides a surface where power semiconductors and other components, such as passive elements and control and power terminals, are placed and interconnected allowing their electrical connection and isolation with a good thermal conductivity [318]. A variety of technological solutions can be found in the literature and the industry, specially when WBG devices are incorporated, being good examples various advanced solutions such as the SKiN structure, the SiPLIT solution, and other embedded structures of multiple layers [319–321]. All the aforementioned require non-conventional materials, processes and design concepts, incorporating novel attach materials, interconnections and advanced heat transfer cooling systems [322, 323]. Considering that the automotive industry is cost sensitive, standard solutions (i.e., inorganic substrates) could be preferred [324].

Various types of inorganic substrates can be found depending on the assembled techonology employed between conductive and dielectric (ceramic) layers. The most common solutions are the Direct Bonded Copper (DBC) and the Direct Bonded Aluminum (DBA) substrates, where the union between conductive and ceramic layers is an eutectic bond. Active Metal Brazing (AMB) can be also highlighted, where copper and ceramic layers are joined by a brazing process [324]. For illustration purposes, figure 5.3 shows the interconnections and layers generally present on a DBC substrate based design [184, 325]. The most common interconnection technology is the wirebonding [326], even though other solutions such as ribbon bonding and flip-chip can be also found to connect the semiconductors with the top layer of the substrate. On the other hand, semiconductors have metallization layers on both surfaces in order to assembly the top surface with the wirebondings and the bottom surface with the substrate. Finally, it is also important to point out that the attaches between semiconductors-substrate and substrate-base plate are based on sintering or brazing processes [327].

All these substrate layers (figure 5.3) determine the vertical thermal behaviour between the power semiconductors and the base plate. The material of each layer must have a high thermal conductivity (λ) to achieve a low thermal resistance (R_{th}), which is given by [184, 319, 328]:

$$R_{th} = \frac{d}{\lambda \cdot A}, \tag{5.1}$$

where d and A are the thickness and the area of the layer, respectively. On the other hand, the equivalent thermal resistance $R_{th_{subs}}$ substrate is the sum of the R_{th} of each layer (figure 5.3):

$$R_{th_{subs}} = R_{th_1} + R_{th2} + R_{th_3} + ... + R_{th_N}. \tag{5.2}$$

Regarding mechanical aspects, the thermal expansion coefficients (CTE or α) of the different materials that constitute the substrate (5.3) are relevant parameters, as they indicate the dilatation/contraction of materials due to temperature variations. Such coefficients must be as close as possible in order to prevent mechanical fatigue between layer, which could significantly reduce the lifetime of the power module [184, 319].

$$\alpha = \frac{\Delta L}{L_0 \cdot \Delta T}, \tag{5.3}$$

where L_0 is the overall length of the material, ΔL is the linear deformation with respect to L_0 and ΔT is the temperature variation with respect to temperature from which L_0 has been determined.

5.4 Gate attack: control signals

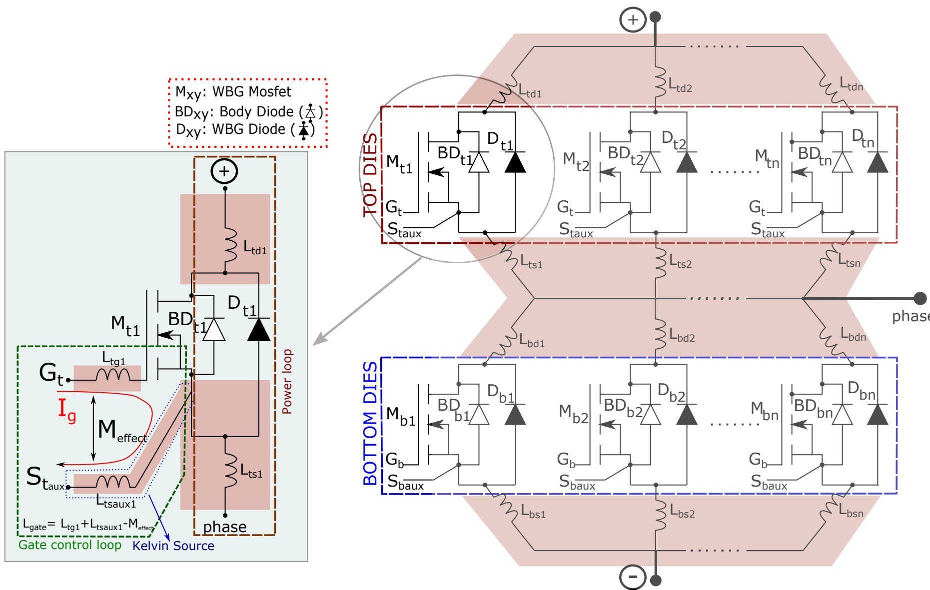
The elements that constitute the gate attack (figure 5.1-C) manage and distribute the control signals that drive the power transistors. In modules with more than one parallelized power semiconductor per switch. (figure 1.3), imbalances in the gate control signals can be produced [329]. Such imbalances are generated, among other things, due to different stray inductances between gate control loops (figure 5.4(a)), whose effects produce turn *on/off* delays, and also variations of power losses among paralleled semiconductors. All this can produce uneven current distributions among the paralleled elements, leading to possible hot spots and thermal runaway which, in some situations, could produce module failures [330–332].

Other significant problem produced by an inadequate gate attack design is the generation of high electromagnetic interferences (EMI). This aspect is more relevant when *SiC* devices with high speed commutation capabilities are used instead of slower *Si* devices. As a solution, minimizing and matching gate loops [333] decreases such harmful electromagnetic interference (EMI) effects [161]. Thus, an adequate gate attack design must be carried out. As a general rule of thumb, it can be said that control signal tracks must be as short as possible to reduce equivalent parasitic impedance of gate loops. However, more specific issues regarding the gate attack design must be considered in order to achieve an adequate solution:

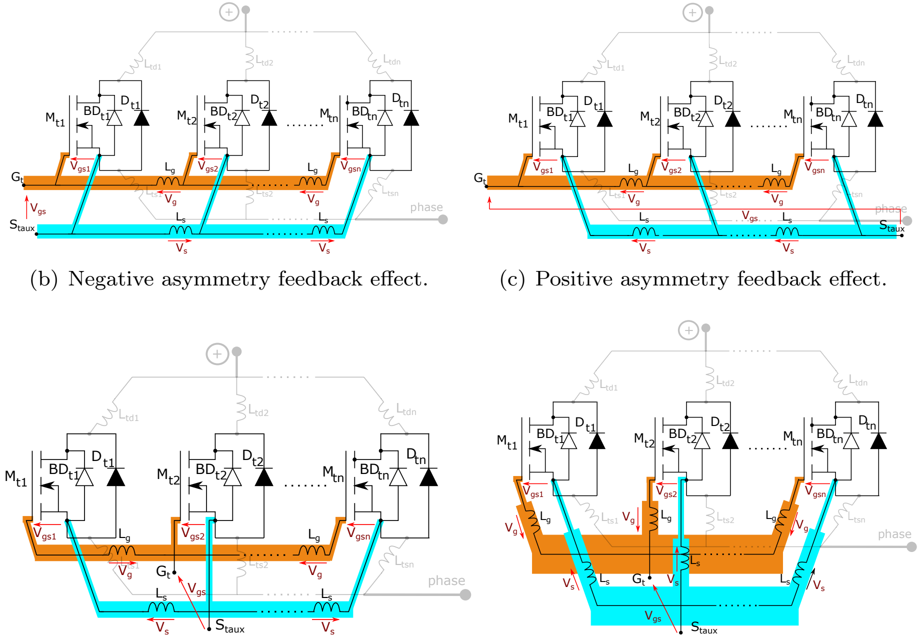
- ❐ The power and gate control loops must be independent in order to avoid feedback effects. For that reason, an auxiliary connection S_{taux} (figure 5.4(a)) is required to control the commutations of the transistors [329, 334–336]. This type of connection is known as Kelvin connection. The control signals, which are applied between the transistor gate (G_t) and source (S_{taux}) contacts, have their own tracks with a low parasitic impedance, being decoupled from the power signals, specially from the stray impedance L_{ts1} (source inductance) of the power loop (figure 5.4(a)).
- ❐ The control signals are differential, consisting on two tracks, gate and source (figure 5.4(a)). These tracks must be as close as possible between them, reducing the length of the gate loop, and improving their mutual coupling effect. All these reduces the parasitic gate loop inductance (5.4), improving the robustness of the differential signal to external noise sources (EMI) [335, 337].

$$L_{gate} = L_{tg1} + L_{tsaux1} - M_{effect}, \tag{5.4}$$

where L_{gate} is the whole inductance of the gate loop, L_{tg1} is the equivalent



(a) Half-Bridge of n semiconductors in parallel with the detail of gate loop.



(b) Negative asymmetry feedback effect.

(c) Positive asymmetry feedback effect.

(d) Negative-positive asymmetry feedback effect.

(e) Negative symmetry feedback effect.

Figure 5.4: Gate current loop and feedback effects.

inductance of the gate track, L_{tsaux1} is the equivalent inductance of the auxiliary track, and M_{effect} is the mutual coupling effect between both tracks. It is important to consider that the inductance value of transistor gate track L_{tg1} (which can produce voltage drops in the control signals and oscillations that are able to produce unexpected turn *ons* [338]) must be minimized [335].

- Each paralleled transistor (figure 5.4(a)) must have its own gate control loop. The gate tracks of all the paralleled devices must have the same length and width to have an equal stray impedance. This is of paramount importance to obtain a good turn *on* synchronization between devices[1]. Thus, a symmetrical gate attack design should be followed [329, 339, 340]. The next examples summarise various feedback effects over gate attack depending on the specific parasitic inductances derived from given layouts [341, 342]:

  (a) When the gate (G_t) and source (S_{taux}) control terminals are placed one next to the other in one side of the switch (figure 5.4(b)), a negative feedback effect is introduced in the gate signals. As a result, transistor 1 turns *on* faster than transistor n, as:

$$V_{gsn} = V_{gs} - n \cdot (V_g + V_s) < V_{gs2} = V_{gs} - (V_g + V_s) < V_{gs1} = V_{gs}, \quad (5.5)$$

  where V_{gsj} is the gate-source voltage of the transistors, being $j = \{1, 2...n\}$ and n the number of paralleled devices per switch, V_g is the voltage drop of the equivalent gate inductance and V_s is the voltage drop of the equivalent source track inductance.

  (b) When the G_t and S_{taux} terminals are located in the opposite sides of the switch (figure 5.4(c)) and the gate track equivalent inductance (L_g) is significantly smaller than the source track equivalent inductance (L_s), a positive feedback effect is generated in the gate signals. As a consequence, transistor n turns *on* faster than transistor 1, as:

$$V_{gsn} = V_{gs} - n \cdot V_g > V_{gs2} = V_{gs} - V_g - (n-1) \cdot V_s > V_{gs1} = V_{gs} - n \cdot V_s. \quad (5.6)$$

[1] If the paralleled semiconductors do not switch *on* at the same instant, there is a small period of time along which the whole phase current is shared by less semiconductors than expected, leading to overheating.

(c) When G_t and S_{taux} are located in the center of the switch (figure 5.4(d)), a negative and positive feedback effect are simultaneously generated in the gate signals. In this situation, transistor 2 turns *on* faster than transistor 1 and n, as:

$$V_{gs2} = V_{gs} > V_{gs1} = V_{gs} - (V_g + V_s) > V_{gsn} = V_{gs} - n \cdot (V_g + V_s), \quad (5.7)$$

where $n \cdot (V_g + V_s) >> (V_g + V_s)$.

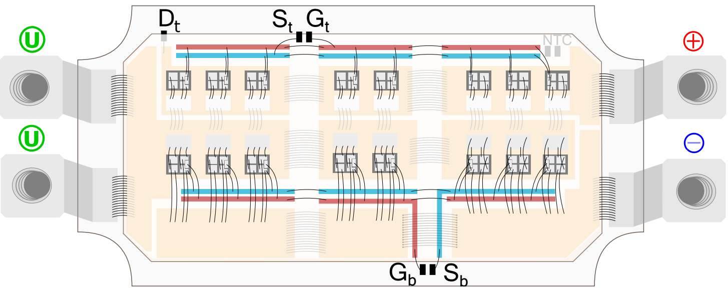
(d) When each parallel transistor has its own gate loop connected to gate-source control terminals in a symmetrical distribution to match the parasitic inductances (figure 5.4(e)), a negative feedback effect is produced in the gate signals, but all the transistors turn *on* at the same time, as:

$$V_{gs1} = V_{gs} - (V_g + V_s) = V_{gs2} = V_{gs} - (V_g + V_s) = V_{gsn} = V_{gs} - (V_g + V_s). \quad (5.8)$$

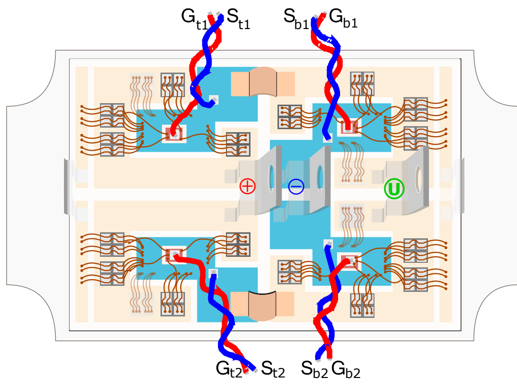
It becomes clear that this should be the design target that should be followed by the power module designer. However, a perfect symmetry is not always feasible, because the mechanical constraints of the power module may not allow to perfectly match the desired gate attack layout.

Once the ideal design criteria have been shown, these concepts can be implemented in different ways. The following three real industrial examples are the mainly commercial implementations of gate attack that will be analysed, focusing on the particularities of the design concepts carried out by each designer team. Such solutions can be summarized as:

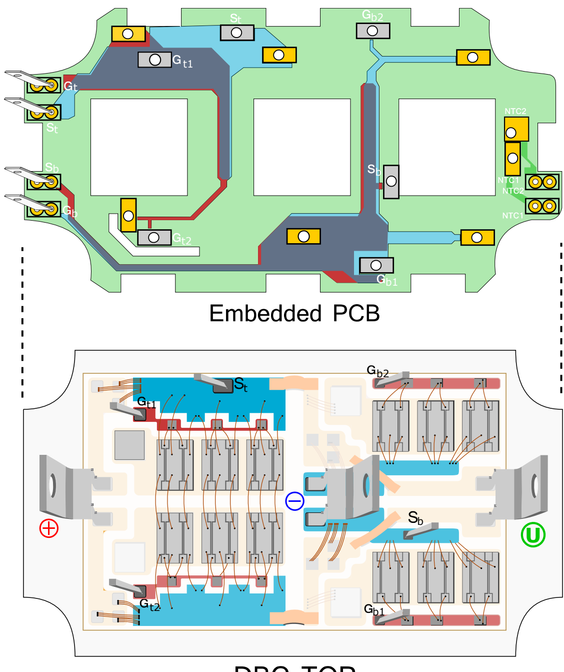
1. **Gate control signals over the power layout area.** In this solution, gate control loops (gate and source tracks) are positioned over the conduction layer of the substrate (power layout), i.e. the first layer of the DBC (figure 5.5(a)). The power and gate loops share the same substrate layer which may introduce interferences through the coupling between the power and control signal tracks [343]. The main drawback of this alternative is that the power module has an specific routing area, defined by the mechanical constraints, where a variety of components such as the power semiconductors, control and power terminals, and passive elements (i.e. gate resistances to protect parallel *SiC* MOSFETs) must be assembled. Consequently, the routing area that is exclusivelly dedicated to the power layout is reduced. Additionally,



(a) Gate signals over power layout.



(b) Gate signals with twisted wires.



(c) Gate signals through PCB embedded.

Figure 5.5: Different gate attack options in commercial half-bridge power modules.

the design routing process becomes more complicated, since there are more electrical connections in a single surface (i.e. the number of wire bonding connections are increased in order to make all the electrical connections).

As a conclusion, it can be stated that this solution increases the total parasitic impedance of the power module, since the area dedicated to the power signals is reduced [344].

2. **Gate control signals through twisted wires connected to the power layout.** This solution allows to use the full DBC area for power connections, overcoming the problems generated by the previous design example. Wires (control signals) can be connected close to the transistor control contacts (figure 5.5(b)), reducing the parasitic impedance of the gate loop [58]. All the required wires are manufactured with the same length, avoiding previously explained imbalance problems. The twisted configuration provides a reduction of the gate loop stray inductance L_{gate} because the wire coupling effect M_{effect} is greater, as it can be seen from (5.4). This twisting also provides a higher robustness against EMI (table 1.3).

   However, this solution does not allow to mount protection circuits directly in the gate loops, because the passive and active components (i.e. capacitors, resistances and diodes) required for such protections only can be implemented on the DBC, which reduces the power signals area and increases the design complexity.

3. **Gate control signals routed through an embedded PCB.** This option increases the degrees of freedom of the design (figure 5.5(c)), because the gate control loop protections (or other additional circuitry) could be mounted over the power module in the embedded PCB [339, 345] . The embedded PCB can be connected in vertical with the transistor gate-source contacts, minimizing the gate loop [335, 345].

   This embedded PCB based design leads to a multilayer structure, where the parasitic impedance (L_{gate}) decreases as the coupling effect (M_{effect}) is increased in the gate-source loop (opposite current directions). Using symmetric strategies for the gate-source tracks together with wide track areas, round squares and anti-copper pours, it is feasible to balance the currents of each paralleled gate transistor [329]. Finally, it is also possible to mount capacitors that reduce the track between the gate-source connection (limiting the current circulating through the gate).

5.5 Power layout: power signals

The power layout (figure 5.1-D) constitutes the larger area of DBC (substrate) from which the high currents flow. As the switches are constituted by various paralleled dies, the design of the power layout should be conducted in a way that such circulating currents become balanced through all the paralleled devices. This arrangement improves the power module lifetime, performance and efficiency [346–349]. Taking all the latter into account, the power layout should be designed according to the following steps:

❒ The characteristics of the selected power semiconductor must be previously analysed in order to understand how they behave in parallel. Differences in parameters such as conduction resistance (R_{dson}) and threshold voltage (V_{th}) of paralleled dies can introduce significant current imbalance problems [341, 350–352]. In order to reduce such deviations, it is highly recommended to use devices with the positive thermal coefficient and same bare code [184].

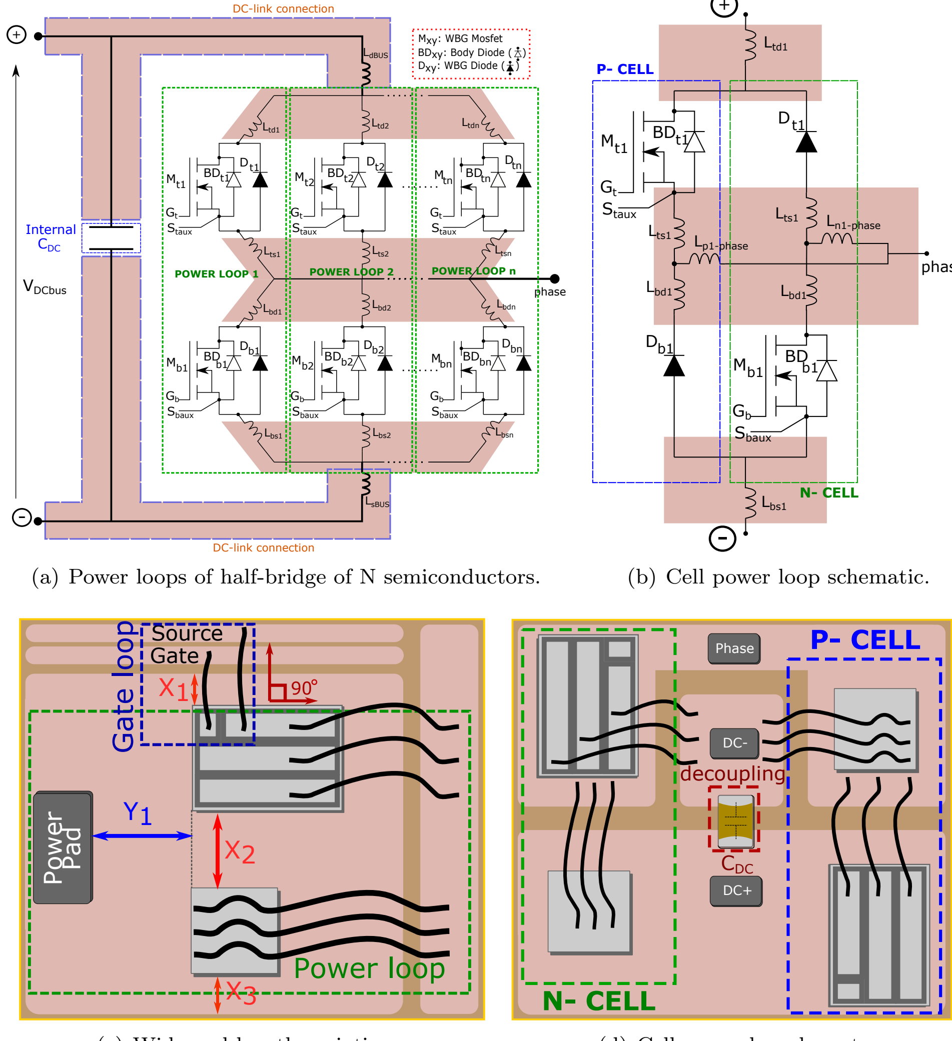
❒ The available space is one of the most significant constraints during the power layout routing process. In general, the less devices to place, the easier is the routing process, because there is more space available to balance the tracks between the power semiconductors (power loops, figure 5.6(a)) [353].

  A *SiC* MOSFET based half-bridge with a given blocking voltage and current handling capability can be designed in a variety of ways. For example, the number of required dies can be reduced by using the body diodes of the MOSFET dies instead of external *SiC* JBS diodes. However, this approach reduces the efficiency of the module, as the resistance of the body diode is higher than of the JBS diode.

  When using external *SiC* diodes, the routing process becomes more complicate, but overall efficiency can be further improved because *SiC* MOSFETs and *SiC* JBS diodes could be placed close together, forming a switch cell with a low stray inductance (figure 5.6(b)) [354, 355].

❒ In order to configure the electrical connections, the position and orientation of power semiconductor dies over the DBC layer (including their contacts, i.e. gate, drain and source for *SiC* MOSFETs) must be considered [344]. A convenient placement allows to cancel electromagnetic fields between the power and gate loops. For example, wirebonding based electrical connections between control (gate-source) and power (drain-source) contacts must be perpendicular to avoid coupling (figure 5.6(c)) [335, 356].

❒ Before beginning to route the power layout connections, the areas that provide electrical insulation (clearance and creepage areas) must be defined to



(a) Power loops of half-bridge of N semiconductors.

(b) Cell power loop schematic.

(c) Wide and length variations.

(d) Cell power loop layout.

Figure 5.6: Power loop device interconnection and stray inductance variation.

avoid possible short circuits. For this, it is important to consider the operating voltage, temperature and environment of the power application. The insulation area will depend on the pollution degree ratings of the specific application, which depends on the amount of dryness and condensation of the environment [357, 358].

- The electrical connections between the parallelized power loops (figure 5.6(a)) must be defined. At this design stage, the total stray inductance of each power loop (L_{sw}) must be balanced (symmetric design) and reduced between the devices and the DC-link [334, 350, 352, 359, 360]. If a perfect symmetry is achieved, the total stray inductances of each power loop is:

$$\begin{aligned} L_{sw1} &= L_{td1} + L_{ts1} + L_{bd1} + L_{ds1} = \\ = L_{sw2} &= L_{td2} + L_{ts2} + L_{bd2} + L_{ds2} = \\ = ... = L_{swn} &= L_{tdn} + L_{tsn} + L_{bdn} + L_{dsn}, \end{aligned} \tag{5.9}$$

  where L_{td} and L_{bd} are, respectively, the top and bottom equivalent parasitic inductances of drain connections, and L_{ts} and L_{bs} are, respectively, the top and bottom equivalent parasitic inductances of source connections subject to the following conditions:

$$\begin{aligned} L_{td1} &= L_{td2} = ... = L_{tdn}, \\ L_{ts1} &= L_{ts2} = ... = L_{tsn}, \\ L_{bd1} &= L_{bd2} = ... = L_{bdn}, \\ L_{bs1} &= L_{bs2} = ... = L_{bsn}. \end{aligned} \tag{5.10}$$

  However, in practice it is not possible to meet a perfect match, but the design should try to approximate, as much as possible, to the result indicated in (5.9)[1].

- For each single power loop, the connection between top and bottom devices must be defined to generate a power loop unit with the lowest L_{sw} possible. There are a great number of posibilities to connect top and bottom devices [336], among them, the cell or split option is generally adopted to achieve this goal [335, 352, 353, 361].

  Figures 5.6(b) and 5.6(d) show the connections between a top *SiC* MOSFET and a bottom *SiC* JBS diode (P-Cell), and viceversa (N-Cell), following the cell concept. This configuration produces a reduction of L_{sw}

[1]This expression indicates the symmetry in terms of parasitic impedances within a half-bridge module. In practice, the current flows through top and bottom level of different half-bridge modules, the current cannot flow through top and bottom level of the half-bridge.

because the physical switching routing is shorter [335, 340, 350]. The output (phase) inductance is increased, but this does not produce a drawback effect, because the load (electric machine) has a significantly higher inductive value.

❒ Adjusting the track dimensions of the switching loops can also help to reduce the stray impedance, because the parasitic inductance of the power layout depends on the width and length of the tracks [335, 336]. In this context, figure 5.6(c) illustrates the effects produced when changing track dimensions:

- If X_1, X_2 and X_3 (specially X_2) distances are increased, a reduction of the parasitic inductance of the area is achieved, since the power loop is widen.
- Increasing the length Y_1 increases the power loop stray inductance, since the distance between the power terminal and the semiconductors is increased.

❒ The application of symmetric design concepts help to balance the tracks of the electrical connections, obtaining similar parasitic impedances [336], providing currents flowing in opposite directions (which helps to reduce the parasitic inductances) [334, 335].

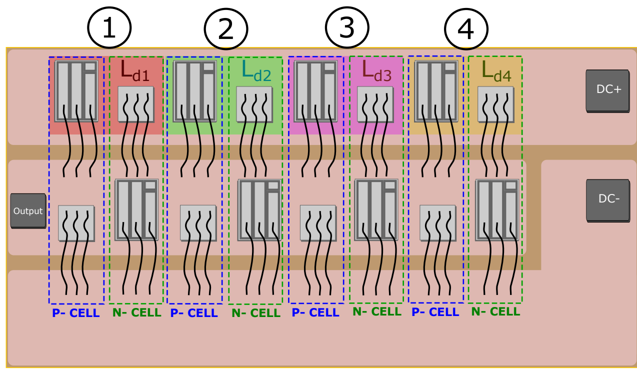
For example, if an asymmetric design (figure 5.7(a)) is conducted, unequal lengths between power semiconductors and terminals are obtained, since the equivalent parasitic inductances between the positive main terminal and the switching cells (L_{DC+1}, L_{DC+2}, L_{DC+3} and L_{DC+4}) are:

$$\begin{aligned} L_{DC+1} &= L_{d1} + L_{d2} + L_{d3} + L_{d4} \neq \\ \neq L_{DC+2} &= L_{d2} + L_{d3} + L_{d4} \neq \\ \neq L_{DC+3} &= L_{d3} + L_{d4} \neq \\ \neq L_{DC+4} &= L_{d4}, \end{aligned} \tag{5.11}$$

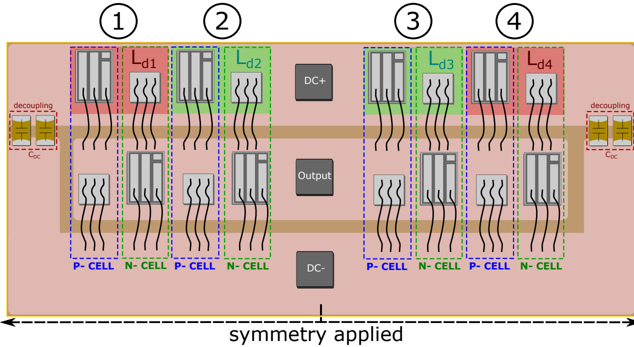
where L_{d1}, L_{d2}, L_{d3} and L_{d4} are the equivalent parasitic inductances of each switching cell in drain connection.

The previous can be greatly improved applying the concept of symmetry over one dimension [361] (figure 5.7(b)), where:

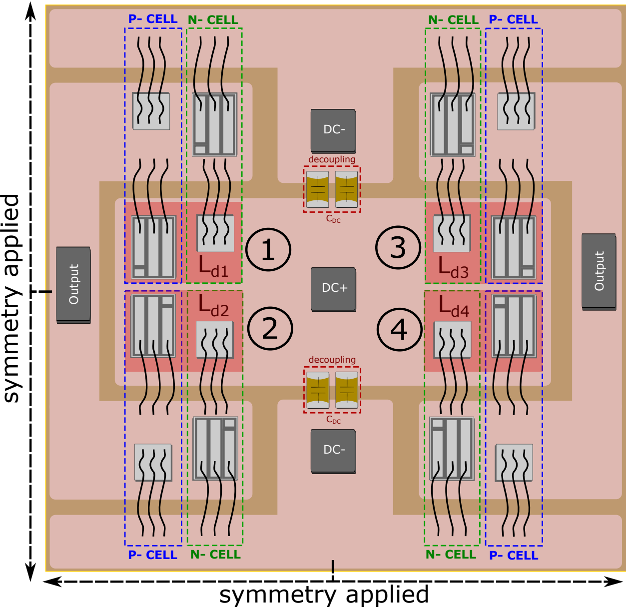
$$\begin{aligned} L_{DC+1} = L_{d1} + L_{d2} = L_{DC+4} = L_{d3} + L_{d4} \neq \\ \neq L_{DC+2} = L_{d2} = L_{DC+3} = L_{d3}. \end{aligned} \tag{5.12}$$



(a) Asymmetric design.



(b) Symmetry applied in one dimension.



(c) Symmetry applied in two dimensions.

Figure 5.7: Examples of applying symmetry over a DBC design.

The symmetry concept can be also applied in two dimensions [361], as shown in figure 5.7(c), improving the balance results and making a scalable power layout, where:

$$L_{DC+1} = L_{d1} = L_{DC+2} = L_{d2} = L_{DC+3} = L_{d3} = L_{DC+4} = L_{d4}. \quad (5.13)$$

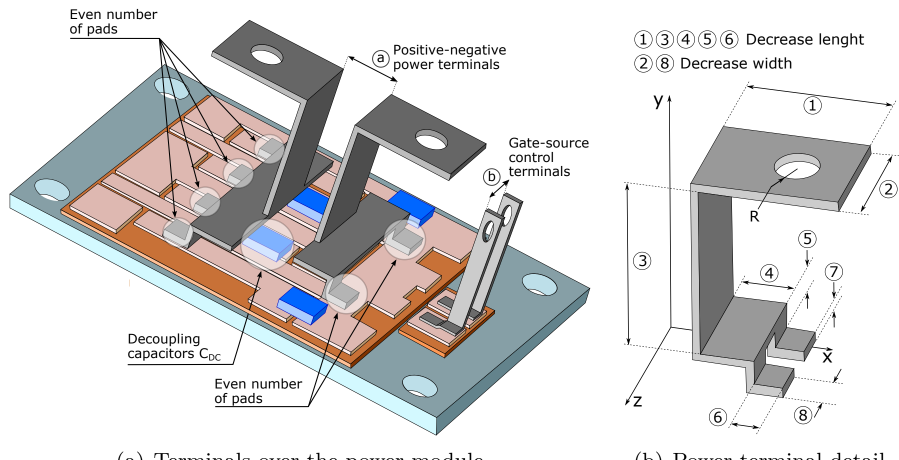
Finally, it is interesting to consider that symmetry can be further improved following the design philosophy inherited from radio frequency (RF) and microwave design techniques used for power amplifiers, because both pursues similar goals [362]. According to these ideas, implementing round tracks, special cuts, edges and using passive components (capacitors, figures 5.7(b) and 5.7(c)) can help to further balance and reduce power loops [359].

- Reducing the number of interconnections, particularly wirebondings, can be beneficial, since they introduce significant parasitic impedances and EMI to the circuit, aside from being the main source of failures due to mechanical stress [334, 354, 363]. As a general rule, wirebondings should only be used when another routing solutions are not possible in the design [315]. When using them, they must be as short as possible, and must be placed in an array configuration to reduce the parasitic inductance (generated due to parallel connection and coupling effects).

5.6 Terminals: power and control

The power and control terminals (figure 5.1-E) connect the DBC substrate with the outside of the power module enclosure [364]. In general, these terminals are long and narrow, which significantly increases the total parasitic inductance of the module. Thus, the selection of the most appropriate connectors is a relevant aspect for automotive WBG modules. In order to improve their design, the following concepts could be adopted:

- The amount of terminals must be minimized, if possible, to avoid complex and long current loops [329]. However, there are some exceptions regarding control terminals. When the gate attack follows the embedded PCB design (section 5.4), the use of more control terminals over the DBC conduction layer could be beneficial, as it would reduce the length of gate loops, improving the inductance balance. This is due to the fact that the gate-source contacts of the dies are directly (vertically) connected.



(a) Terminals over the power module. (b) Power terminal detail.

Figure 5.8: Examples of control and power terminals over a power module.

- The pads of the terminals are the linking points between the terminals and the substrate conduction layer. Usually, the terminals have two pads to provide a good mechanical robustness and balance the current distribution in the connector (figure 5.8(a))[1]. The gate and power tracks must be designed to flow equal currents through the multiple pads that constitute the terminal, in order to minimize possible current distribution imbalances [364]. According to this symmetric concept, the terminals should be designed with a minimum even number of pads.

- Ideally, the terminals should be as width and short as possible to reduce their parasitic inductances (figure 5.8(b)), because they take part into the gate control and power loops. Also, differential signals must place their connectors as close as possible to reduce the stray inductance [184]. If the differential connectors (figure 5.8(a)) are close enough, it is possible to internally assemble a decoupling capacitor (C_{DC}) between the positive and negative power terminals [365], providing a reduction on the parasitic inductance.

As a conclusion, it is remarkable that the terminals are sometimes forgotten during the design process. This represents a design flaw as, in some specific cases, they may introduce up to 50 % of the total inductance of power loop [334, 352].

[1]There are some particular exceptions, such as control terminals with only one pad.

5.7 Design steps of the *SiC* power module

Once the parts that constitute the module, their most significant design aspects and the interrelation between them have been clarified, it is important to point out which steps should be carried out in order to achieve a successful automotive power module design. It must be bear in mind that a well organized and appropriate design flow will allow to simplify and accelerate the whole design process of the module. This topic has been addressed in the scientific literature [320, 343, 356, 364]. However, this paper particularizes such work-flows to the WBG context and to the automotive application. As a summary, the design steps are depicted in figure 5.9.

5.8 Conclusions

The scientific literature and a number of agencies from Europe, United States and Asia support the idea that transport electrification will help to reduce current greenhouse gas emissions, which are responsible for some of severe environmental problems. In order to widespread the penetration of HEV/EV technologies, great research efforts should be conducted by the scientific community, leading to investigations on novel power conversion architectures, state of the art WBG power semiconductors, and particularized power module designs, to name a few. For this reason, this section summarises the main thesis concepts treated up to this point.

Regarding the identification of the most appropriate power conversion topology, which is the starting point of this thesis explained in chapter 1, it can be concluded that there is not an unique optimum solution. The following points should be considered in order to select the topology for a given HEV/EV application:

1. In the near future, battery voltage will not exceed 1500 V (typically will be between 300-870 V), because operational safety requirements would significantly increase if such voltage is exceeded. Considering both blocking voltage capabilities of current semiconductor technology and cost efficiency, it becomes evident that two-level technologies will be the preferred option for HEV/EV propulsion system inverters.

2. Considering HEV/EV typical current and power ratings, parallelization of power semiconductor devices becomes mandatory, in the form of bare dies (constituting a power module) or discrete semiconductors.

3. The two-level three-phase topology is generally applied in current light to medium HEV/EVs, as it represents a cost effective solution. However, the

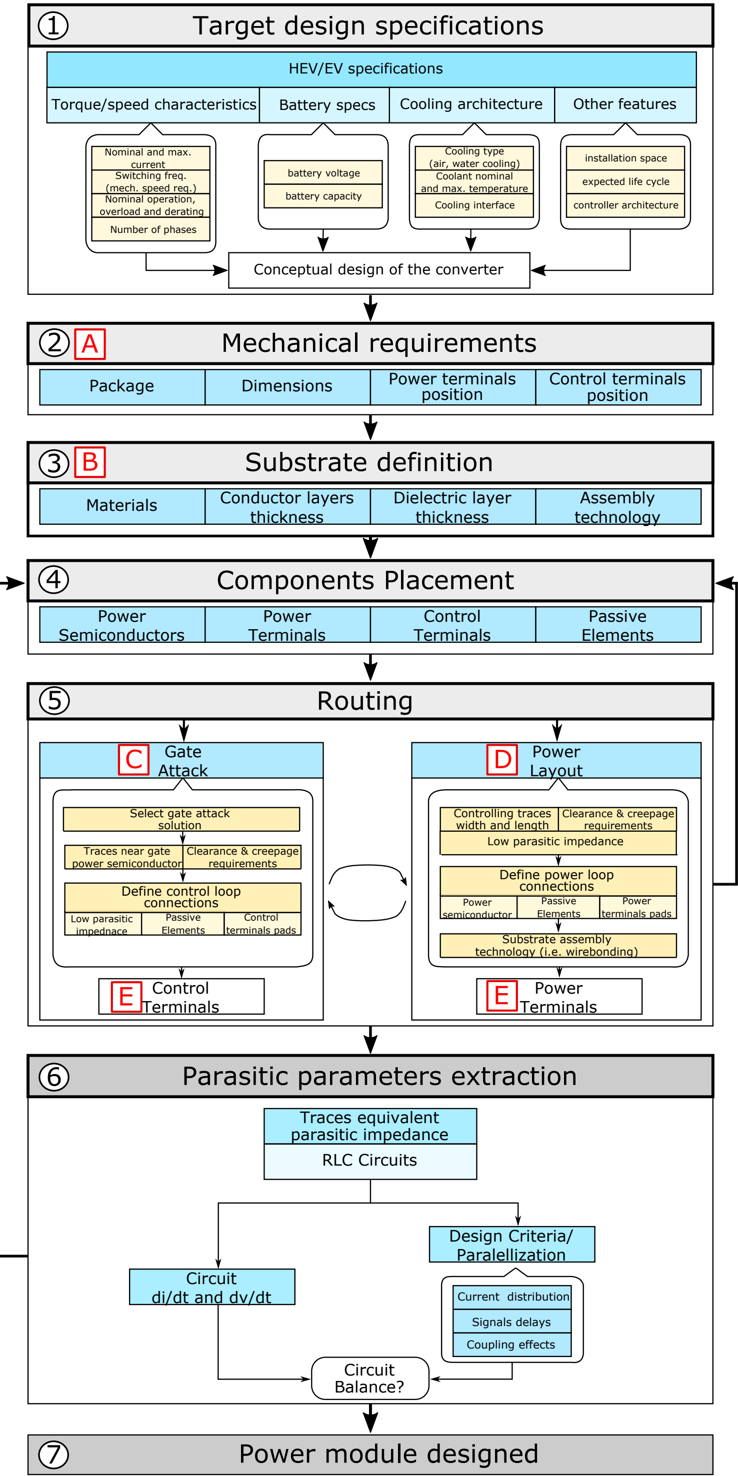


Figure 5.9: General design process for power modules based on standard solutions.

introduction of multiphase technologies should be considered, not only for high power applications (trucks, electric buses or sport cars), but also when relevant propulsion system features such as efficiency, reliability and power and torque density need to be improved. On the other hand, it is important to remark that multiphase topologies could also be used to remove the need of a dedicated power converter for battery charging.

4. The progressive introduction of HSEM technologies will require to progressively increase the switching frequency of the power inverter. For this reason, the introduction of WBG technologies with reduced switching losses becomes crucial for the future. As these new semiconductors can operate at higher junction temperatures, another benefit derived form their introduction would be a reduction of the complexity and cost of the cooling system.

Remembering WBG technologies explained in chapter 3, the scientific literature shows that *GaN* and *SiC* devices are gaining popularity in the automotive market, as they overcome the limitations of traditional *Si* based technology. In this context, the following can be concluded:

5. Current *GaN* technology provides various diodes and HEMT transistors with blocking voltages of around 600-650 V, which, theoretically, could be applied for HEV/EV propulsion systems. However, up to date, they are not a valid option, because their current handling capabilities are highly limited (10-15 A), requiring the parallelization of too many devices. Moreover, there are no vertical devices (lateral devices) at the moment, which are necessary to manufacture compact power module designs with optimized thermal performance.

6. Currently, *SiC* power technology represents a real solution for HEV/EV applications, as a significant variety of matured vertical devices can be found in the market. Among them, it can be concluded that JBS diodes and MOSFETs are the most adequate for this application, because they can substitute traditional *Si* FRD diodes and *Si* IGBTs, providing lower power losses and higher operation temperatures. The migration from *Si* IGBTs to the aforementioned technologies would be simpler than expected, as the same firing circuitry (with minor modifications) can be reused.

From the proposed design criteria, the constituting element of the HEV/EV propulsion converter, with independence of the number of phases, would be (in the great majority of cases) the half-bridge configuration. In general, power modules are preferred over discrete devices due to their superior features. Considering, on the one hand, the demanding requirements of the automotive industry and, on

the other, that parasitic inductances must be minimized as much as possible when incorporating WBG devices with high switching speeds, the following conclusions regarding design aspects can be highlighted:

7. The mechanics (power module encapsulation and layout of power and auxiliary terminals) imposes the main constraints for the design of the other elements that constitute the power module. Thus, special attention is required when designing such critical part. In the automotive context, the mechanical design must support extreme thermal variations during driving profiles, ensuring a minimum number of operating cycles in such extreme conditions.

8. A great number substrate alternatives, specially for modules incorporating *SiC* technologies, can be found in the scientific literature. However, the standard substrate technology, based on inorganic substrate and wire-bonding interconnections, is a valid option, because it provides a sufficient thermal conductivity and is a cost effective solution.

9. As a general design consideration, gate attacks should be implemented with Kelvin connections in order to avoid feedback effects between control and power signals. Their tracks (i.e., gate and source) should be placed as close as possible, improving mutual coupling effects and avoiding EMI problems. It could also be suitable that each parallel transistor could have its own gate-source connection. This connection should be as short as possible, in order to reduce the equivalent parasitic impedance, and equal to other transistor connections in order to avoid delay problems that produce current imbalances. Finally, it is important to remark that symmetry design should be also conducted, as it helps to balance the control tracks.

10. Application requirements impose the number of device parallelized. Thus, the power semiconductor characteristics should be as similar as possible in order to avoid *on/off* delays issues. Thus, it is convenient to use devices with the same bare code within a module.

11. Regarding the power layout, the number of elements implemented over the substrate should be also minimized in order to obtain more space to balance the electrical connections. Another important aspect when designing the layout is the position and orientation of dies, as it helps to cancel electromagnetic fields between control and power loops. The equivalent parasitic inductance of power loops must be reduced by controlling the dimensions of the tracks. The concept of symmetric design (achieving a unit, the cell or split, where coupling effect reduce the parasitic inductances and current imbalances) could be also convenient, resulting in a scalable power layout.

12. According to the literature, terminals can introduce up to 50 % of the whole parasitic inductance of the power module. For this reason, this drawback must be mitigated minimizing their number, controlling their dimensions (being the connectors as width and short as possible), and dividing the current in an even number of pads for balancing.

Following such design criteria, the performance of the automotive modules would be enhanced, improving the overall features of the propulsion system and, consequently, of the vehicle. As a general conclusion, it can be stated that next generation WBG based power systems will have a relevant role in the development of future HEV/EVs.

Chapter 6

Parallelization of power converter circuits (PCC) according to the proposed design criteria

6.1 Introduction

Nowadays, power electronic applications need high voltage and current ranges. These ranges are usually out of operational limits of discrete chips and, sometimes, of power modules, so serial and parallel configurations are necessary. A solution to increase power converter current ranges is to use the device parallelization. This solution is used in commercial designs composed of several dies in parallel where current imbalances can appear due to physical properties of layout.

The proper parallel operation is produced when semiconductor current distributions are as equal as possible, since imbalances reduce device lifetime and deteriorate circuit electrical properties [346, 347]. There are many factors in a circuit in order to get a good balance of parallelized power semiconductors. As chapter 4 mentions, the balance depends on semiconductor characteristic parameters ($V_{ce_{(sat)}}$, $t_{d_{(on)}}$, $t_{d_{(off)}}$, temperature coefficient, etc), the gate-emitter (Z_{ge})

and collector-emitter (Z_{ce}) impedances[1] and the DC-link connection [341, 366], whose parasitic effects on the power converter must be minimized.

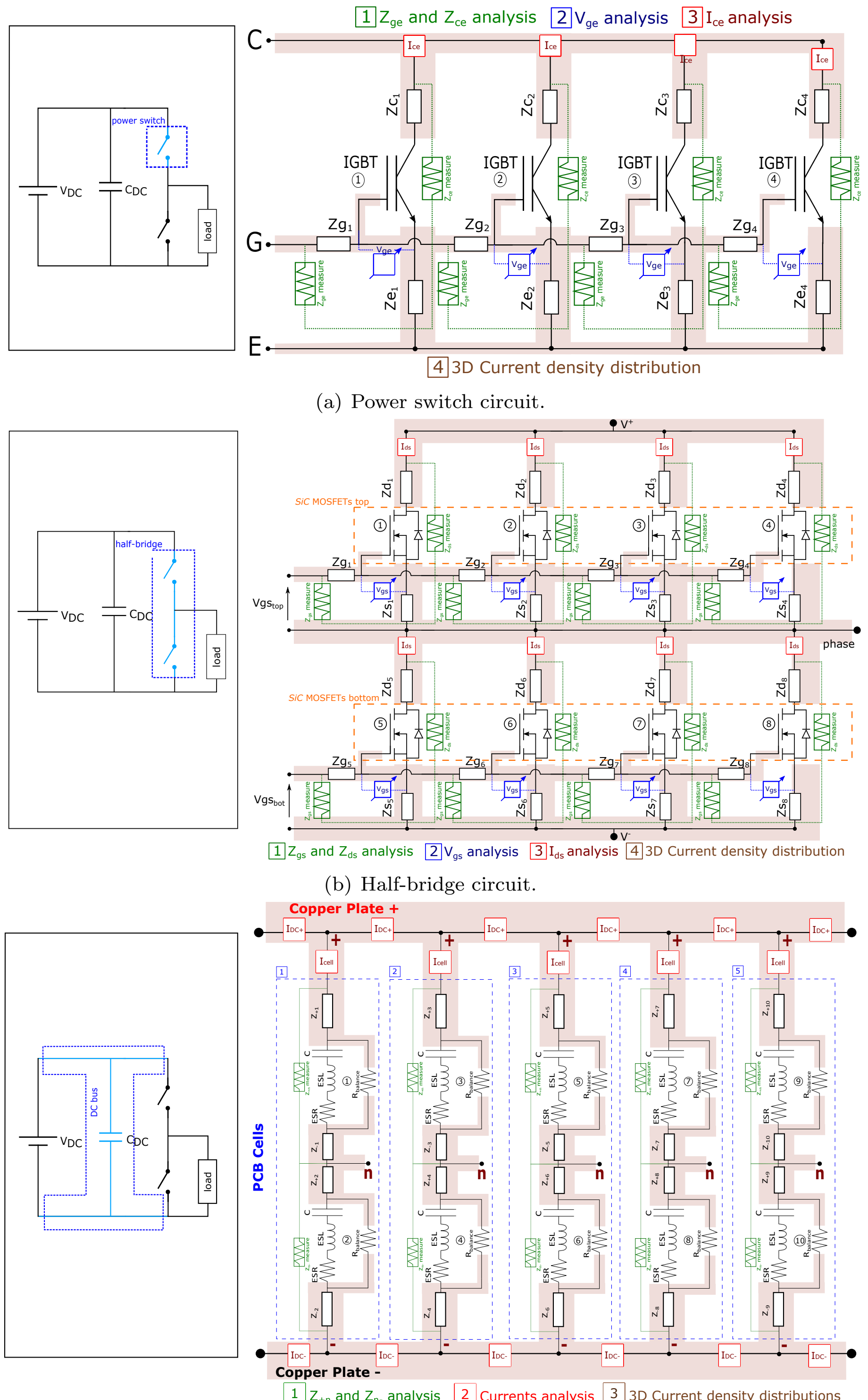
Taking into account the concepts and criteria previously developed in chapter 5, this chapter puts into practice their implementation through a series of power converter circuits (figure 6.1). The improvements of this methodology are checked through simulations of the following circuits, which are the previous step to apply the design criteria in a specific power module (chapter 7):

1. A power switch composed by 4 parallel IGBTs (figure 6.1(a)) is analysed, extracting the layout parasitic impedances, voltages and current distributions of four alternatives. The simulations of these circuits are compared with each other to understand the switching variations due to geometries, specially the position of main terminals. The study helps in establishing and checking criteria for parallelization (section 6.2).
2. A half-bridge composed of 4 *SiC* MOSFETs (figure 6.1(b)) per level is presented. The study of symmetry application is done though three alternatives of half-bridge over a PCB substrate [367]. These simulations show how symmetric tracks and wide area connections improve the performance of power semiconductors in parallel. Finally, the implementation of circuit protections and RF design techniques (chapter 5), where round tracks and cutting edges improve the circuit current distributions, are presented over one half-bridge (section 6.3).
3. A multilayer DC bus (figure 6.1(c)) rated at 400/500 V is designed taking into account the parallelization technique of power devices [342], balancing the capacitors and reducing stray impedances. Thus, the DC bus electromagnetic model is extracted [368], which allows the analysis of 3D current density distribution. Finally, the simulation results are validated with experimental measures from a prototype (section 6.4).

6.2 Power switch based on semiconductor parallelization

In this section, different layouts are simulated with the aim of studying parallelization effects. These analyses are summarized in figure 6.1(a), where stray impedances, the variations in gate control voltages and power semiconductor currents and current density distributions are extracted from each circuit topology. The switch circuit consists of 4 parallel IGBTs (AUIR4067D1, 600 V/160 A,

[1] In the case of MOSFETs, gate-source (Z_{gs}) and collector-source (Z_{cs}).

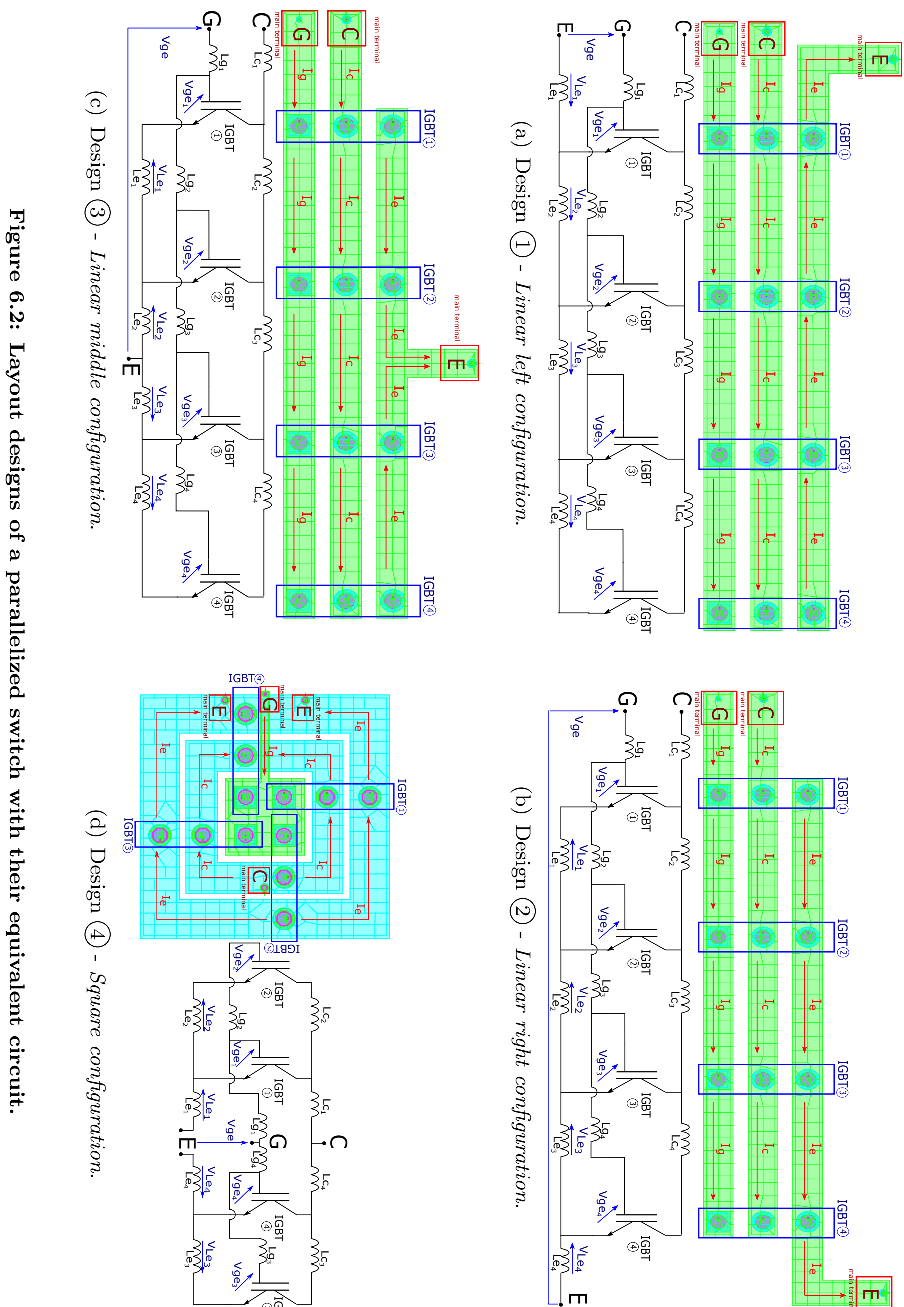


(a) Power switch circuit.

(b) Half-bridge circuit.

(c) DC bus circuit (C=20 μF, ESL=35 nH, ESR=1.9 mΩ and $R_{balance}$=1 MΩ).

Figure 6.1: Circuits and analysis applied in each power circuit.



(a) Design ① - *Linear left configuration.*

(b) Design ② - *Linear right configuration.*

(c) Design ③ - *Linear middle configuration.*

(d) Design ④ - *Square configuration.*

Figure 6.2: Layout designs of a parallelized switch with their equivalent circuit.

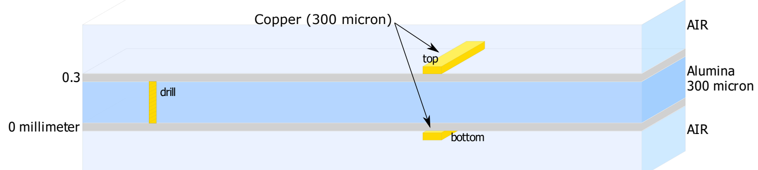


Figure 6.3: Substrate configuration of power switch alternatives (ADS^{TM}).

International Rectifier) in different topologies connected to a load (87 nH and 0.8 Ω). The figure 6.2 shows the proposed power switch configurations:

1. Design ① (figure 6.2(a)) is a linear topology connection of IGBTs. The main terminals (gate, collector and emitter) are in the same side of layout, where I_c and I_e path currents have opposite directions. In the following, this design will also be called *linear left configuration*, due to the position of emitter terminal in its layout.

2. Design ② or *linear right configuration* (figure 6.2(b)) presents the emitter main terminal in the opposite side compared to design ① , so I_g, I_c and I_e path currents have the same direction.

3. In design ③ (figure 6.2(c)) the emitter main terminal appears in the middle of the track, so it is named *linear middle configuration*. For this emitter terminal position, there are two I_e current directions in the same path, being a mix of design ① and ②.

4. Design ④ (figure 6.2(d)) presents IGBTs in a *square configuration* around their gates (symmetric concept) and in two layers (top and bottom) with a better coupling effect (parallel plate) [369].

6.2.1 Closed loop impedances: gate-emitter and collector-emitter

In this section, the equivalent stray impedances for each power switch alternative are extracted to calculate the electrical length of each circuit connection, so that great connection differences between parallelized devices can be identified and solved. In order to calculate the equivalent impedances of gate-emitter and collector-emitter closed loops, the substrate topology has to be defined (figure 6.3) because impedances depend on material properties. The gate-emitter closed loop gives the equivalent Z_{ge} impedance values between gate and emitter main terminals with each IGBT gate and emitter. Measurements in collector-emitter closed loop also give the equivalent Z_{ce} values between collector and emitter main terminals with each IGBT collector and emitter. The impedance values have been extracted from S-parameters matrix where a Y-parameters conversion has been applied to obtain directly R and L values (methodology of appendix A).

Figures 6.4(a) and 6.4(d) show impedance values of gate-emitter closed loop (L_{ge} and R_{ge}), and figures 6.4(b) and 6.4(e) collector-emitter closed loop (R_{ce} and L_{ce}) for 10 kHz (modulation frequency of the power converter). The maximum variations between IGBTs for each design are shown in figures 6.4(c) and 6.4(f). The results show that the *square* design has the lowest R_{ge}, L_{ge}, R_{ce} and L_{ce} values with a little variation of them, due to its symmetrical topology, short paths and better coupling effect (the main design criteria objectives of chapter 5).

On the other hand, *right* design configuration presents maximum Z_{ge} and Z_{ce} values, so semiconductor losses are higher. However, variations between R_{ge}, L_{ge}, R_{ce} and L_{ce} are minimum; as a result, the current per each IGBT is more evenly distributed, thus producing lower imbalances than in other designs. This is because I_g, I_c and I_e have the same direction in layout tracks.

The main difference between *left* and *right* designs is the direction of I_e, which is why impedance values are therefore different because of mutual coupling effects. The values R_{ge}, L_{ge}, R_{ce} and L_{ce} of *left* design are lower than *right* design, but variations between IGBT branches are higher. *Middle* design reduces R_{ge}, L_{ge}, R_{ce} and L_{ce} values compared with design *left*, but inductance and resistance variations are not enough compared with *right* and *square* designs.

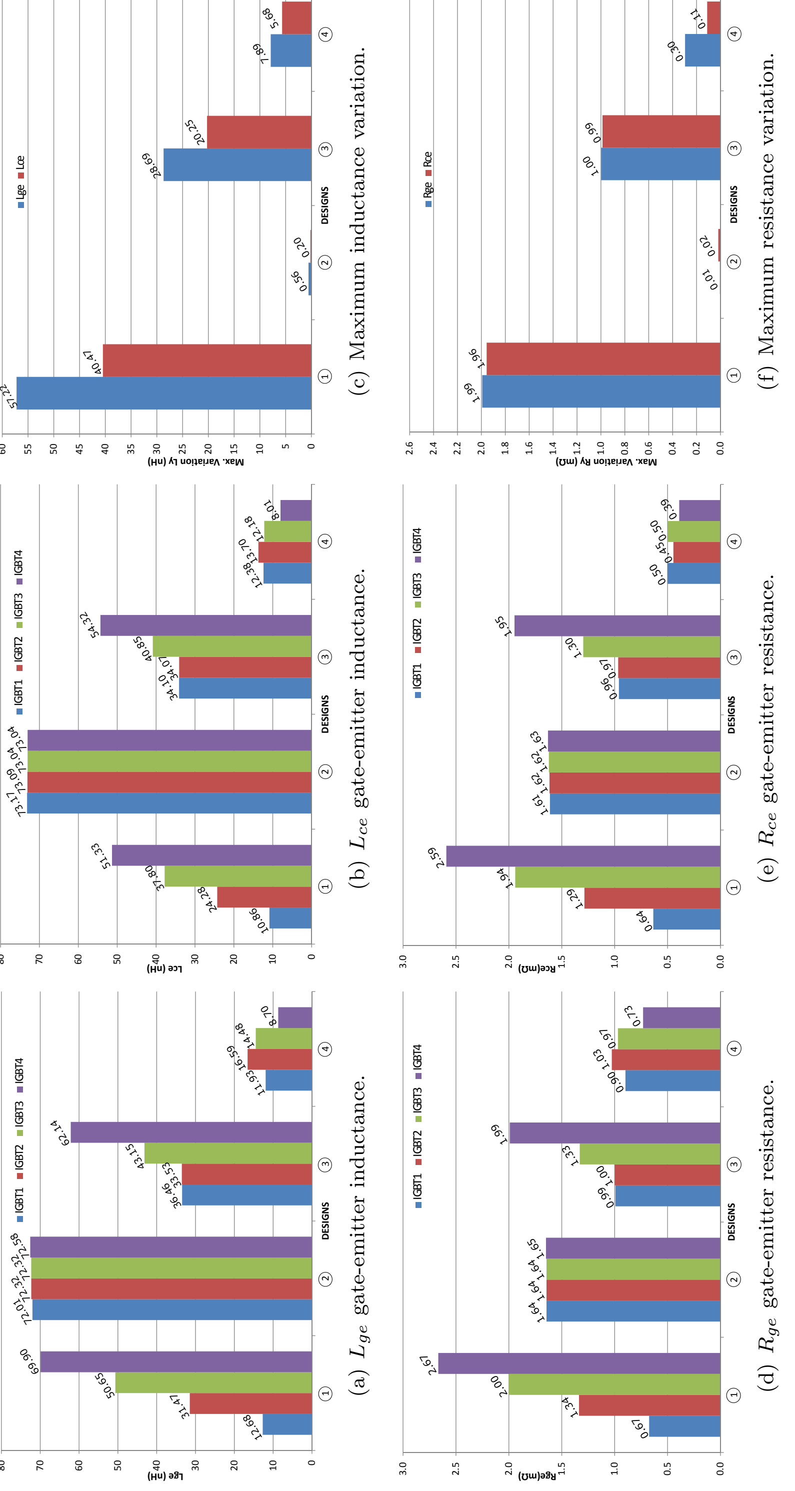
6.2.2 Gate-emitter closed loop influence on V_{ge} signals

Connection between IGBTs and driver circuit (gate connection) generates a closed gate-emitter loop. Here, different feedback effects produce variations between parallelized IGBTs gate voltage signals (V_{ge}). These V_{ge} signal variations affect, specially, the turn *off* process, causing differences in switching losses.

The origin of feedback effect depends on the emitter position and parasitic inductance values (figure 6.4). The specific feedback effect of each design, taking into account the four types detailed in chapter 5, is explained through the gate-emitter voltage equations. In these voltage expressions, the gate inductance is negligible respect to emitter inductance ($\frac{di_e}{dt}>>\frac{di_g}{dt}$), simplifying the equations:

1. *Linear left configuration* (design ①) presents a negative asymmetric feedback (figures 6.2(a) and 6.5(a)) causing IGBT4 to turn *on* slower than IGBT1. This layout presents equal length tracks between IGBT2-IGBT4, being shorter the IGBT1. For this reason, the following inductance expression L=L_{e_2}=L_{e_3}=L_{e_4}> L_{e_1} explains the inductance voltage drop V_L=$V_{L_{e_2}}$=$V_{L_{e_3}}$=$V_{L_{e_4}}$>$V_{L_{e_1}}$ and therefore.

$$\begin{aligned} V_{ge_4} = (V_{ge} - 3 \cdot V_L - V_{L_{e_1}}) < V_{ge_3} = (V_{ge} - 2 \cdot V_L - V_{L_{e_1}}) < \\ < V_{ge_2} = (V_{ge} - V_L - V_{L_{e_1}}) < V_{ge_1} = (V_{ge} - V_{L_{e_1}}). \end{aligned} \tag{6.1}$$



(a) L_{ge} gate-emitter inductance.

(b) L_{ce} gate-emitter inductance.

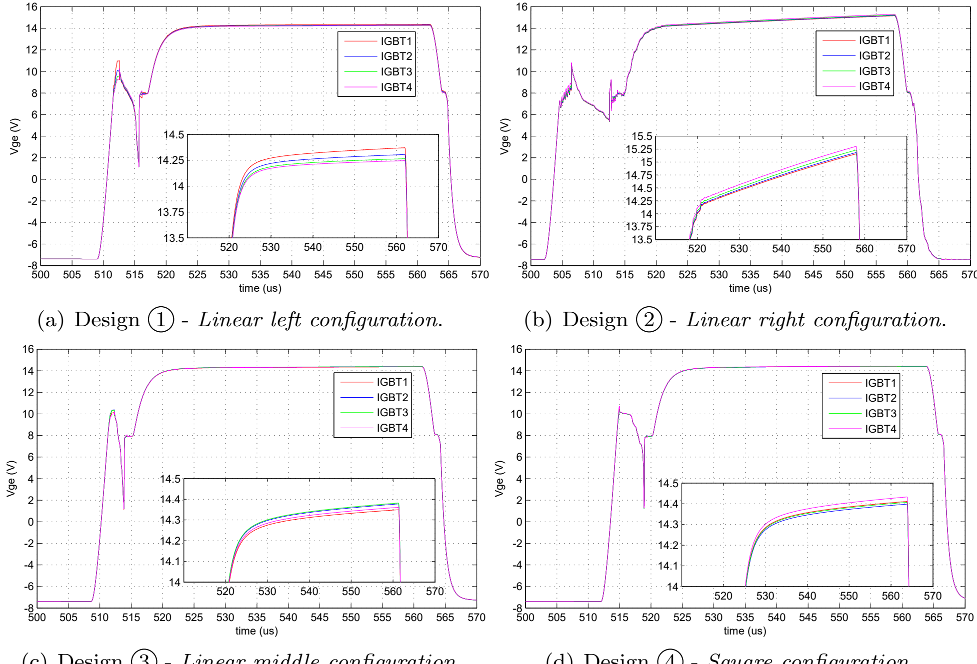
(c) Maximum inductance variation.

(d) R_{ge} gate-emitter resistance.

(e) R_{ce} gate-emitter resistance.

(f) Maximum resistance variation.

Figure 6.4: Z_{ge} and Z_{ce} measures for each design at 10 kHz.



(a) Design ① - *Linear left configuration.*

(b) Design ② - *Linear right configuration.*

(c) Design ③ - *Linear middle configuration.*

(d) Design ④ - *Square configuration.*

Figure 6.5: V_{ge} signals for the designs of a power switch with 4 IGBT parallelized.

2. *Linear right configuration* (design ②) has a positive asymmetric feedback (figures 6.2(b) and 6.5(b)), so IGBT1 is turned *on* faster than IGBT4. The layout inductance expression $L{=}L_{e_1}{=}L_{e_2}{=}L_{e_3}{>}L_{e_4}$ produces the voltage drops $V_L{=}V_{L_{e_1}}{=}V_{L_{e_2}}{=}V_{L_{e_3}}{>}V_{L_{e_4}}$, and therefore.

$$\begin{aligned} V_{ge_1} &= (V_{ge} - 3 \cdot V_L - V_{L_{e_4}}) < V_{ge_2} = (V_{ge} - 2 \cdot V_L - V_{L_{e_4}}) < \\ &< V_{ge_3} = (V_{ge} - V_L - V_{L_{e_4}}) < V_{ge_4} = (V_{ge} - V_{L_{e_4}}). \end{aligned} \tag{6.2}$$

3. *Linear middle configuration* (design ③) presents a positive and negative feedback (figures 6.2(c) and 6.5(c)), because emitter currents flow in two directions. Mutual inductances have an important effect in this case, so the following inductance expressions $L_{e_3}{<}L_{e_2}{<}L_{e_4}{<}L_{e_1}$ produce the voltage inductance drops $V_{L_{e_3}}{<}V_{L_{e_2}}{<}V_{L_{e_4}}{<}V_{L_{e_1}}$, and therefore.

$$\begin{aligned} V_{ge_3} &= (V_{ge} - V_{L_{e_3}}) > V_{ge_2} = (V_{ge} - V_{L_{e_2}}) > V_{ge_4} = \\ &= (V_{ge} - V_{L_{e_3}} - V_{L_{e_4}}) > V_{ge_1} = V_{ge} - V_{Le_1} - V_{Le_2}. \end{aligned} \tag{6.3}$$

4. *Square configuration* (design ④) works like two positive asymmetric feedback (figures 6.2(d) and 6.5(d)) because of trace length behaviour $L_{e_4}{<}L_{e_1}$

and $L_{e_3} < L_{e_2}$, so voltage emitter inductance drops are $V_{L_{e_4}} < V_{L_{e_1}}$ and $V_{L_{e_3}} < V_{L_{e_2}}$, and therefore.

$$\begin{aligned} V_{ge_4} = (V_{ge} - V_{Le_4}) > V_{ge_1} = (V_{ge} - V_{Le_1}) > V_{ge_3} = \\ = (V_{ge} - V_{Le_4} - V_{Le_3}) > V_{ge_2} = (V_{ge} - V_{Le_1} - V_{Le_2}). \end{aligned} \tag{6.4}$$

This analysis shows that designs ② and ④, which present lower Z_{ge} and Z_{ce} variations, have lower V_{ge} voltage drops between IGBTs. The currents through IGBTs are more balanced. However, design ① presents a wide V_{ge} variation because its emitter inductances are very unequal, causing high imbalances between IGBT currents. Design ③ has two different V_{ge} (two I_e current directions in the same copper trace) levels proportional to the distance between each IGBT emitter and main emitter layout terminal.

6.2.3 Collector-emitter closed loop influence on I_{ce}

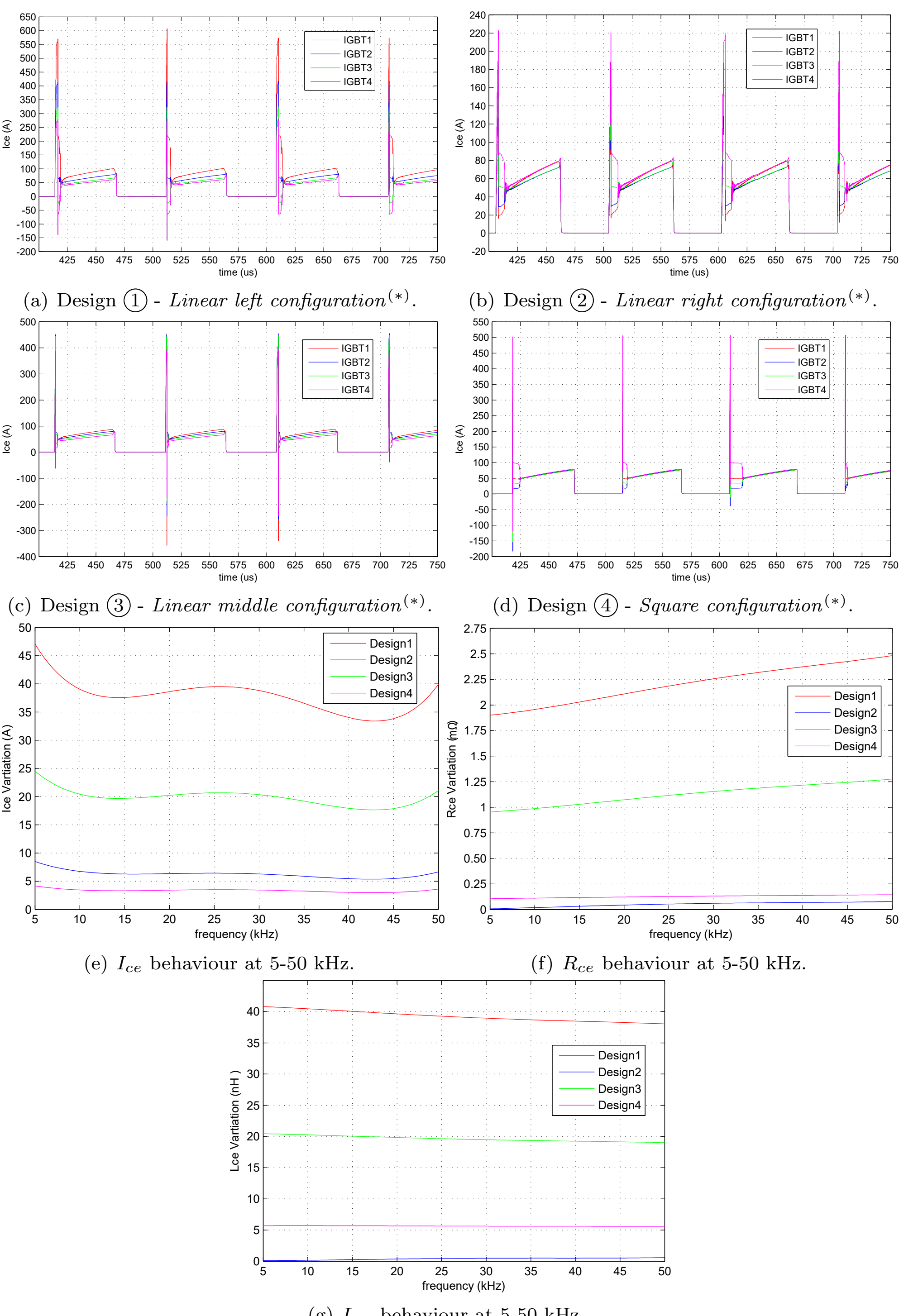
Parallelized IGBTs have different current distribution because of trace connections. Apart from IGBT gate and driver connections, which generate delays between device gate signals (V_{ge}), the design of path between collectors and emitter of the IGBTs is critical. The following conclusions can be drawn from the simulations shown in the figure 6.6:

1. *Linear left configuration* (design ①) presents the worst current distribution for 10 kHz switching signals (figure 6.6(a)) with 47 A current variation due to the large differences between Z_{ce} IGBT values and its linear topology.

2. *Linear right configuration* (design ②) has similar current per IGBT branch (figure 6.6(b)) with maximum variation of only 8.5 A. Moreover, initial turn *on* oscillation is lower than in the other designs due to higher Z_{ce} values, compared with the other design impedances. In spite of its linear geometry, coupling effects compensate the layout dimensions due to current directions.

3. *Linear middle configuration* (design ③) has the same problems as ①. The current distribution presents a maximum of 24.5 A variation between IGBTs at 10 kHz (figure 6.6(c)) because R_{ce} and L_{ge} are very different between IGBTs. However, results are better than in previous designs, since emitter main terminal provides better symmetry.

4. *Square configuration* (design ④) has the best current distribution between IGBT branches with a maximum variation of 4.1 A at 10 kHz (figure 6.6(d)), due to symmetrical dimensions and equal values of Z_{ce} between IGBTs and the main terminals.



(a) Design ① - *Linear left configuration*$^{(*)}$.

(b) Design ② - *Linear right configuration*$^{(*)}$.

(c) Design ③ - *Linear middle configuration*$^{(*)}$.

(d) Design ④ - *Square configuration*$^{(*)}$.

(e) I_{ce} behaviour at 5-50 kHz.

(f) R_{ce} behaviour at 5-50 kHz.

(g) L_{ce} behaviour at 5-50 kHz.

(*) Current signals obtained with a switching frequency of 10 kHz.

Figure 6.6: IGBT currents and I_{ce}, R_{ce} and L_{ce} variations with frequency.

These data reveal that IGBT current distribution depends on R_{ce} and L_{ce}. When these values are very unequal between IGBTs and layout main terminals, current distribution presents wide variations (designs ① and ③). However, if R_{ce} and L_{ce} values are similar, current variations are smaller (designs ② and ④). The improvements of symmetry reducing current imbalances and parasitic impedance values are shown in figures 6.6(e), 6.6(f) and 6.6(g) with stable behaviours between 5 - 50 kHz (switching frequency range to silicon power modules).

6.2.4 Current density distribution over the power switches

Current distribution depends on the previous data: Z_{ge} and Z_{ce} (proportional to layout configuration and physical), V_{ge} voltage signals (causing delays between parallel IGBTs), and current direction (adding/subtracting mutual coupling effects).

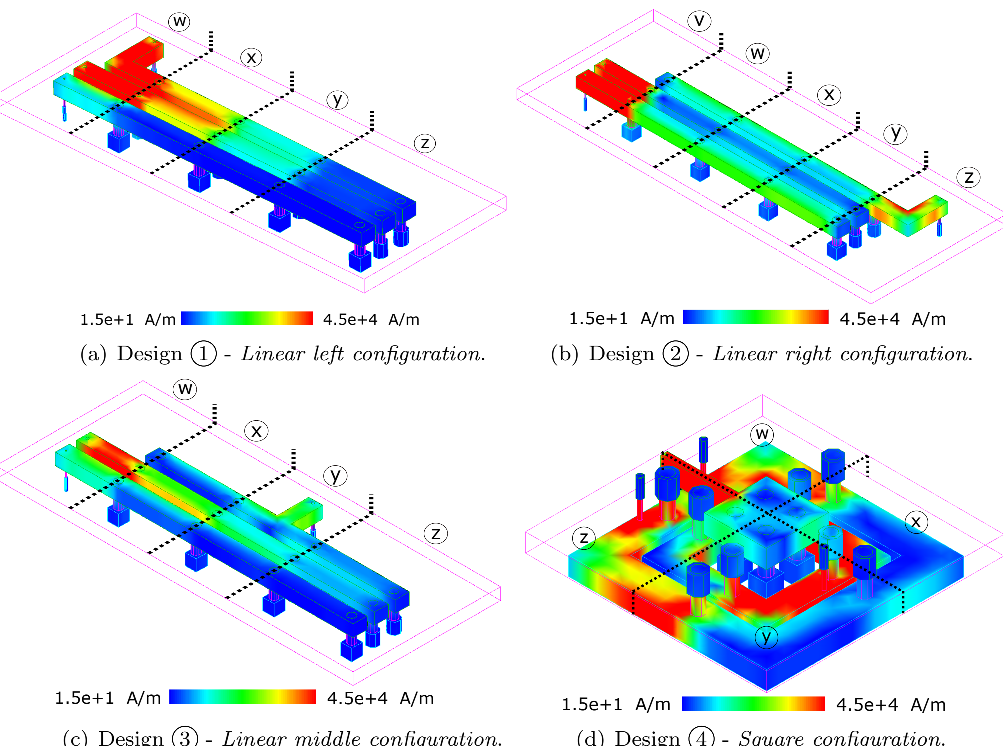
Indeed, according to V_{ge} signals and I_{ce} currents, that *left* (design ①, figure 6.7(a)) and *right* (design ②, figure 6.7(b)) configurations present the worst current density distribution, in both designs 10 kHz signals present the ⓦ (figures 6.7(a)-6.7(b)) area with a higher current density than the rest of paths. This fact is due to no symmetry of *left* and *right* configurations.

However, the *middle* configuration (design ③) presents a better current density distribution (figure 6.7(c)), since emitter main terminal (figure 6.7(c)-ⓨ area) gives to the circuit a symmetrical behaviour at 10 kHz and an equal current emitter distribution, but design ③ presents a higher current density in the figure 6.7(c)-ⓦ area which unbalances collector current.

Finally, the *square* design (design ④, figure 6.7(d)) has the best symmetrical current density distribution, because 10 kHz signals have similar current density through paths of the figures 6.7(d)-ⓦ and 6.7(d)-ⓩ areas with high current density levels.

6.3 Half-bridge based on the layout symmetry

This section studies how the geometry influences the performance of a half-bridge circuit that has 4 900 V, 36 A *SiC* MOSFETs parallelized per level. The analyses are shown in figure 6.1(b) (load of 55 μH and 5 Ω), considering the same studies on voltage and current as in the power switch case (section 6.2). The particularity of this section is the application of chapter 5 design criteria for the development of the power module constituting element, the half-bridge topology. The following three proposed half-bridge geometries are a step forward in the



(a) Design ① - *Linear left configuration.*

(b) Design ② - *Linear right configuration.*

(c) Design ③ - *Linear middle configuration.*

(d) Design ④ - *Square configuration.*

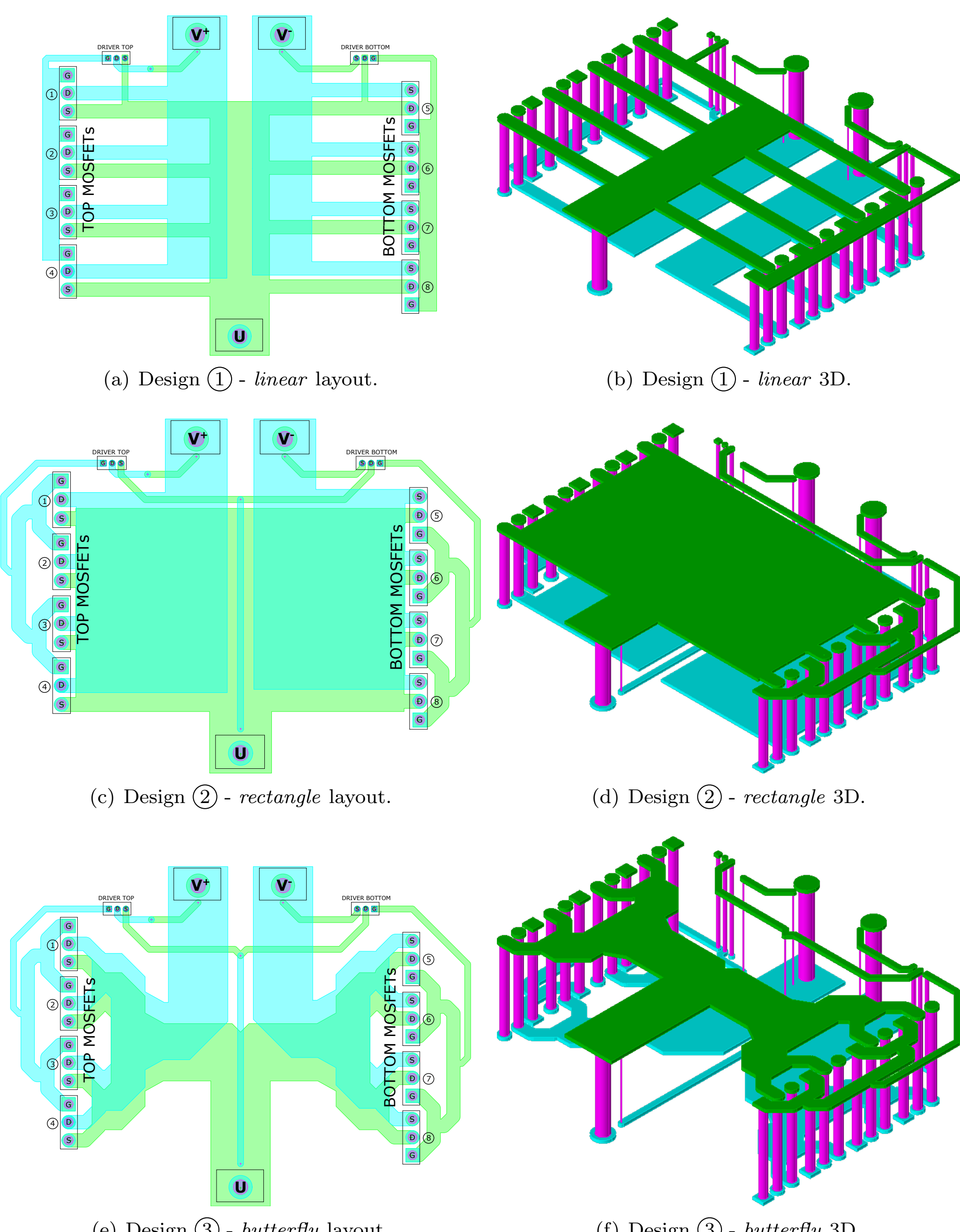
Figure 6.7: 3D current density distribution at 10 kHz.

symmetry application and exemplification (chapter 5) using WBG technology (chapter 3), where the control of parasitic circuit elements are more critical.

1. Design ① (figures 6.8(a) and 6.8(b)) presents a geometry without symmetry application in the paths that join the driver gates (top and bottom connectors) with the the *SiC* MOSFET gates. The same happens in drain-source connections between the main terminals and the *SiC* MOSFETs, because of this lack of symmetry the design is also called *linear* configuration.

2. Design ② (figures 6.8(c) and 6.8(d)) presents a modification of design ①, where symmetric traces connect the gates of driver (top and bottom) with *SiC* MOSFETs gates. The connection of the drains and sources (between the main terminals and the *SiC* MOSFETs) is implemented through large copper areas, so that current can flow through the shortest path. In fact, these copper areas give the name of *rectangle* configuration.

3. Design ③ (figures 6.8(e) and 6.8(f)) presents the evolution of the ② design, where the symmetry of paths which connect the driver connectors



(a) Design ① - *linear* layout.

(b) Design ① - *linear* 3D.

(c) Design ② - *rectangle* layout.

(d) Design ② - *rectangle* 3D.

(e) Design ③ - *butterfly* layout.

(f) Design ③ - *butterfly* 3D.

Figure 6.8: Half-bridge PCB with 4 *SiC* MOSFET in parallel.

Table 6.1: Substrate materials used in the half-bridge designs.

Layer	Material	Thickness (mm)
Top	Copper	$0.105^{(*)}$
Dielectric	FR-4	$2.990^{(*)}$
Bottom	Copper	$0.105^{(*)}$

Table notes:
(*) Typical thickness used in 3.2 mm PCBs with top and bottom layers.

and MOSFETs gates are maintained. However, the areas of drain-source with the main terminals are reduced, thus trying to force the current flow homogeneously. This design is also named *butterfly* configuration.

6.3.1 Closed loop impedances: gate-source and collector-source

As in the power switch case (figure 6.1(a)), the behaviour of the circuit depends on layout connections and substrate materials (table 6.1), which define the circuit parasitic impedances, as well asswitching frequencies and each *SiC* MOSFET internal characteristics.

The gate-source closed loop provides the parasitic impedance value Z_{gs}, obtained for each MOSFET between the driver terminals (top and bottom) and the respective transistor terminals. The drain-source closed loop measurements provide the parasitic impedance values Z_{ds} between the drain and source driver terminals respect to the MOSFET terminals. Thanks to these impedance values (Z_{gs} and Z_{ds}) the equivalent parasitic resistive and inductive components are calculated, thus obtaining R_{gs} and L_{gs}, for the loop gate-source, and R_{ds} and L_{ds} for the drain-source loop.

Figures 6.9(a), 6.9(b), 6.9(c) and 6.9(d) show the values of parasitic inductances and resistances for the three designs at 20 kHz (*SiC* MOSFET switching frequency[1]). According to data extracted from simulations, the *linear* design (design ①) has the lowest values of inductances L_{gs} and L_{ds}, as well as resistance R_{gs} and R_{ds} with respect to the rectangle (design ②) and butterfly (design ③ designs, where *butterfly* shows the highest values.

In spite of lowest parasitic inductance and resistance values of *linear* design, the design criteria developed in chapter 5 explains that absolute parasitic element

[1]The *SiC* MOSFET technology allows to switch at higher frequencies than *Si* IGBT technology, as chapter 3 indicates. The 20 kHz switching frequency is adopted in order to avoid simulation converge problems of MOSFET equivalent model provided by the manufacturer (Wolfspeed/Cree).

values are important, but relative values between parallelized semiconductors are more relevant in order to reduce current imbalance effects. Thus, top ($MOSFET_1$, $MOSFET_2$, $MOSFET_3$ and $MOSFET_4$) and bottom ($MOSFET_5$, $MOSFET_6$, $MOSFET_7$ and $MOSFET_8$) MOSFETs must present inductance and resistance values as similar as possible each other. Analysing the variation of L_{gs} (figure 6.9(e)), R_{gs} (figure 6.9(g)), L_{ds} (figure 6.9(f) and R_{ds} (figure 6.9(h)), the *linear* design has the widest variation in their inductances and parasitic resistances with respect to the *rectangle* and *butterfly* designs whose variations are minimal.

6.3.2 Gate-source closed loop influence on V_{gs}

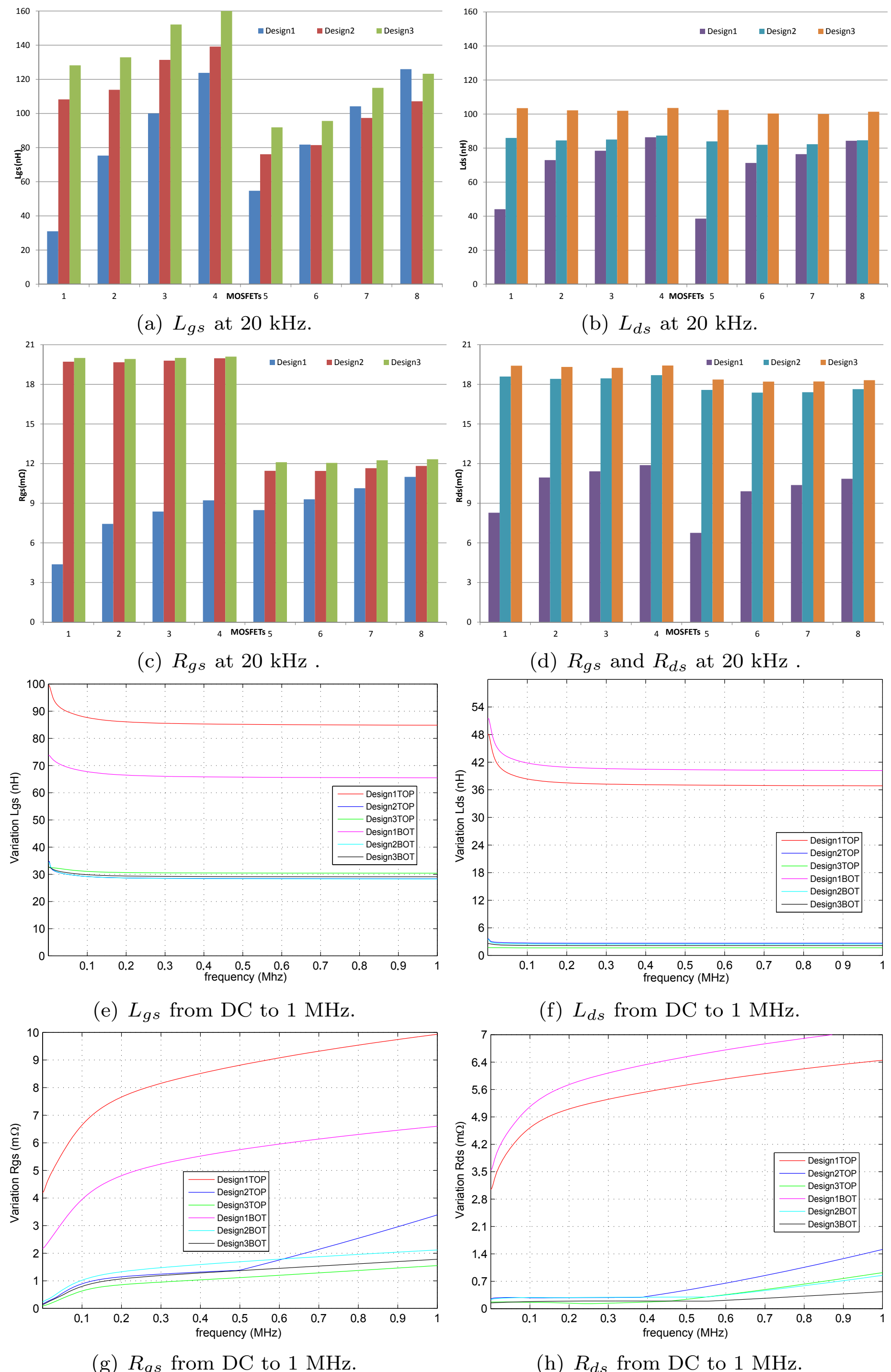
The connection between the *SiC* MOSFETs and the driver generates a closed loop gate-source. As a result, the non-application of symmetry (different parasitic impedance) provokes feedback effects, which cause delays of the V_{gs} signal, affects the switching *on/off* and generate different switching losses. The inductive values extracted from simulation provoke the following effects on the signals V_{gs} for each design:

1. The *linear* configuration (design ①) presents a positive asymmetric feedback for the top MOSFETs, so $MOSFET_1$ turns *on* faster than $MOSFET_4$ (figure 6.10(a)). Bottom MOSFETs have identical connections; therefore, the same feedback effects are produced and their consequences are less decisive since in the half-bridge the bottom devices operate as diodes (figure 6.10(d)).

2. The *rectangle* configuration (design ②) presents a major improvement over the design ①, since the paths that connect the driver and MOSFET gates are symmetric (top and bottom). In addition, the drain and source connections are large cooper areas allowing the best current propagation. As a result of the simulations, the V_{gs} signals for top (figure 6.10(b)) and bottom (figure 6.10(e)) MOSFETs are practically identical (symmetric feedback), with certain oscillations because of inductance increment in the circuit.

3. The *butterfly* configuration (design ③) is an evolution of the design ②, where the symmetry of the drain-source is improved, forcing the current to flow in a certain way on the circuit. As in the design ②, the possible feedback effects are minimized thanks to the symmetry. Although the parasitic inductances are greater than in ②, the behaviour of the gate signals for both the top (figure 6.10(c)) and bottom (figure 6.10(f)) MOSFETs is identical.

Chapters 4 and 5 show the behaviour of the V_{gs} signals directly affects each device current, since the gate-source and drain-source loops share the source inductance



(a) L_{gs} at 20 kHz.

(b) L_{ds} at 20 kHz.

(c) R_{gs} at 20 kHz .

(d) R_{gs} and R_{ds} at 20 kHz .

(e) L_{gs} from DC to 1 MHz.

(f) L_{ds} from DC to 1 MHz.

(g) R_{gs} from DC to 1 MHz.

(h) R_{ds} from DC to 1 MHz.

Figure 6.9: Equivalent parasitic impedance variations.

(L_s) of each MOSFET. Thus, the *butterfly* design will have the lower current deviation between MOSFETs.

6.3.3 Collector-source closed loop influence on I_{ds}

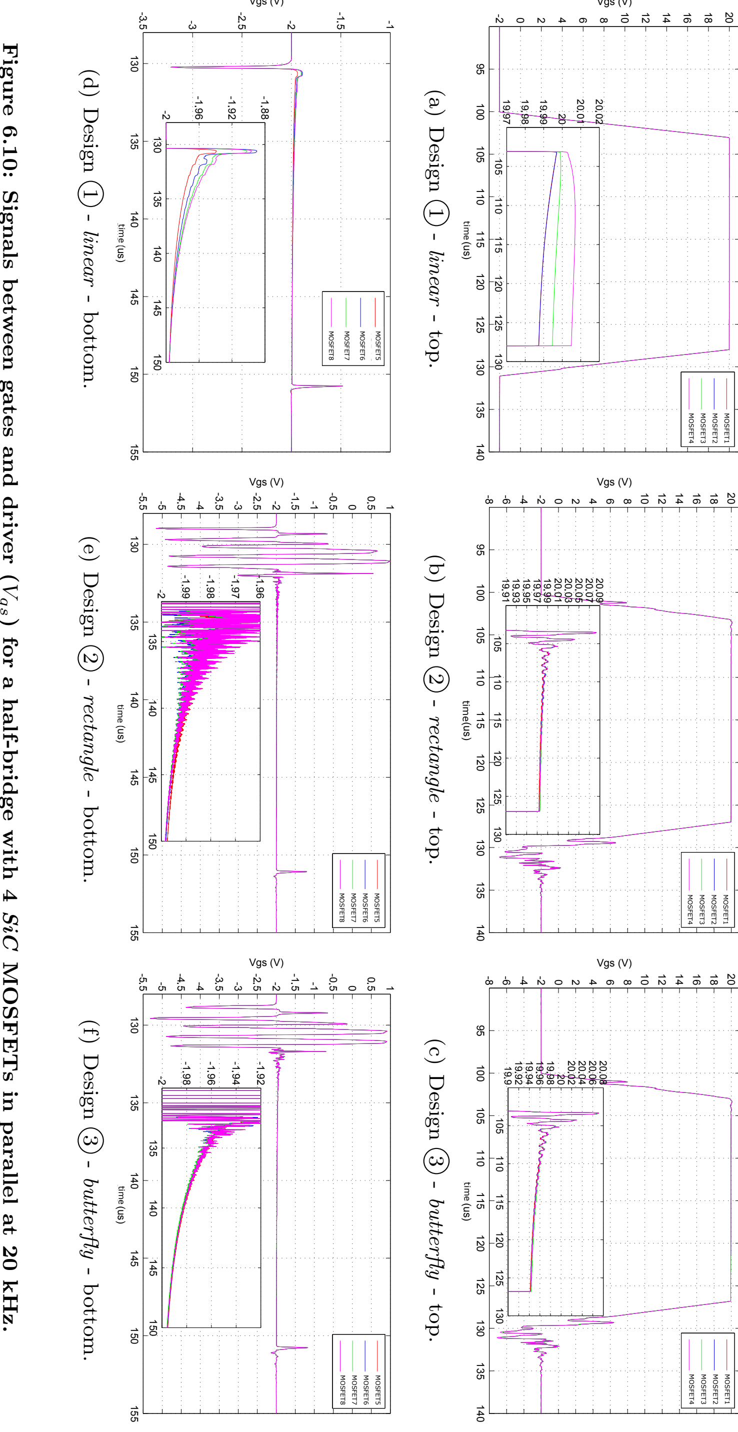
The connections between drains and sources are also critical, since they are part of layout where high current flows. If symmetry is not correctly implemented on the drain-source closed loop, current distribution imbalances through MOSFETs can appear. The current distributions for the three designs is as follows:

1. The *linear* configuration (design ①) presents the worst current distribution at 20 kHz, since the current of the top *SiC* MOSFETs is not equal in each parallel device (figure 6.11(a)). Although the simulations provide a minimum variation, they are conditioned by the quality of the *SiC* MOSFET model and the device simplification where all the transistors are identical. Therefore, this current imbalance should be higher in real conditions. On the other hand, the current flowing through the bottom MOSFETs (figure 6.11(d)) does not produce imbalances due to the characteristics and model of the MOSFET intrinsic diode.

2. The *rectangle* configuration (design ②) presents an identical current distribution for each MOSFET, both top (figure 6.11(b)) and bottom (figure 6.11(e)). The current simulations show some oscillations due to the increase of parasitic inductances. These oscillations can be produced by mathematical simulation (layout convergence problems with the semiconductor model) or real physical effects that must be controlled through the protections implemented on the driver.

3. The *butterfly* configuration (design ③) is the layout with the best current distribution, since the concept of symmetrical layout is applied. In addition, the current is distributed efficiently in the circuit. Therefore, the currents through the top (figure 6.11(c)) and bottom (figure 6.12(f)) MOSFETs are practically identical, which indicates the balance of the circuit. As it is previously mentioned, this design presents the highest values of inductances and parasitic resistances, which produce some oscillations, as in design ②. However, figures 6.11(c) and 6.11(f) show that these oscillations are smaller than in ②.

As already mentioned, the current flowing through each *SiC* MOSFET depends, among other factors, on the L_{ds} and R_{ds} values. These values are important to reduce, but according to the results obtained from simulations, they must be as similar as possible in order to reduce current imbalances, as it is recalled in the design criteria presented in chapter 5.



(a) Design ① - *linear* - top.

(b) Design ② - *rectangle* - top.

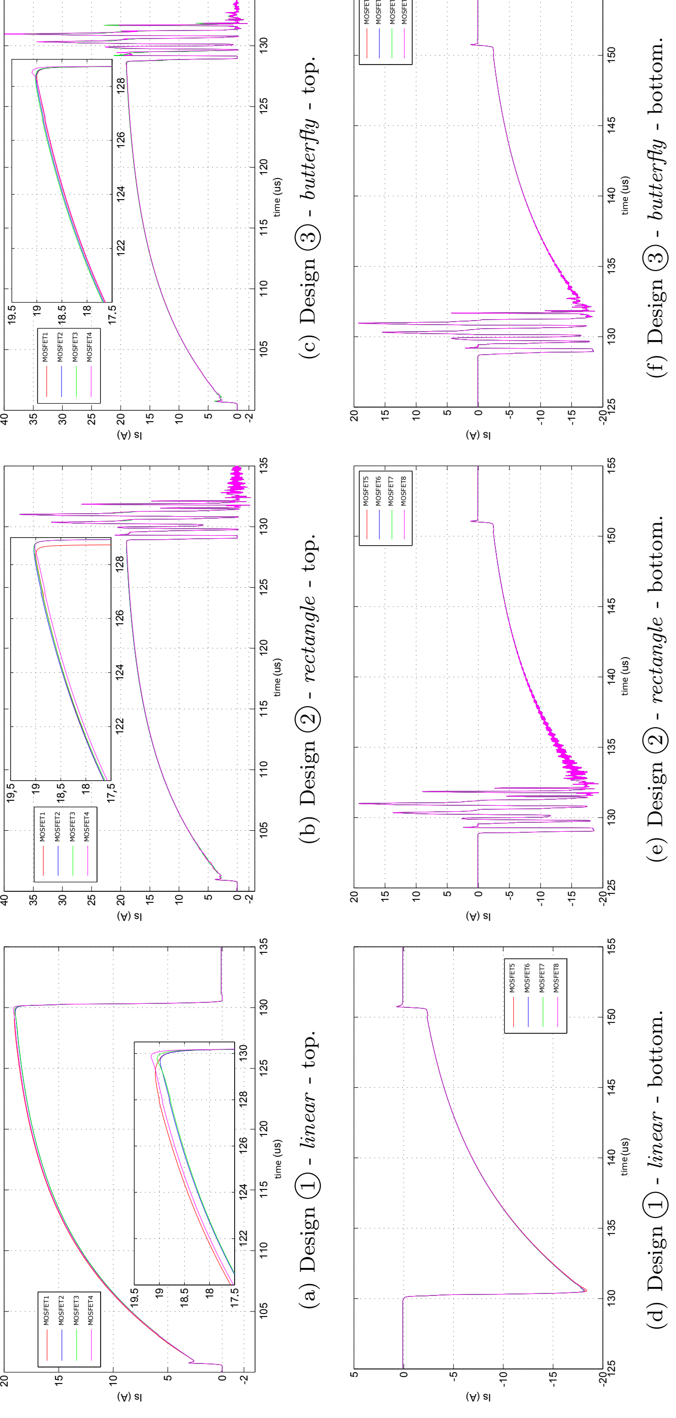
(c) Design ③ - *butterfly* - top.

(d) Design ① - *linear* - bottom.

(e) Design ② - *rectangle* - bottom.

(f) Design ③ - *butterfly* - bottom.

Figure 6.10: Signals between gates and driver (V_{gs}) for a half-bridge with 4 *SiC* MOSFETs in parallel at 20 kHz.



(a) Design ① - *linear* - top.

(b) Design ② - *rectangle* - top.

(c) Design ③ - *butterfly* - top.

(d) Design ① - *linear* - bottom.

(e) Design ② - *rectangle* - bottom.

(f) Design ③ - *butterfly* - bottom.

Figure 6.11: Current over the *SiC* MOSFETs top and bottom for each design at 20 kHz.

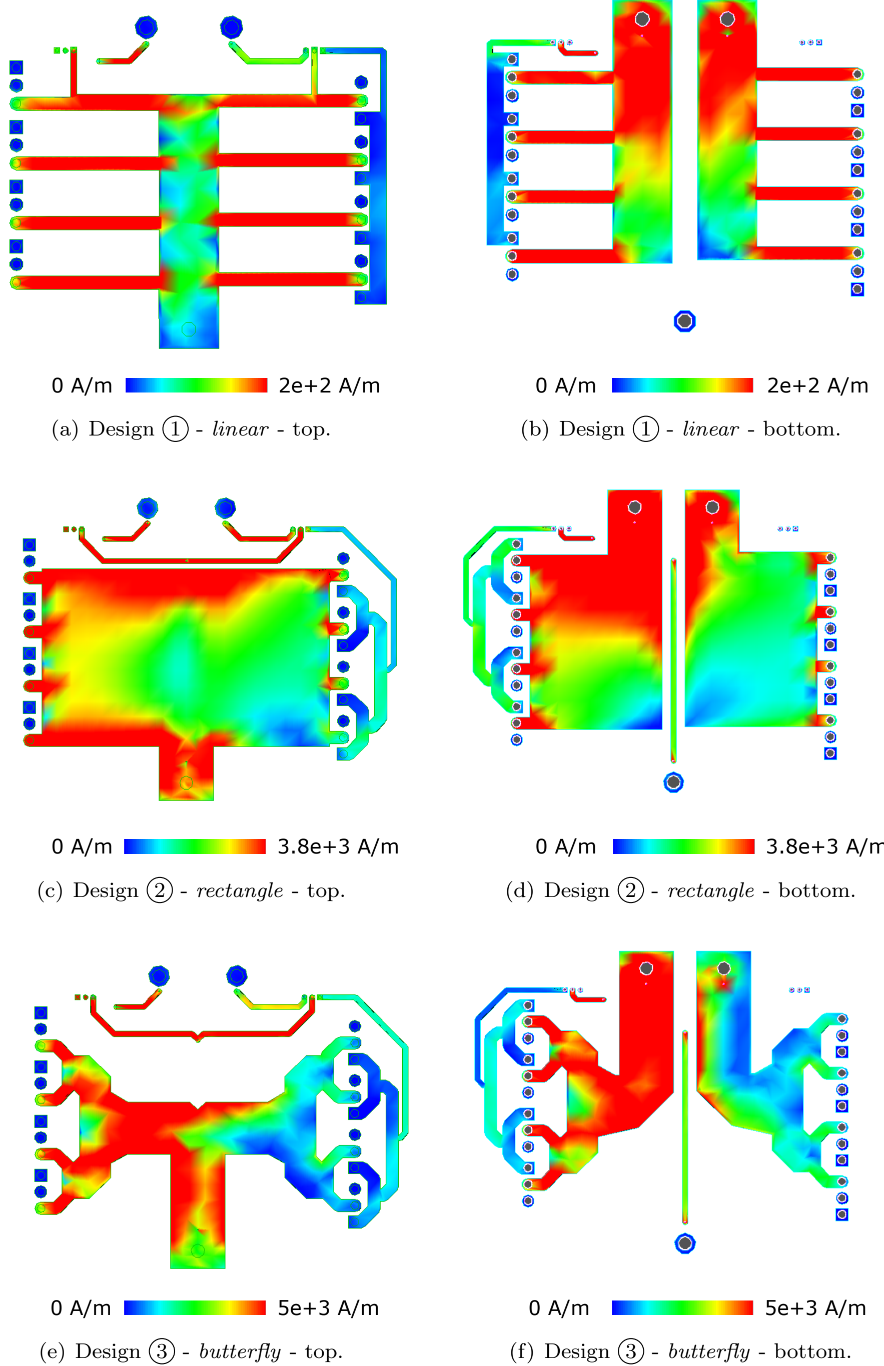
6.3.4 Half-bridge current density distributions

The current distribution in the designs depends on the parasitic impedances Z_{gs} and Z_{ds} (proportional to the dimensions, layout and materials among others), the gate V_{gs} voltages, and current propagation in the circuit. The 3D distribution of the current density allows to check the benefits of applying symmetrical connections:

1. The *linear* configuration (design ①) presents the worst current density distribution, since on the top layer (figure 6.12(a)) the current is concentrated in a path where transistors have not a common point of connection. Therefore, in the area where the MOSFET_4 source and MOSFET_8 drain are connected, the total current of all transistor flows. On the other hand, in the section where the MOSFET_1 source and the MOSFET_5 drain are connected, only the current of these devices flows. As for the bottom layer (figure 6.12(b)), through the connection of MOSFET_1 drain and MOSFET_5 source flow four times more current than the connection of MOSFET_4 drain and the MOSFET_8 source. Something similar happens with the traces that join the driver connectors with the MOSFET gates, where there is a higher current concentration in the gate section of the MOSFET_1 and MOSFET_5, instead of the MOSFET_4 and MOSFET_8 gates.

2. The *rectangle* configuration (design ②) presents a better distribution of the current density than ①. Its top layer (figure 6.12(c)) shows a similar distribution through the transistor top sources with the transistor bottom drains. The bottom layer (figure 6.12(d)) shows a similar behaviour, even though there is a higher concentration of current near the main terminals. In addition, both on the top and on the bottom layers, the current tends to flow around the edges of the design without taking advantage of the complete surface. As for the gate connections, by using a symmetrical design where each MOSFET has the same path length, the current is distributed homogeneously.

3. The *butterfly* configuration (design ③) presents the best distribution of current density, since a greater level of symmetry is implemented. In the top layer (figure 6.12(e)), the design employs a symmetric structure that connects the transistor top sources and bottom drains, thus forcing the current flow throughout. The same case happens on the bottom layer (figure 6.12(f)). Using the symmetric configuration of the design ② gates, the parasitic impedances of the *SiC* MOSFETs in parallel are practically similar, producing a more homogeneous current distribution.



(a) Design (1) - *linear* - top.

(b) Design (1) - *linear* - bottom.

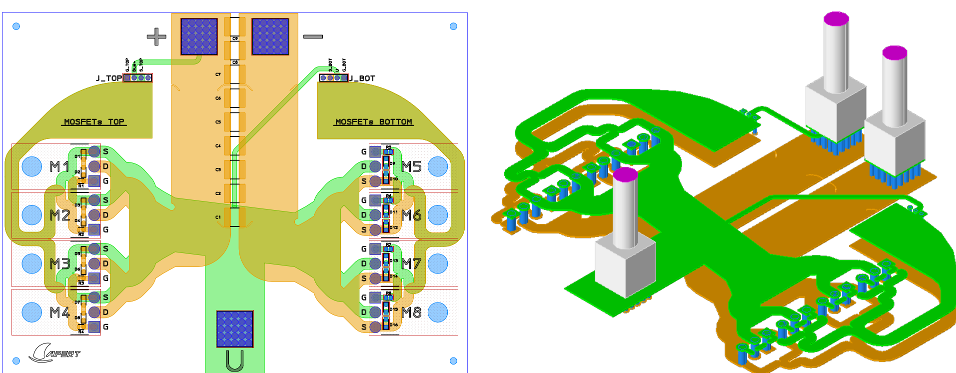
(c) Design (2) - *rectangle* - top.

(d) Design (2) - *rectangle* - bottom.

(e) Design (3) - *butterfly* - top.

(f) Design (3) - *butterfly* - bottom.

Figure 6.12: Current density distribution in top and bottom layers for each design at 20 kHz.



(a) Enhanced *butterfly* layout. (b) Enhanced *butterfly* 3D view.

(1) This layout includes gate circuit protection per semiconductor to protect gate MOSFETs from overvoltage: gate resistance and zener diodes.
(2) There are nine snubber capacitors between positive and negative bus terminals to mitigate bus parasitic inductance effects.
(3) RedCube Press-Fit power connectors are used to reduce their parasitic impedances and flow higher currents.

Figure 6.13: Enhanced butterfly design implementing round tracks and cutting edges.

6.3.5 Techniques to Round tracks and cutting edges

After studying the three half-bridge variations, the butterfly configuration (design ③) presents the best behaviour due to design symmetry where gate signals (V_{gs}) are practically identical and current (I_{ds}) are balanced, presenting the best current density distribution. Thess results are consequence of making the symmetrical connections explained in chapter 5. However, other techniques such as round tracks and cutting edges[1] can improve the circuit behaviour.

In order to illustrate the application of such techniques, some improvements and changes are applied over the *butterfly* configuration. The new layout[2] is shown in the figures 6.13(a) and 6.13(b). In this case, the substrate presents the top and bottom layer configuration of table 6.2. This new substrate configuration reduces absolute inductance values and reliability problems of the original *butterfly* half-bridge, which reinforce the idea that relative parasitic impedance values between parallelized semiconductors are more important than absolute values.

[1] These techniques are also indicated in chapter 5. They are also referenced as radio-freqquency techniques.

[2] This butterfly layout includes gate circuit protections, snubber capacitors and special power terminals. These components are necessary for a real implementation, they have been ignored in the extraction of parasitic impedances and voltage and current signals.

Table 6.2: Substrate materials used in the enhanced *butterfly* half-bridge.

Layer	Material	Thickness (mm)
Top	Copper	0.210$^{(*)}$
Dielectric	FR-4	2.780
Bottom	Copper	0.210$^{(*)}$

Table notes:
(*) The thickness of top and bottom layers are the double than in conventional 3.2 mm PCBs with two layers.

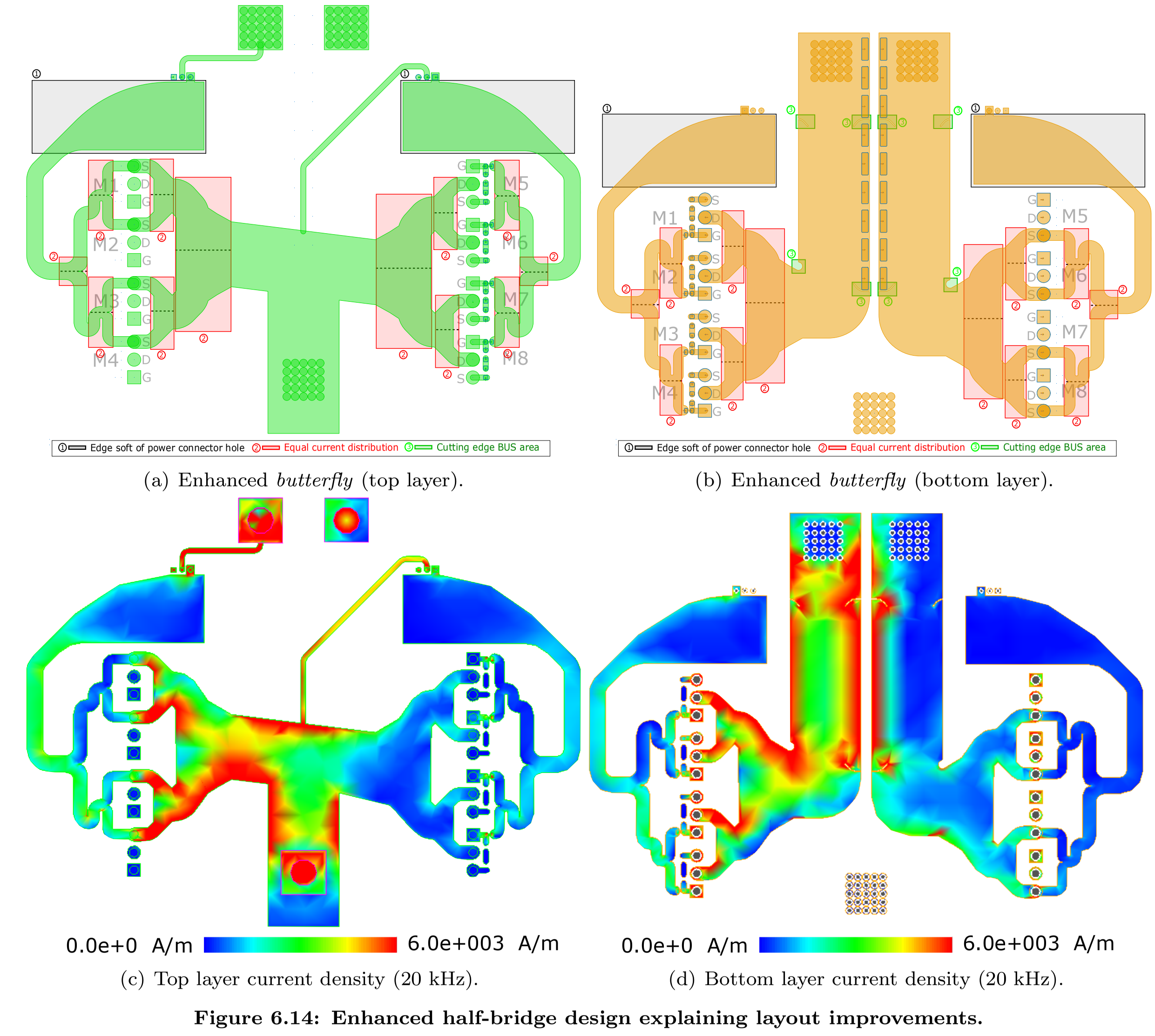
The details of the improvements applied in the layout circuit are shown in the figures 6.14(a) and 6.14(b), whose main objective is to improve current density distribution avoiding hot points:

(a) Top and bottom gate-source connections should reduce their closed loop parasitic inductance value, so wide copper areas (figures 6.14(a)-① and 6.14(b)-①) are added in top and bottom driver connectors. These areas also show a large curve softening the higher current density in the area edges. This behaviour can be observed in figures 6.14(c) and 6.14(d) for a current density at 20 kHz.

(b) The gate-source closed loops and drain-source closed loop should distribute device currents as equally as possible. For this reason, special structure implemented over top and bottom layers, figures 6.14(a)-② and 6.14(b)-②, divide equally the circuit currents. The round edge of these special divisions helps to reduce current density of these connections, thus balancing the closed loops. The results can be seen in the current concentration in the figures 6.14(c) and 6.14(d).

(c) The DC bus current must be distributed equally between positive and negative tracks. Both tracks present a high coupling effect, concentrating the current between the edges of positive and negative tracks. In order to reduce this consequence, some special cuts (figure 6.14(b)-④) are made to find a better current distribution between DC bus tracks. This homogeneous concetration is possible to see in the figure 6.14(d).

Applying the round and cutting techniques over a power layout helps to find a more homogeneous current density. The effects of these round forms and cuts are minimal over the design, as the figures of parasitic L_{gs} (figure 6.15(a)) and L_{ds} (figure 6.15(c)) show, where the inductance variations between *SiC* MOSFETs are less than 5 nH. The same behaviour is shown with equivalent parasitic resistances, R_{gs} (figure 6.15(b)) and R_{ds} (figure 6.15(d)). These parasitic impedance values produce that the gate signals (V_{gs}) for top and bottom *SiC* MOSFETs are practically equal, as figures 6.15(e) and 6.15(f) show, and their current imbalance is practically null, as figures 6.15(g) and 6.15(h) show.



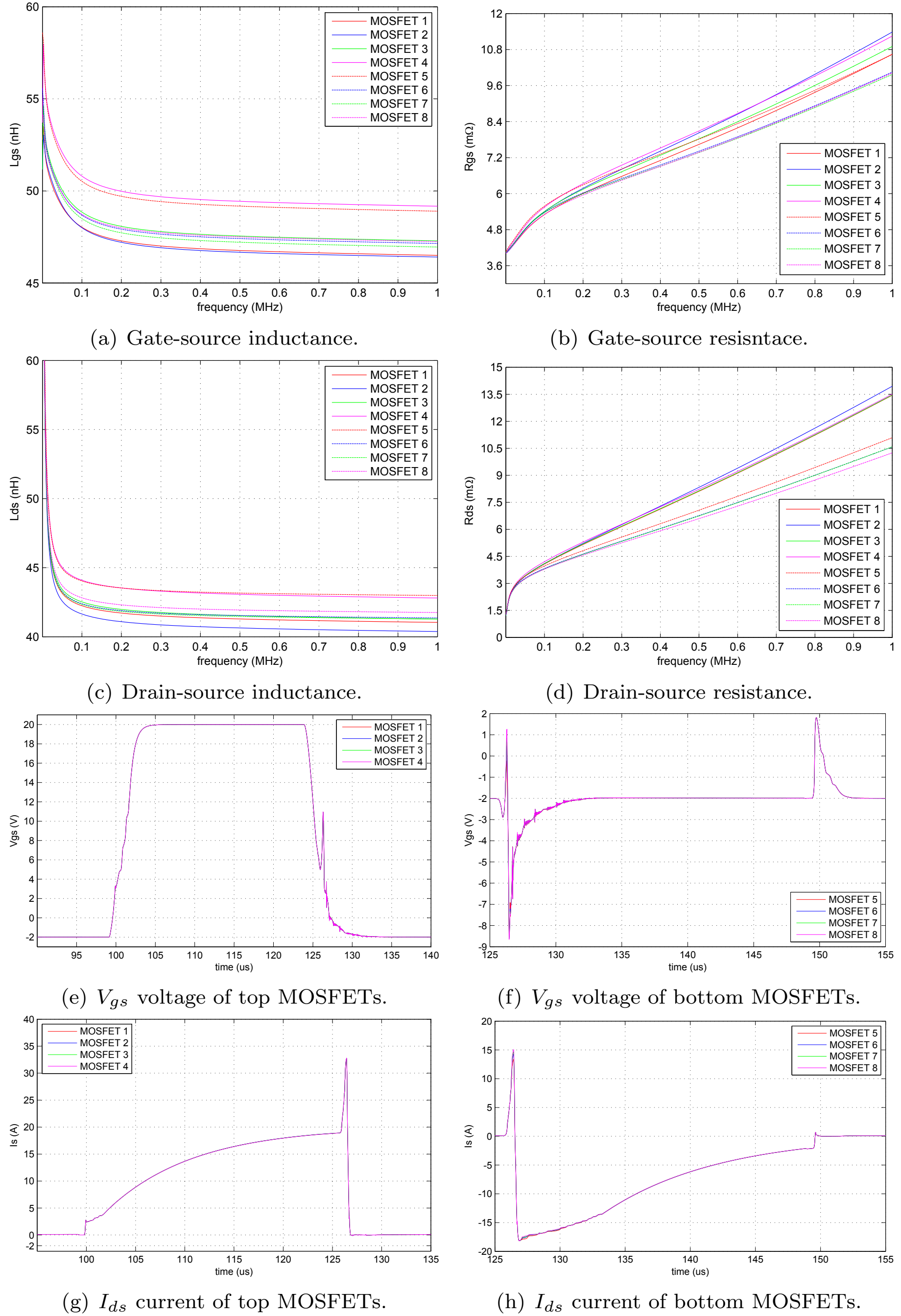
(a) Enhanced *butterfly* (top layer).

(b) Enhanced *butterfly* (bottom layer).

(c) Top layer current density (20 kHz).

(d) Bottom layer current density (20 kHz).

Figure 6.14: Enhanced half-bridge design explaining layout improvements.



(a) Gate-source inductance.

(b) Gate-source resisntace.

(c) Drain-source inductance.

(d) Drain-source resistance.

(e) V_{gs} voltage of top MOSFETs.

(f) V_{gs} voltage of bottom MOSFETs.

(g) I_{ds} current of top MOSFETs.

(h) I_{ds} current of bottom MOSFETs.

Figure 6.15: Enhanced *butterfly* half-bridge design closed loop impedances, gate signals and current *SiC* MOSFETS.

6.4 Multilayer DC bus design

The DC bus (composed by the DC-link and DC bus capacitors) is an important element of the power converter. Automotive and traction converters work at high switching frequencies, thus producing high *dv/dt* and *di/dt* [358, 370]. These effects are more critical in *SiC*-based MOSFET converters [371] than in *Si*-based IGBT converters [372]. This is why, decreasing stray impedance is fundamental to avoid overshoots, overvoltage spikes across power semiconductors and resonance effects between bus capacitors [373]. Apart from restricting the stray impedance with the DC bus shape and dimensions, using a multilayer structure [374] minimizes total parasitic inductance due to layer coupling effects. Thus, the power module design criteria developed in this thesis (chapter 5), the extraction of parasitic impedances and voltage and current analysis (figure 6.1(c)) can be applied in a DC bus design in order to attain the following goals [375]:

(a) Decreasing stray impedances, especially inductances.

(b) Balancing current capacitor branches [376, 377].

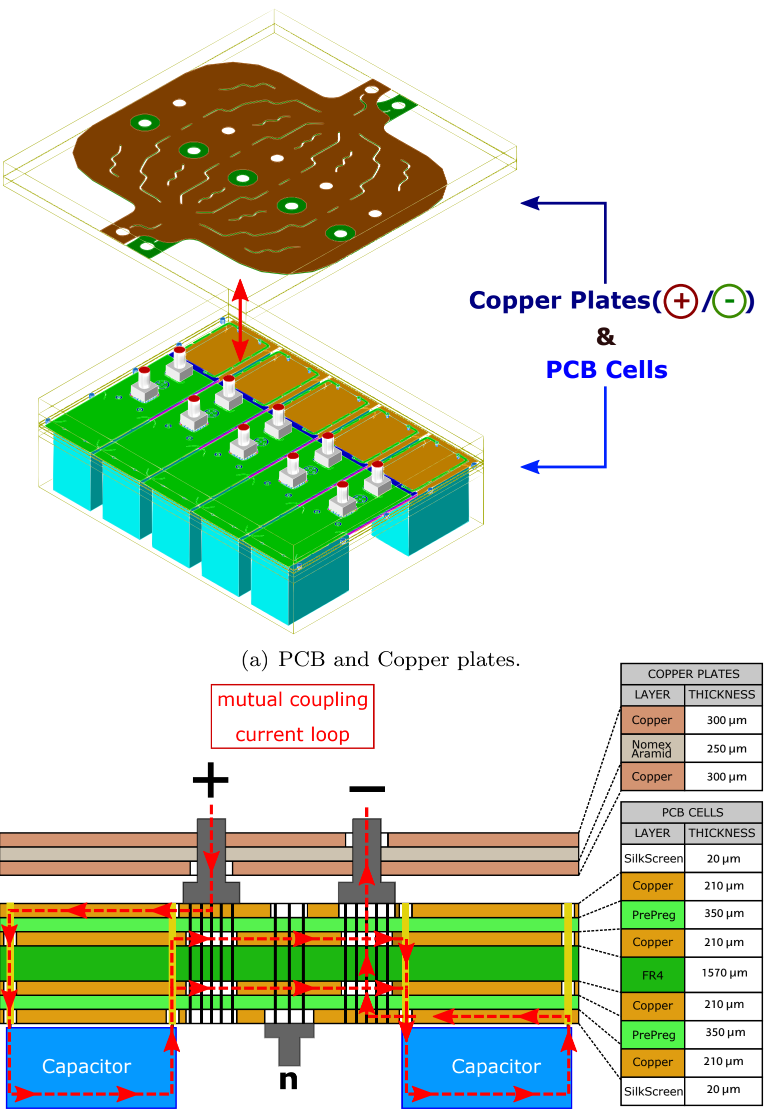
(c) Allowing scalability to obtain a standard structure for multiple applications.

Therefore, the present design has two main parts, as figure 6.1(c) shows:

1. PCB Cells (figure 6.16(a)): consisting of a PCB with 5 isolated capacitor cells [374]. Each cell has two capacitors (KEMET C4ATHBW5200A3NJ, 20 μF, 600 V and 29 A) in series, to get the voltage range for automotive (400/500 V) and traction (1000 V) applications, and resistances (1 MΩ) to balance the voltage between the two series capacitors. Figure 6.16(b) shows the different layers and thickness of this power PCB (3.2 mm total thickness).

2. Copper plates (figure 6.16(a)): these two copper plates (figure 6.16(b)), with a dielectric in the middle, connect the 5 parallel capacitor PCB cells, reducing the ripple current of capacitors, with and homogeneous current distribution [376].

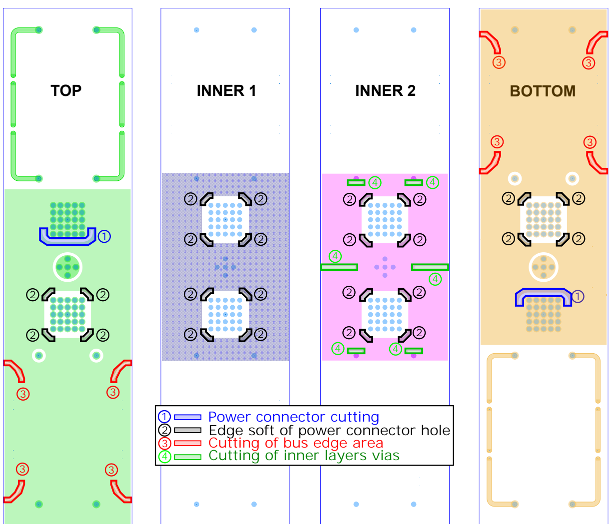
The following sections explain the design benefits of this DC bus made with a PCB and copper plates. These criteria are based on the device paralellization technique developed in the present thesis (chapters 4 and 5), showing that the concepts can be applied in other power electronic circuits apart from power modules, specially the application of cuts in order to get symmetrical paths with stray impedances as identical as possible.



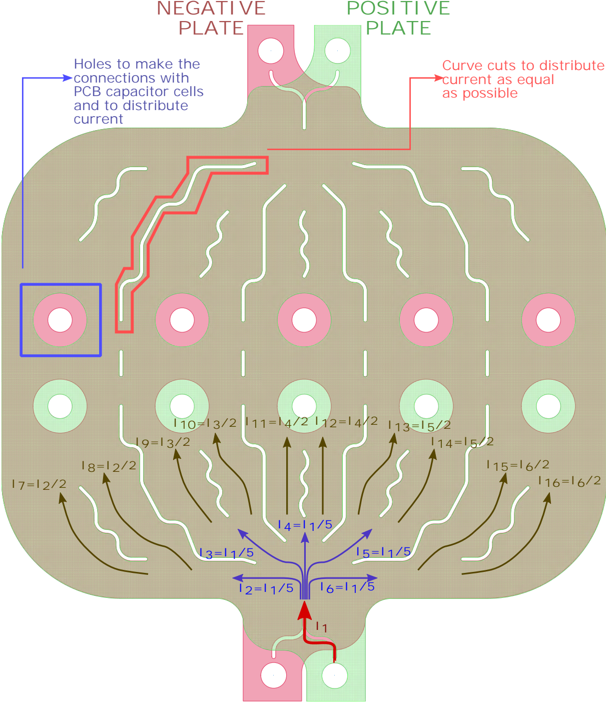
(a) PCB and Copper plates.

(b) Multilayer stackup with the current loop.

Figure 6.16: DC bus main structures and its multilayer substrate.



(a) Layout of each layer of the PCB cell.



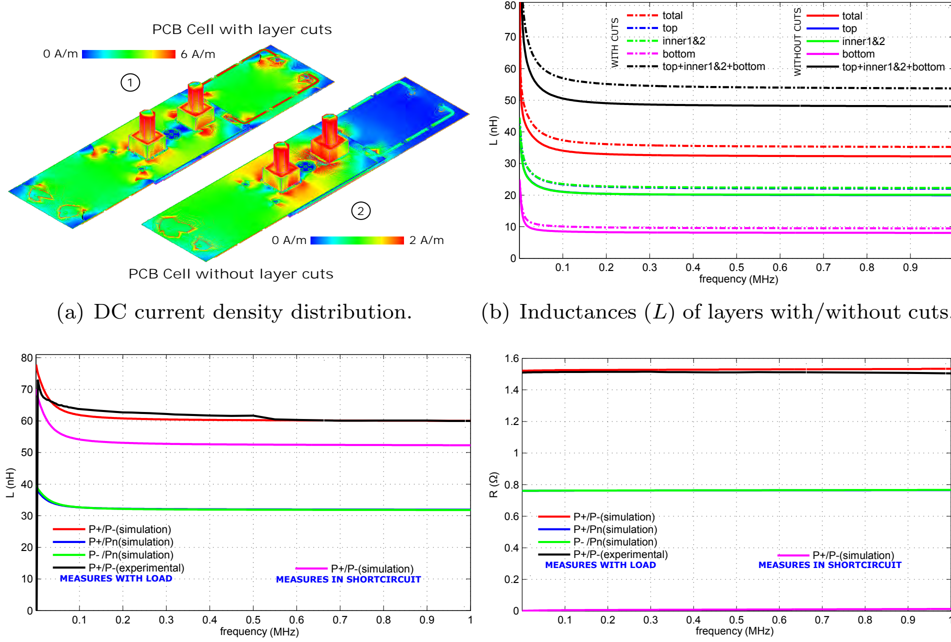
(b) Design of the two plates of copper.

Figure 6.17: Power multilayer PCB and copper plates.

6.4.1 Power multilayer PCB: stray inductance study

The capacitor cells have been designed with a PCB multilayer structure to satisfy the following criteria:

1. The material has to provide ease and flexibility for designers, so a PCB structure (figure 6.16(b)) is cheaper than a copper plate-based laminated busbar with dielectrics [378].
2. The design has to offer an easy scalability to be applied in other power applications. Therefore, this DC bus is divided in basic cells (figure 6.16(a)) to be added or subtracted according to application requirements.
3. The power connectors must be able to withstand high voltages and currents, as well as present low stray impedances, and be easily assembled on a PCB. Therefore, the RedCube Press-Fit connectors (300 A and 8 nH at 10 kHz) of CuZn39Pb3 alloy (62 nΩ· cm) have been selected.
4. The design must benefit from the mutual coupling effect to reduce stray inductances, thus a multilayer structure has been defined. Inside each capacitor cell, the current flows with opposite directions through each layer due to an internal loop (figure 6.16(b)), which provides high coupling.
5. The current distribution inside the cell has to be as homogeneous as possible to avoid thermal issues. Moreover, PCB designs cannot support high temperature, so a balanced current distribution is fundamental. With this aim, the different layers of the capacitor cell (figure 6.17(a)) have special cuts to get a good current distribution over the following copper areas:
   (a) The top and bottom layers have a cut in front of the power connector (figure 6.17(a)-①) to avoid a high current in only few connector pins, so current flows with better distribution through power connector.
   (b) The four layers (top, inner1, inner2 and bottom) have soft edges in the power connector clearance (figure 6.17(a)-②) to avoid high current densities in their vertices.
   (c) The top and bottom layers have wide and long copper areas, to achieve a good current distribution without high current densities in the borders of these areas. Rounded cuts (figure 6.17(a)-③) are made to control current density instead of increasing stray inductance.
   (d) The inner1 and inner2 layers are electrically connected. Due to the current loop, inner 2 has a higher current density. However, current must be distributed as equally as possible, so that rounded cuts are made (figure 6.17(a)-④) in inner2 to distribute the current between the layers.



(a) DC current density distribution.

(b) Inductances (L) of layers with/without cuts.

(c) Inductances (L) between power connectors.

(d) Resistances (R) between power connectors.

Figure 6.18: Capacitor cell simulations and experimental data.

The design criteria mentioned and layer cuts in the PCB capacitor cell produce an improvement of current distribution as figure 6.18(a)-① and figure 6.18(a)-② show. Layer cuts improve the current distribution, but they increase the parasitic inductance of each layer (figure 6.18(b)). However, this increase of stray inductance is assumable to get a better current distribution. Moreover, the effect of mutual coupling inductances due to internal current loop reduces the total parasitic inductance value, as figure 6.18(b) shows in the total value, which is less than the sum of each layer.

$$L_{total} < L_{top} + L_{inner1} + L_{inner2} + L_{bottom}. \tag{6.5}$$

The PCB capacitor cell is a circuit with low stray inductance (table 6.3) and low resistance values, according to simulation and experimental data. Figure 6.18(c) and figure 6.18(d)) compare the experimental total values (P+/P- experimental) with different simulation measures between main terminals: positive-negative (P+/P- load), positive-neutral (P+/Pn load), negative-neutral (P-/Pn load) and positive-negative (P+/P- short-circuit)[1].

[1]It is important to indicate that test and simulations have been done done with 1.5 Ω and 8 nH to be able to obtain the inductance values of PCB without high-pass capacitor effects.

6.4.2 Copper plates: stray inductance study

These two copper plates (positive and negative, figure 6.17(b)) connect in parallel the isolated capacitor cells of the power PCB. As in the case of PCB capacitor cells, the copper plates have been designed to satisfy the following design criteria:

1. The structure has to present low resistance and inductance values to minimize the total impedance of DC bus, so two copper plates of 300 μm have been used (figure 6.16(b)).
2. The mutual coupling effect has to be exploited in order to reduce the total inductance value. For this reason, both copper plates have to be as symmetric as possible with same dimensions (figure 6.17(b)). Moreover, the current of each layer must flow with different direction, so a high coupling effect appears between both plates.
3. The plates must distribute the current as equal as possible between capacitor branches, since a higher current in a particular cell or a wide imbalance between them could produce PCB crystallisation and capacitor thermal break. To achieve all this, the design must implement the following cuts, as in figure 6.17(b):
   (a) The holes, which connect copper plates with the positive and negative terminals of PCB cell power connectors, must be circles to improve the current flow.
   (b) The copper cuts must be employed to make as equal as possible the distances and dimensions between PCB cells connectors and the main power DC bus inputs/outputs.

According to these requirements, the copper layers present an improvement in the current distribution due to the holes and cuts, as figures 6.19(a)-①-③ show. The rounded holes connect copper plates with PCB cells, producing by default a good current distribution (figure 6.19(a)-②) because circular structures are not major obstacles for current flow. However, this current distribution can be improved with the copper cuts (figure 6.19(a)-③). These cuts increase the stray inductance value of each copper plate (figure 6.19(b)), but they improve current distribution. Moreover, the mutual coupling effect produces a low stray inductance (figure 6.19(b)).

$$L_{total} < L_{positive} + L_{negative}. \tag{6.6}$$

Finally, different measures between the main terminals (figure 6.19(c) and figure 6.19(d)) with/without external load (1.5 Ω and 70 nH) verify the low resistance and inductance values of these copper plates, which are 2 mΩ and 15 nH in shortcircuit.

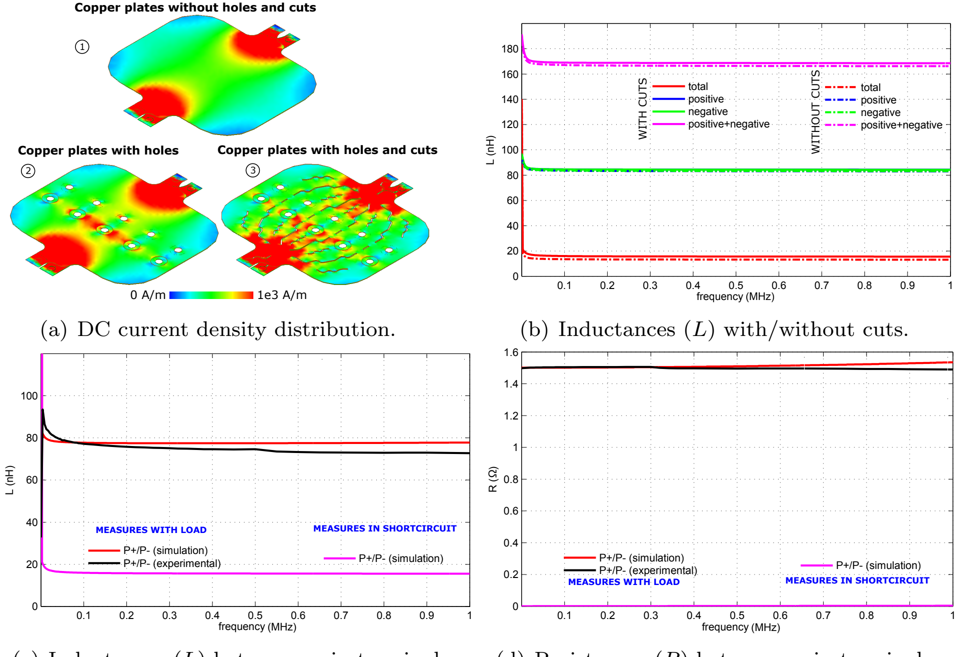


Figure 6.19: Copper plates simulations and experimental data.

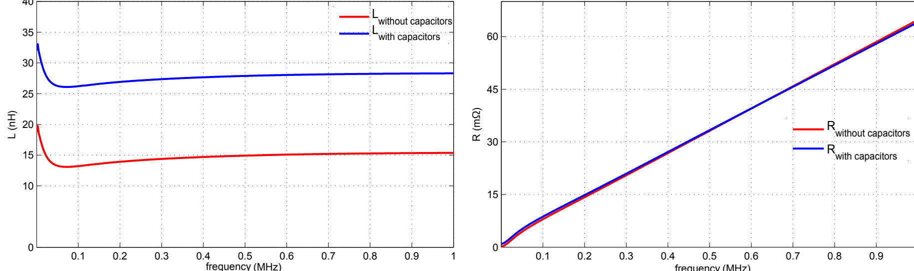
6.4.3 DC bus assembly

The union of the two parts of the design, PCB capacitor cells and copper plates, forms the total DC bus structure (figure 6.16(a)). The positive and negative copper plates connect in parallel the 5 PCB cell branches of the DC bus. The stray impedance value of the full structure is lower than each part of the design due to this parallel connection with its coupling effects [379]. For example, table 6.3 shows a comparative of each partial structure and the full design taking into account or not the values of ESL and ESR capacitors. The parasitic inductance and resistance values of the full structure with/without the stray impedance of the 10 capacitors are shown in the figure 6.20(a) and figure 6.20(b), respectively.

These stray impedances of this DC bus are higher than some market solutions, which have inductances between 15-20 nH. However, these solutions cannot be customized easily depending on voltages and currents of the power applications. In this DC bus, the current level can be modified adding or subtracting the number of PCB capacitor cells and voltage levels using different capacitors. Moreover, the design has a symmetrical layout to balance the current in each part, so capacitors are going to provide a similar current, the same concept than in semiconductor paralellization.

Table 6.3: Parasitic impedances values at 10 kHz.

Structure	L (nH)	R (mΩ)
PCB cell	64.8	126
Copper plates	18.4	67
Full structure (without stray capacitor impedances)	17.2	68
Full structure (with stray capacitor impedances)	30.3	145



(a) Inductances (L) with/without capacitors. (b) Resistances (R) with/without capacitors.

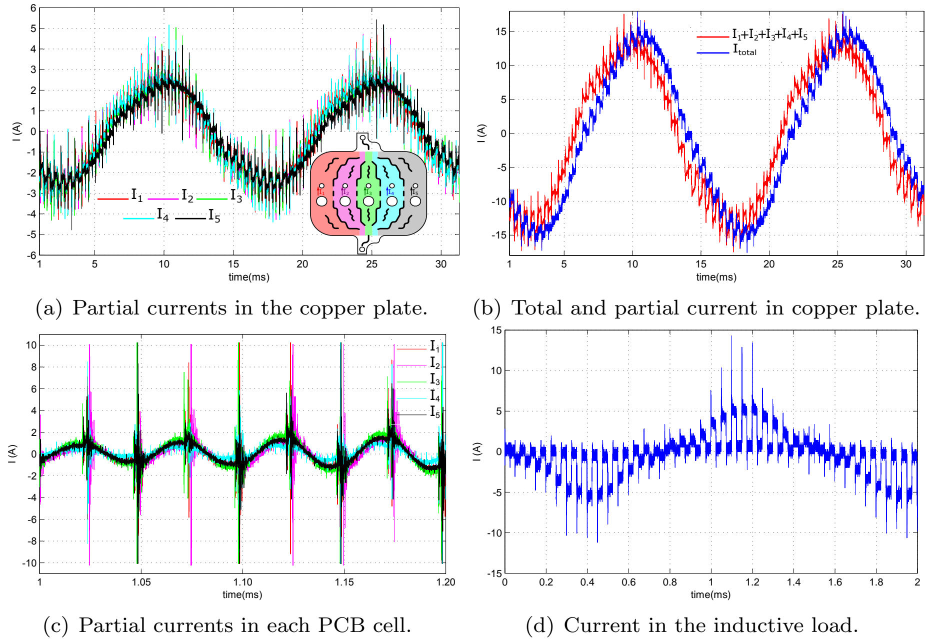
Figure 6.20: Impedance values of PCB cells + copper plates.

6.4.4 Current balance and current density distribution

In this design, it is fundamental to find a current distribution as homogenous as possible to avoid problems (e.g. hotspots) with PCB cell branches, since they are made of FR4 dielectric and any current imbalance or higher concentration can produce a thermal breakdown. For this reason, copper plates have to divide the current as equal as possible between PCB cells.

In order to check that copper plates divide equally the current, a signal of 16 App and 660 Hz flows through a copper plate. Different current measures are made in the points where PCB cells have to be connected. The results of each partial current are shown in the figure 6.21(a). These results verify that the copper plate makes a good current division, since high imbalances are not appreciated. Moreover, figure 6.21(b) shows a comparative between the total current and the sum of each partial current; this test indicates that losses are very low because both signals have the same amplitude. Finally, figure 6.21(c) shows the current per each PCB cell when the DC bus is connected to a power converter with 600 V_{dc} and a current in the inductive load (figure 6.21(d)). The signals of figure 6.21(c) are similar, without large current imbalances, so the 5 PCB cell branches are balanced and each one provides, the same current for the DC bus.

Other important point to be tested is the current density distribution. A single PCB cell and the copper plates have been tested independently (to avoid long computing times in ADS^{TM} simulation platform). Each part of the design is con-



(a) Partial currents in the copper plate.

(b) Total and partial current in copper plate.

(c) Partial currents in each PCB cell.

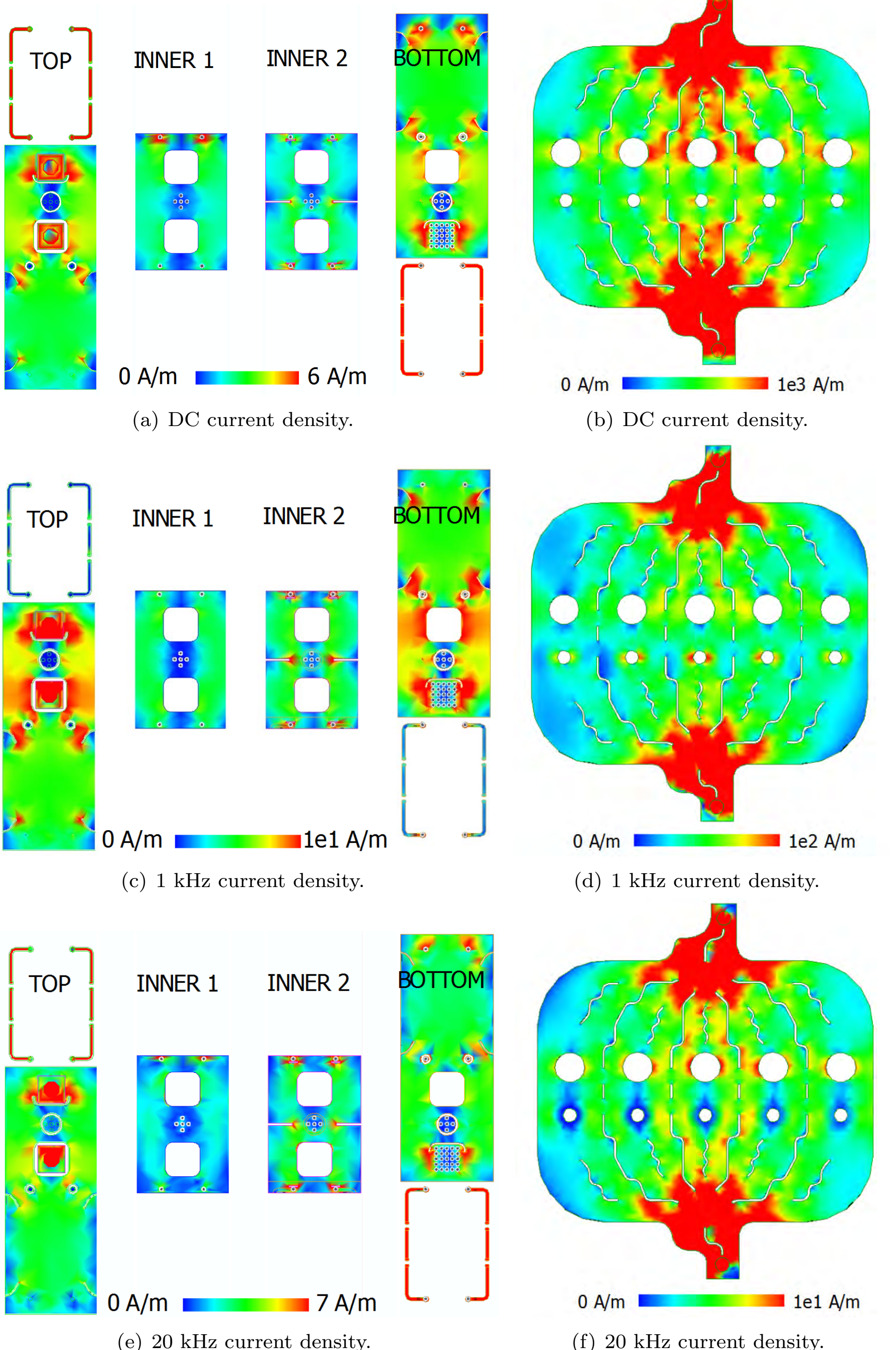
(d) Current in the inductive load.

Figure 6.21: Current measures in copper plate and PCB cell.

nected to a simplified circuit emulating a power converter. This circuit consists of a voltage source of 600 V (1 Ω and 2 μH) and a current source of three spectral components: DC (0 Hz), 1 kHz and 20 kHz with amplitude of 200 A, 50 A and 5 A, respectively.

The current density simulations of the PCB cell at different frequencies (figure 6.22(a), figure 6.22(c) and figure 6.22(e)) allow to detect areas with a higher current density. Due to design criteria, specially internal cuts of layers, the PCB cell does not show wide current imbalances. In figure 6.22(a), figure 6.22(c) and figure 6.22(e), the critical points are PCB vias and power connectors, but these always have higher current density because of being points with high current flux.

Finally, the figure 6.22(b), figure 6.22(d) and figure 6.22(f) show the current density distribution of the positive copper plate. The negative copper plate is not shown because of its symmetry, which presents identical current density values. As in the PCB cell case, due to holes and cuts, the current does not show wide current imbalances at different frequencies. Moreover, the figure 6.22(b), figure 6.22(d) and figure 6.22(f) show similar current distribution at different frequencies, so copper plates produce a good current division between the 5 cell branches. It is clear that cell branches of borders do not have the same current than the centre branch. However, the difference is not critical as figure 6.21(a) and figure 6.21(c) display.



(a) DC current density.

(b) DC current density.

(c) 1 kHz current density.

(d) 1 kHz current density.

(e) 20 kHz current density.

(f) 20 kHz current density.

Figure 6.22: Current density distribution at different frequencies in the layers of PCB cell capacitors and in the positive copper plate.

6.5 Conclusions

In this chapter three power circuits have been proposed. The design criteria developed in chapter 5 have been applied, where the parallelization factors summarised in chapter 4 and symmetry layout distribution have been applied.

The power switch case shows that connections between parallelized devices are critical in order to avoid detrimental feedback effects and control-power signals coupling problems. As it is specified in this chapter, a *square* configuration, where tracks are as equally as possible, exhibits the best behaviour. Although this circuit does not show the lowest stray impedance values, their values are practically identical between devices. This *square* configuration is a good example of symmetry application, where connections are balanced without voltage control signal delays and wrong power signal current distributions.

The case of half-bridge topology is a step forward in the application of power module design criteria, because the increase in the number of devices and a two-level configuration imply a greater difficulty level. The three half-bridge proposals of this chapter are examples of parallelization and symmetry evolution. They show that layout signals can be managed through the circuit in order to get the best balance for the specific application requirements, as the proposed *butterfly* configuration. Moreover, the current density distribution can be improved using radio frequency techniques (round and cuttings edge) without changing drastically track stray impedance values.

The DC bus circuit shows that the design criteria for the parallelization of power semiconductors can also be used in other power circuits. The capacitors are connected through wide copper areas with low stray inductances, where the current flows homogeneously due to application of special cuts and soft edges, avoiding current imbalances between capacitors. Moreover, the usage of two substrate technologies is also adopted by power modules in order to improve coupling effects and increase the routing area, thus easing the electrical connections.

Finally, the circuit examples developed in this chapter are made with PCB substrate, which provides a major design flexibility to designers in order to test and modify circuits. These examples provide the previous knowledge in order to apply design criteria developed in this thesis to a power module configuration (DBC substrate).

Chapter 7

SiC half-bridge module development based on the proposed design criteria

7.1 Introduction

The development of a power module for the automotive industry is a complicated task due to, among other issues, the lack of a specific and exhaustive solution, where all design parts are completely defined. The advice and tips of the literature are focused on general ideas, where applying symmetry is the most important concept in order to design a power module. However, this implementation concept is not usually completely defined. Moreover, each manufacturer uses its own constraints and technology, restricting the access to these industrial/commercial solutions. In fact, chapter 5 presents some power module design criteria in order to solve this lack of information.

Plenty of these criteria are checked in chapter 6 through PCB circuits where the parallelization is applied over a power switch and a half-bridge circuit, apart from getting homogeneous current distributions thanks to the symmetry. Nevertheless, these design criteria need to be put into practice with a power substrate and semiconductor bare dies according to mechanical and structural constraints (mechanics), instead of discrete devices and a PCB substrate, where electrical connections and physical dimensions of the encapsulation reduce designer freedom.

For these reasons, this chapter presents the electrical and thermal characterization of two half-bridge power modules, according to the criteria developed in chapter 5. The application of each design concept is explained and checked through the extraction of parasitic impedances using simulation tools. Moreover, voltage and current signals are extracted through co-simulation between *SiC* devices (manufacturer electrical models) and power module layouts, as well as surface current density. Finally, the thermal behaviour of power layout and substrate is evaluated through a methodology combining 1D and 3D thermal simulations under driving cycle profiles (appendix B).

7.2 Electrical characterization: layouts according to the proposed design criteria

According to the defined power module design criteria (chapter 5) and to the data extracted from some power designs (chapter 6), in this chapter two proposals of a *SiC* half-bridge with maximum voltage and current ranges of 1700 V/160 A are presented, analysing their electrical and thermal behaviours.

Both power module proposals have the same physical dimensions, substrate configuration and materials, number of power and control terminals[1], quantity of *SiC* MOSFETs (CPM2-1700-0045B[2]) and *SiC* diodes (CPW5-1700-Z050B[3]) in parallel. The main differences between both proposals lie on the gate attack and the power layout connections, as well as the amount of passive elements. These two proposals are the following:

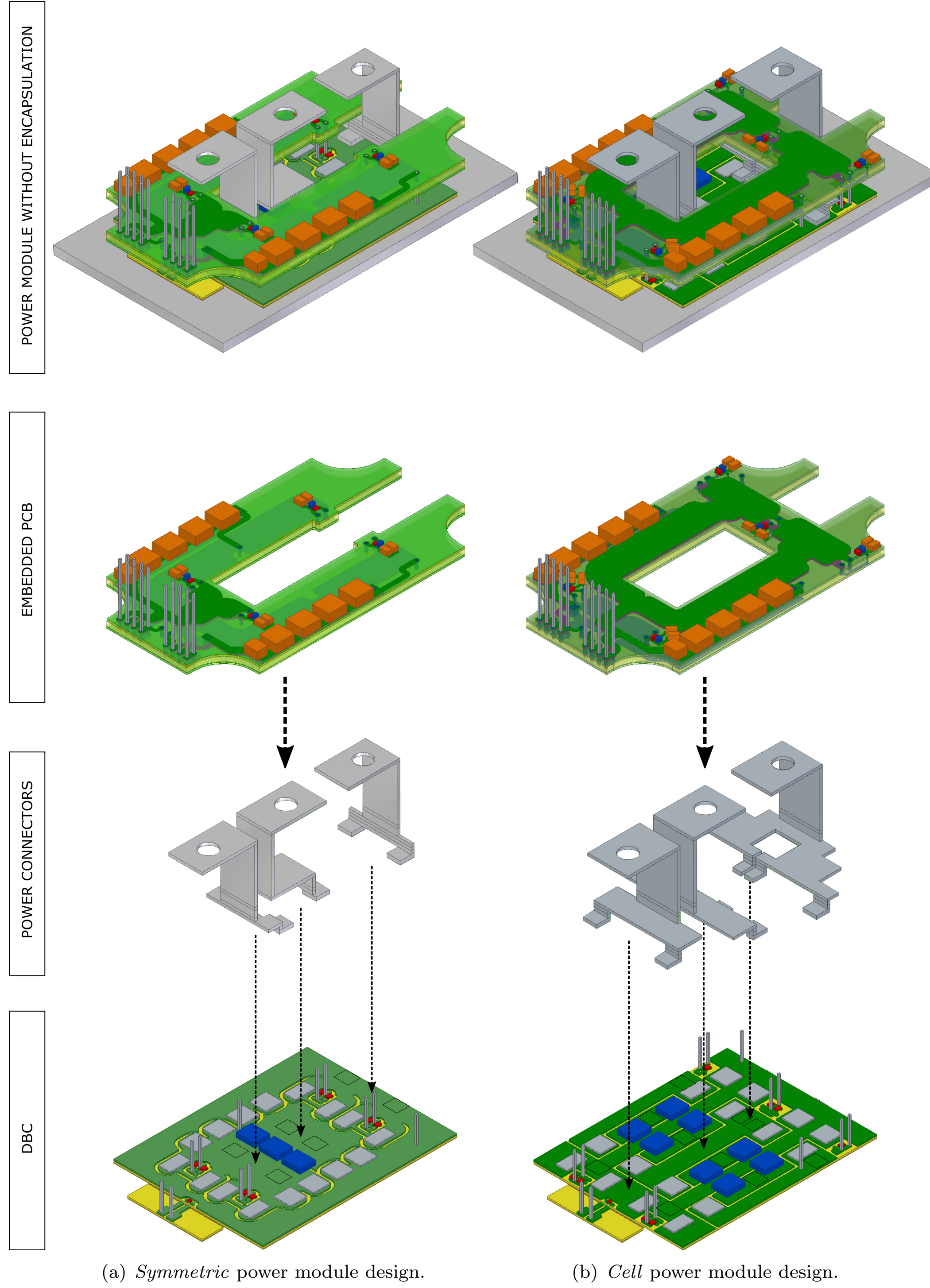
- *Symmetric* design (figure 7.1(a)): it is based on a rigorous symmetry application over the power layout in order to balance switching loops. Moreover, circuit tracks and areas are implemented trying to reduce parasitic inductances.
- *Cell* design (figure 7.1(b)): it is based on the usage of P-Cell and N-Cell concept, which reduces the distance between MOSFETs and the corresponding diode (figure 7.2), placing the top MOSFET with the bottom diode as close as possible, and viceversa, and using snubber capacitors in order to decrease parasitic inductances of switching loops.

The solutions presented are a hybrid configuration where two kind of substrate technologies are interconnected in order to improve standard solutions (inorganic

[1] The same number of external auxiliary terminals: there is a variation in the number of the internal auxiliary terminals in order to connect PCB and DBC substrates.

[2] The Wolfspeed (Cree) *SiC* MOSFET: 1700 V/72 A@25^{0}C - 1700 V/48 A@100^{0}C.

[3] The Wolfspeed (Cree) *SiC* diode: 1700 V/50 A@150^{0}C.



(a) *Symmetric* power module design. (b) *Cell* power module design.

(*) Wire bondings are excluded in these views in order to focus on other details visibility.

Figure 7.1: Proposed *SiC* half-bridge power module designs

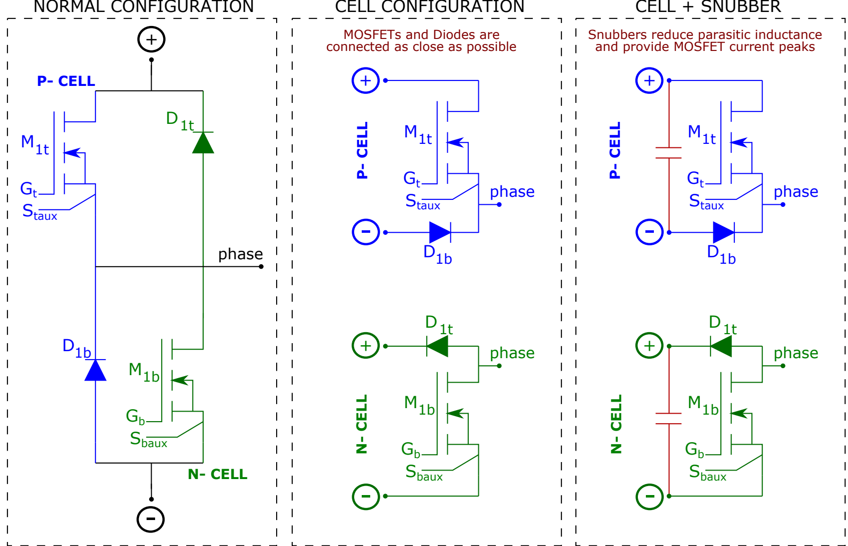
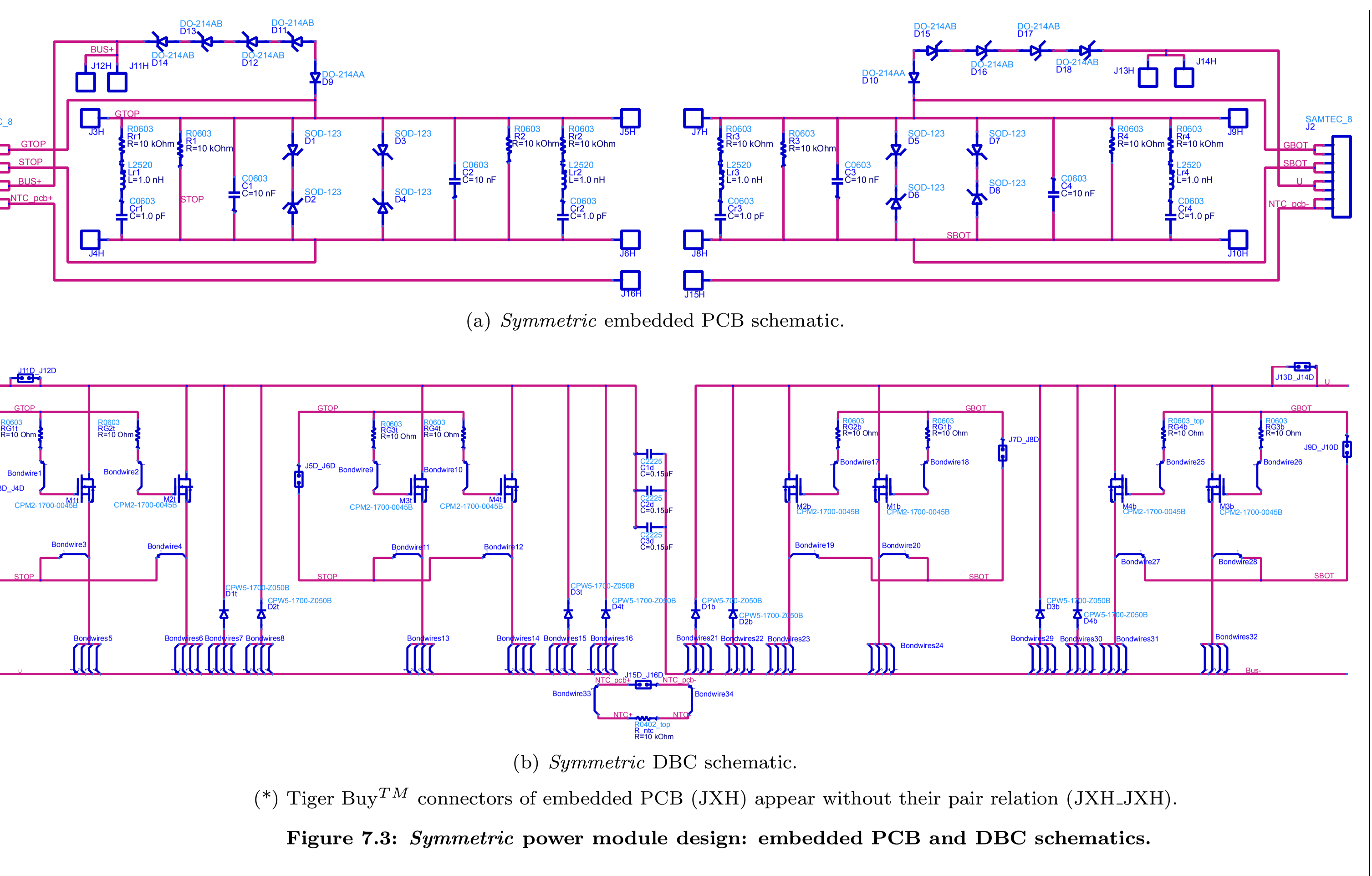


Figure 7.2: P-Cell and N-Cell configuration.

substrates such as DBC, DBA and AMB). Figures 7.1(a) and 7.1(b) show the interconnection between power module main parts and substrates (embedded PCBs, power connectors and DBC power layouts) of the *symmetric* and *cell* solutions, respectively.

The *symmetric* half-bridge schematics for embedded PCB and DBC circuits are shown in figures 7.3(a) and 7.3(b), respectively, whose components are summarised in the table 7.1. Similarly, the *cell* half-bridge schematics for embedded PCB and DBC are shown in the figures 7.4(a) and 7.4(b), summarising their components in the table 7.2. For the development of power modules, knowing component footprints is fundamental because they determinate the dimensions to establish the electrical connections, being less critical the specific value of each component. In fact, component values must be calculated or customised according to operating conditions in terms of voltage, current, switching frequencies and others.

Once the general vision and circuits of each *SiC* half-bridge are presente, in the following sections each power module part is defined in detail according to the design criteria developed in chapter 5. The application of these criteria is checked thanks to the extraction of design equivalent impedance values, electrical behaviour and current density distribution using ADS^{TM} Keysight simulation tool.

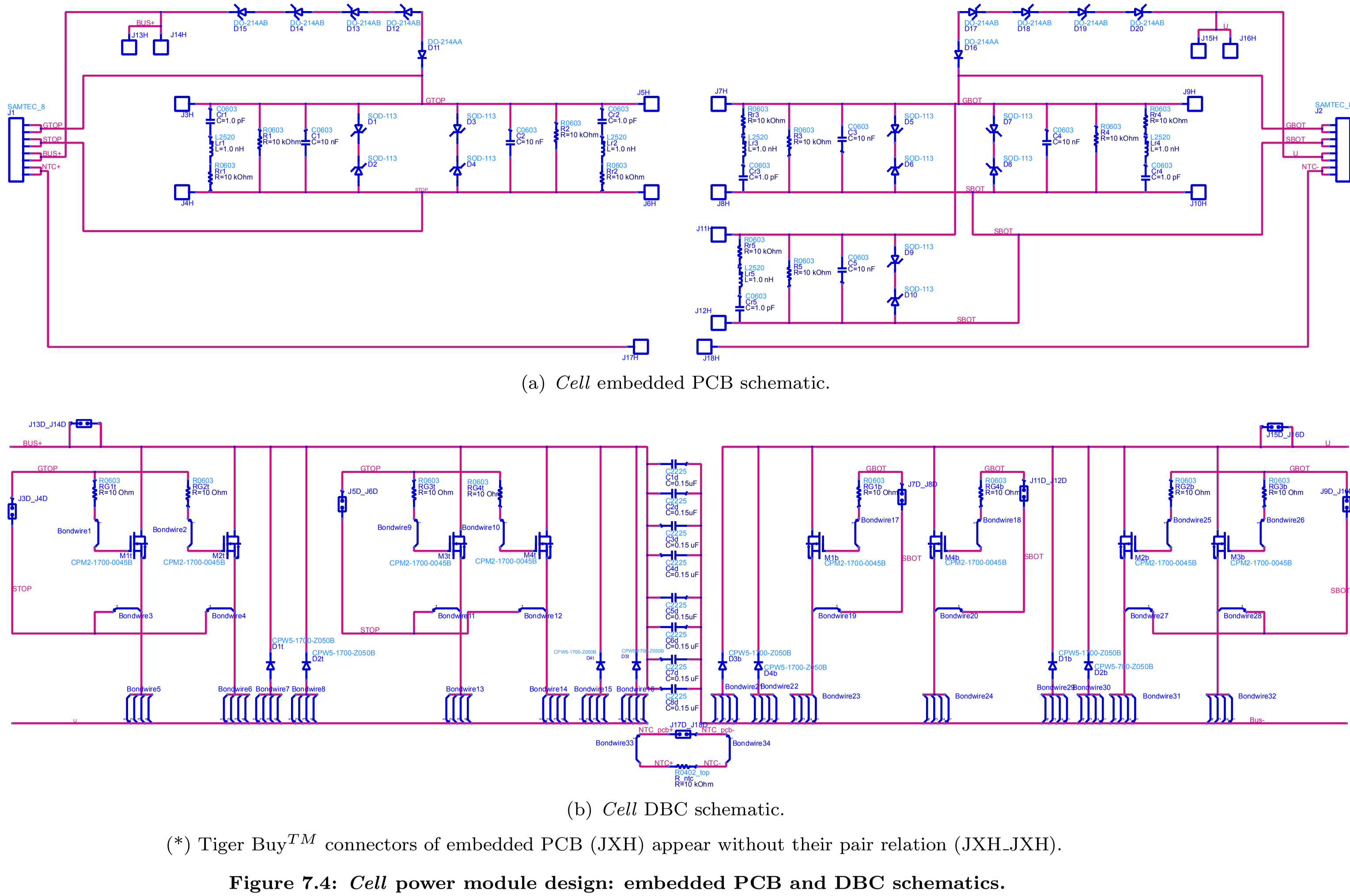


(a) *Symmetric* embedded PCB schematic.

(b) *Symmetric* DBC schematic.

(*) Tiger Buy^{TM} connectors of embedded PCB (JXH) appear without their pair relation (JXH_JXH).

Figure 7.3: *Symmetric* power module design: embedded PCB and DBC schematics.



(a) *Cell* embedded PCB schematic.

(b) *Cell* DBC schematic.

(*) Tiger Buy^{TM} connectors of embedded PCB (JXH) appear without their pair relation (JXH_JXH).

Figure 7.4: *Cell* **power module design: embedded PCB and DBC schematics.**

Table 7.1: *Symmetric* power module design components.

Symmetric embedded PCB: figure 7.3(a)				
Item	**Name/Alias**	**Schematic ref.**	**Part value(1)**	**Footprint**
1	C_{gs} gate clamping	C1, C2, C3, C4	10 nF/50 V/X7R	C0603
2	R_g gate clamping	R1, R2, R3, R4	10 kΩ	R0603
3	TVS active clamping (gate)	D1, D3, D5, D7	SMF6.0A	SOD-123
4	TVS active clamping (source)	D2, D4, D6, D8	SMF22A	SOD-123
5	TVS active clamping(2)	D11, D12, D13 D14, D15, D16 D17, D18	SMCJ130A	DO-214AB
6	Diode active clamping(3)	D9, D10	GB02SLT12-214	DO-214AA
7	Square post connector (4)	J1, J2	HTSW-104-11-G-D	SAMTEC_8
8	Tiger Buy^{TM} connector(5)	J3H_J4H J5H_J6H J7H_J8H J9H_J10H J11H_J12H J13H_J14H J15H_J16H	SQT-102-03-G-S	SAMTEC_2
9	R_{oscil} gate-source(6)	Rr1, Rr2 Rr3, Rr4	10 kΩ	R0603
10	L_{oscil} gate-source(6)	Lr1, Lr2 Lr3, Lr4	1 nH	L2520
11	C_{oscil} gate-source(6)	Cr1, Cr2 Cr3, Cr4	1 pH	C0603

Symmetric DBC: figure 7.3(b)(7)				
Item	**Name/Alias**	**Schematic ref.**	**Part value(1)**	**Footprint**
1	Bare die *SiC* MOSFET	M1t, M2t M3t, M4t M1b, M2b M3b, M4b	CPM2-1700-0045B	CPM2-1700-0045B
2	Bare die *SiC* Diode	D1t, D2t D3t, D4t D1b, D2b D3b, D4b	CPW5-1700-Z050B	CPW5-1700-Z050B
3	C_{dc} snubber capacitors	C1d, C2d, C3d	0.15 μF/1 kV	C2225
4	Rg_{int} gate resistance	RG1t, RG2t RG3t, RG4t RG1b, RG2b RG3b, RG4b	10 Ω/1 %/0.250 W	R0603
5	R_{NTC} temperature sensor	R_{NTC}	10 kΩ/1 %/70 mW	R0402
6	Square post connector(5)	J3D_J4D J5D_J6D J7D_J8D J9D_J10D J11D_J12D J13D_J14D J15D_J16D	TW-10-07-L-D-300-SM	SAMTEC_2
7	Power connectors	Bus+, Bus-, U	(8)	(8)

Table notes:
(1) These values are taken as reference.
(2) TVS for automotive and traction applications: SMCJXXA.
(3) Fast *SiC* diode.
(4) Driver connection, connector 4x2 and pitch 2.54 mm (SAMTEC).
(5) Embedded PCB and DBC interconnection, pitch 2.00 mm (SAMTEC).
(6) RLC filter in order to reduce gate *SiC* MOSFETs oscillations. The components must be experimentally tuned in.
(7) Wire bondings are not included in the table.
(8) Power connectors are not included in the schematic (custom design).

Table 7.2: *Cell* **power module design components.**

Cell embedded PCB: figure 7.4(a)				
Item	**Name/Alias**	**Schematic ref.**	**Part value(1)**	**Footprint**
1	C_{gs} gate clamping	C1, C2 C3, C4, C5	10 nF/50 V/X7R	C0603
2	R_g gate clamping	R1, R2 R3, R4, R5	10 kΩ	R0603
3	TVS active clamping (gate)	D1, D3 D5, D7, D10	SMF6.0A	SOD-123
4	TVS active clamping (source)	D2, D4 D6, D8, D10	SMF22A	SOD-123
5	TVS active clamping(2)	D12, D13, D14 D15, D16, D17 D18, D19, D20	SMCJ130A	DO-214AB
6	Diode active clamping(3)	D11, D16	GB02SLT12-214	DO-214AA
7	Square post connector (4)	J1, J2	HTSW-104-11-G-D	SAMTEC_8
8	Tiger Buy^{TM} connector(5)	J3H_J4H J5H_J6H J7H_J8H J9H_J10H J11H_J12H J13H_J14H J15H_J16H J17H_J18H	SQT-102-03-G-S	SAMTEC_2
9	R_{oscil} gate-source(6)	Rr1, Rr2 Rr3, Rr4, Rr5	10 kΩ	R0603
10	L_{oscil} gate-source(6)	Lr1, Lr2 Lr3, Lr4, Lr5	1 nH	L2520
11	C_{oscil} gate-source(6)	Cr1, Cr2 Cr3, Cr4, Cr5	1 pH	C0603

Cell DBC: figure 7.4(b)(7)				
Item	**Name/Alias**	**Schematic ref.**	**Part value(1)**	**Footprint**
1	Bare die *SiC* MOSFET	M1t, M2t M3t, M4t M1b, M2b M3b, M4b	CPM2-1700-0045B	CPM2-1700-0045B
2	Bare die *SiC* Diode	D1t, D2t D3t, D4t D1b, D2b D3b, D4b	CPW5-1700-Z050B	CPW5-1700-Z050B
3	C_{dc} snubber capacitors	C1d, C2d, C3d C4d, C5d, C6d C7d, C8d	0.15 μF/1 kV	C2225
4	$R_{g_{int}}$ gate resistance	RG1t, RG2t RG3t, RG4t RG1b, RG2b RG3b, RG4b	10 Ω/1 %/0.250 W	R0603
5	R_{NTC} temperature sensor	R_{NTC}	10 kΩ/1 %/70 mW	R0402
6	Square post connector(5)	J3D_J4D J5D_J6D J7D_J8D J9D_J10D J11D_J12D J13D_J14D J15D_J16D J17D_J18D	TW-10-07-L-D-300-SM	SAMTEC_2
7	Power connectors	Bus+, Bus-, U	(8)	(8)

Table notes:
(1) These values are taken as reference.
(2) TVS for automotive and traction applications: SMCJXXA.
(3) Fast *SiC* diode.
(4) Driver connection, connector 4x2 and pitch 2.54 mm (SAMTEC).
(5) Embedded PCB and DBC interconnection, pitch 2.00 mm (SAMTEC).
(6) RLC filter in order to reduce gate *SiC* MOSFETs oscillations. The components must be experimentally tuned in.
(7) Wire bondings are not included in the table.
(8) Power connectors are not included in the schematic (custom design).

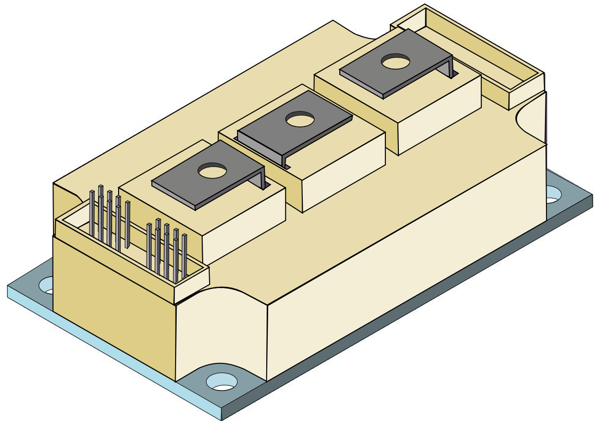


Figure 7.5: Power module mechanics based on SEMITRANS solution.

7.2.1 Power module mechanics

The mechanics of both *SiC* power modules developed in this thesis are based on the SEMITRANS standard solution. The power module mechanics is the first step of design process because it establishes the main space and placement constrains. The SEMITRANS topology is chosen as reference due to its usage in wide range of converter topologies, included half-bridges, applications (AC drives, switched reluctance and DC motors) and power ranges. They typically have 600-1700 V/25-900 A ranges, and present a high insulated copper baseplate assembled on a DBC substrate.

In addition to these reasons, this package is selected because it is a proven technology, easier of developing and implementing than other advanced packages mentioned in chapter 5. Therefore, this encapsulation is considered a valid option for *SiC* power modules, especially for prototyping.

The package of *symmetric* and *cell* half-bridges is similar to commercial solutions, but a customization has been required due to particular power connectors and auxiliary terminals used in these *SiC* half-bridge proposals. The physical dimensions are shown in the figure 7.5, where the main differences with commercial SEMITRANS modules the connector spaces.

7.2.2 Substrate stack-up: vertical hybrid configuration

As mentioned in chapter 5, inorganic substrates still are an interesting alternative to develop *SiC* power modules because they provide the sufficient thermal conductivity and their production is less complicated than other advanced substrate designs.

As a result, the power layout of both the *SiC* power alternatives are implemented over a DBC, using wirebonding interconnection technology[1]. The traditional solution of inorganic substrates consists of implementing gate attack and power layout tracks on the same surface. In this solution, the routing process is more complicated due to loss of space for power signals and increase EMI effects in control signals.

In order to avoid these problems of standard inorganic solutions, two substrate technologies are connected. This hybrid solution consists of a PCB and a DBC whose full substrate is shown in the figure 7.6[2]:

- ❒ PCB substrate: the substrate circuits consist of control signals between the driver and power semiconductors. The gate-source connection of each transistor (*SiC* MOSFETs) is critical, so gate active clamping circuits are implemented in order to avoid breakdown problems. Moreover, some filters are also added which seek to reduce gate signal oscillations. Additionally, other clamping protections are implemented to limit the transistor drain-source voltage drop. The particularities of each half-bridge solution are the following:
  - *Symmetric* embedded PCB (figure 7.7(a)): gate protection circuits only present one configuration, one protection circuit for a couple of *SiC* MOSFETs.
  - *Cell* embedded PCB (figure 7.8(a)): gate protection circuits presents three options, two of them in order to protect a couple of *SiC* MOSFETs and the other only for one MOSFET.
- ❒ DBC substrate: the circuits consist of four *SiC* MOSFETs with four external *SiC* diodes in parallel per level (top and bottom). The usage of external *SiC* diodes avoids worse characteristics of MOSFET body diodes. Each transistor has its own gate resistance to control turn *on/off* process and there are snubber capacitors[3] between DC bus tracks to reduce their stray impedance values. The interconnection between both substrates is done through gate interfaces (vertical pins, differential signals), in particular:

[1]The wirebonds are not implemented and simulated in designs due to their specific characteristics and configurations that are only provided by the power module assembly company.

[2]This substrate is used in electrical simulations without solder layers in order to simplify models, reducing their computational load. In the thermal behaviour, DBC solder/sinterization layers are taken into account.

[3]The number of capacitors depend on the design: the *symmetric* design only has 3 capacitors between Bus+ and Bus-, whereas, the *cell* design implements 8 capacitors between DC bus tracks.

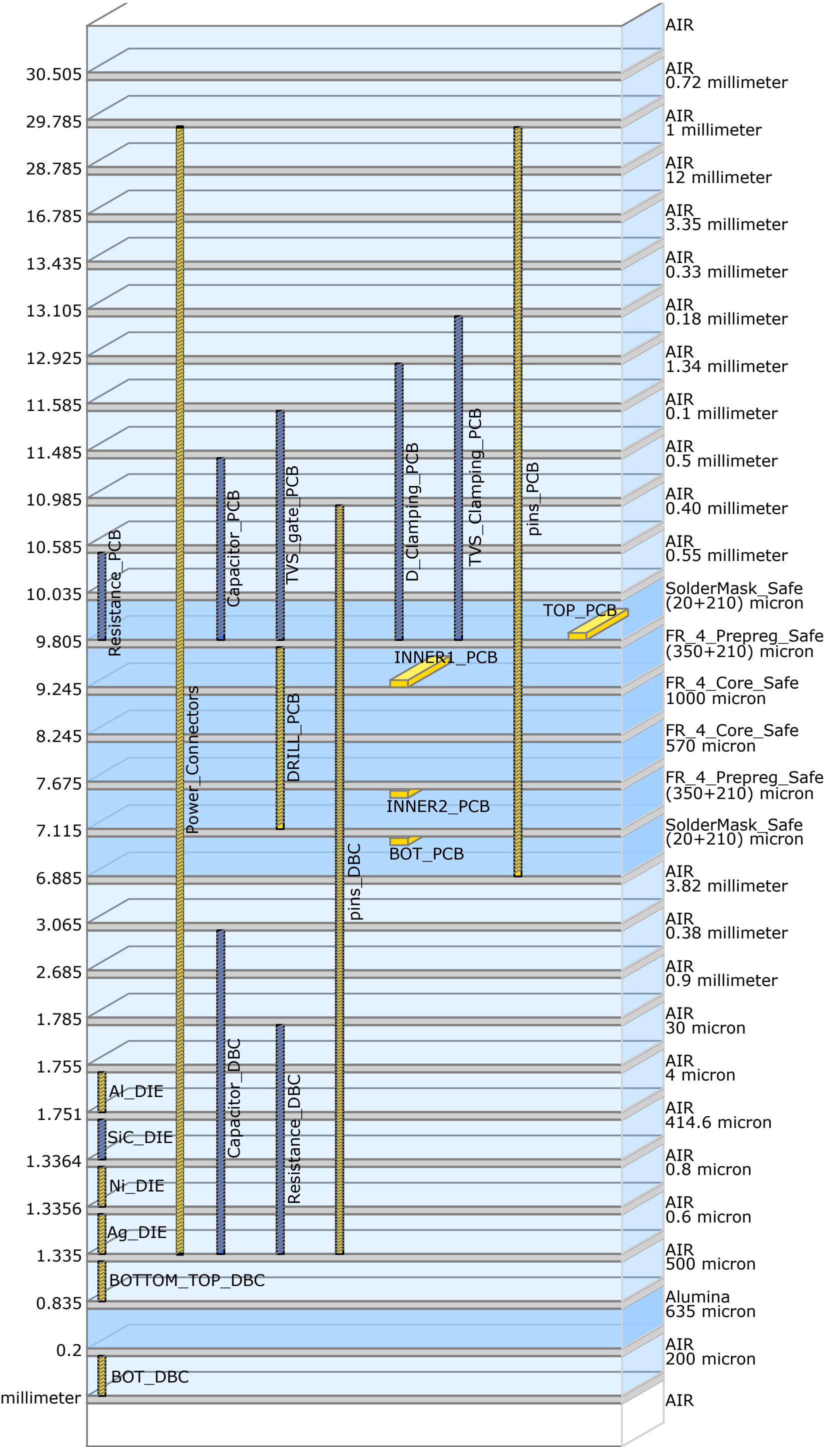


Figure 7.6: Power module ADS^{TM} simulation stack-up.

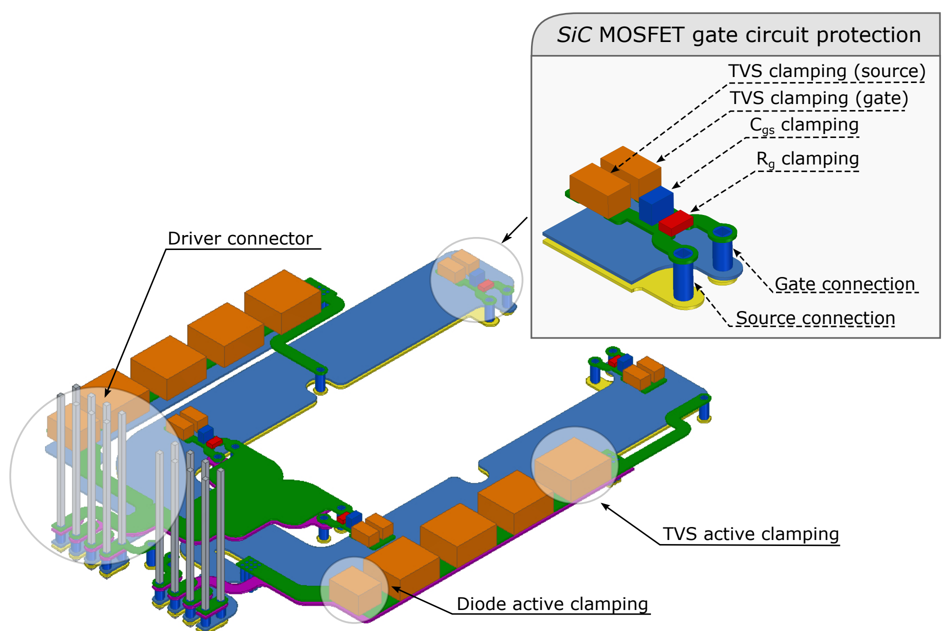
- *Symmetric* DBC (figure 7.7(b)): it presents the same configuration for gate interfaces which connect control signals of embedded PCB (figure 7.7(a)) with gate-source (auxiliary source) of each *SiC* MOSFET in the power layout.
- *Cell* DBC (figure 7.8(b)): it presents three gate interface options to connect the embedded PCB (figure 7.8(a)) with the DBC.

7.2.3 Gate attack: embedded PCBs

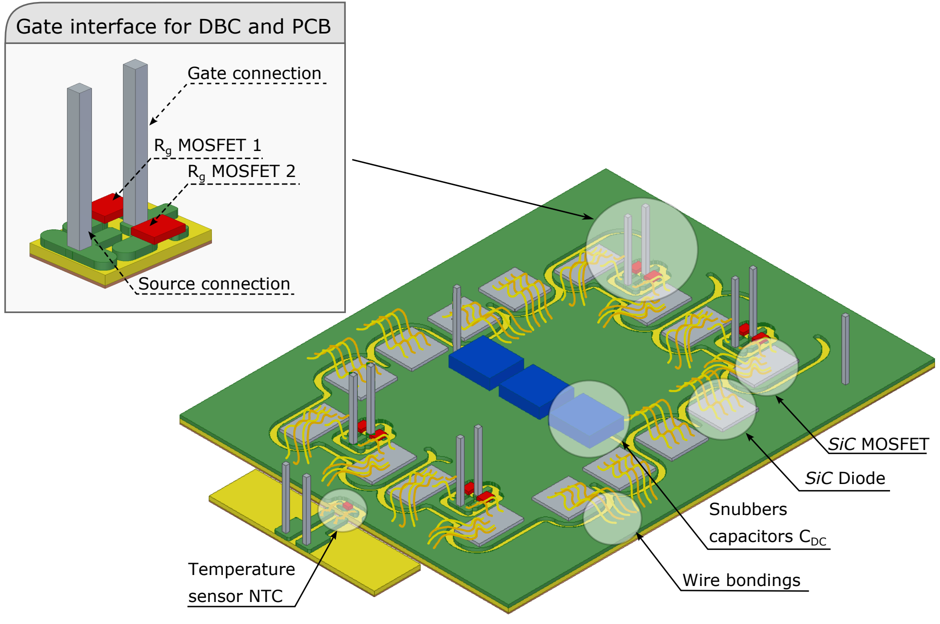
The solution of routing gate control signals through an embedded PCB is adopted, according to established design criteria (chapter 5). This solution connects gate control loops vertically with gate-source contacts of *SiC* MOSFETs through gate interfaces between PCB and DBC substrates (vertical pins). In the routing process of embedded PCB for *symmetric* and *cell* solution (figures 7.9 and 7.10, respectively), the following concepts have been taken into account:

1. The power loop and the control loop are independent. The embedded PCBs link control signals vertically with semiconductor dies (gate and source contacts), establishing a Kelvin connection which provides an auxiliary source contact isolated from the power layout (figures 7.9-① and 7.10-①).
2. The control signals are differential. They consist of a gate and a source track, each one routed through a PCB layer in order to provide enough electrical isolation and improve the coupling effect between these differential tracks (figures 7.9-② and 7.10-②). The multilayer PCB structure favours the coupling between gate loops, thus reducing parasitic values (L_{gate}).
3. Each pair of paralleled MOSFET has its own gate control loop[1]. The tracks of each gate loop are as equal and symmetric as possible (figures 7.9-③ and 7.10-③). Thus, parasitic inductances are practically identical, which produces a symmetric negative feedback effect in gate control connections. The best feedback effect for control signals studied in chapter 5.
4. The usage of wide copper areas and round edges help minimize parasitic impedance, improve the circuit symmetry and flow homogeneous control signals (figures 7.9-④ and 7.10-④)
5. The protection circuits and other components (gate filters to reduce oscillations) are embedded into the PCB without reducing power layout surface (figures 7.9-⑤ and 7.10-⑤).

[1]The transistors are connected in pairs in order to favour symmetry and equal current distribution. In the case of the *cell* module, two bottom transistors have an individual connection.



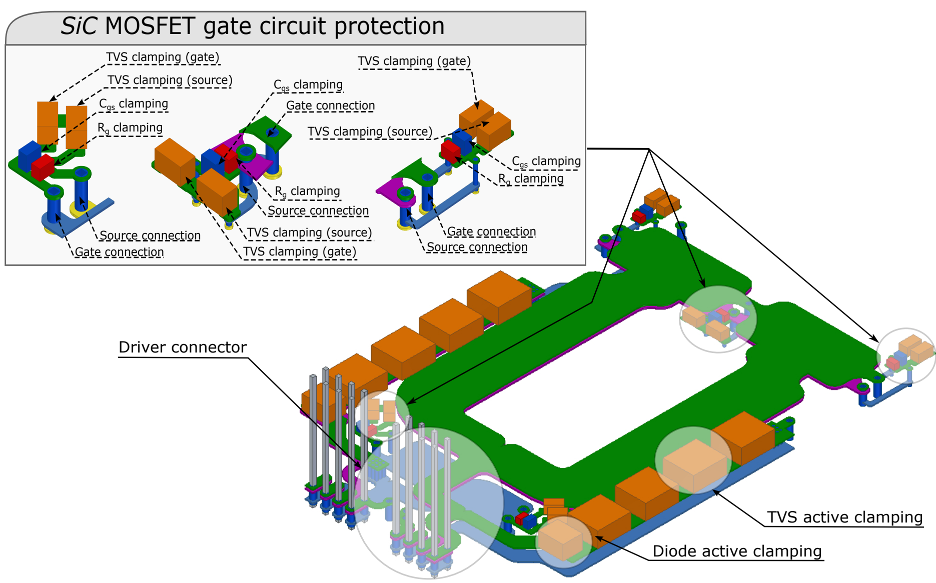
(a) Details of the *symmetric* embedded PCB.



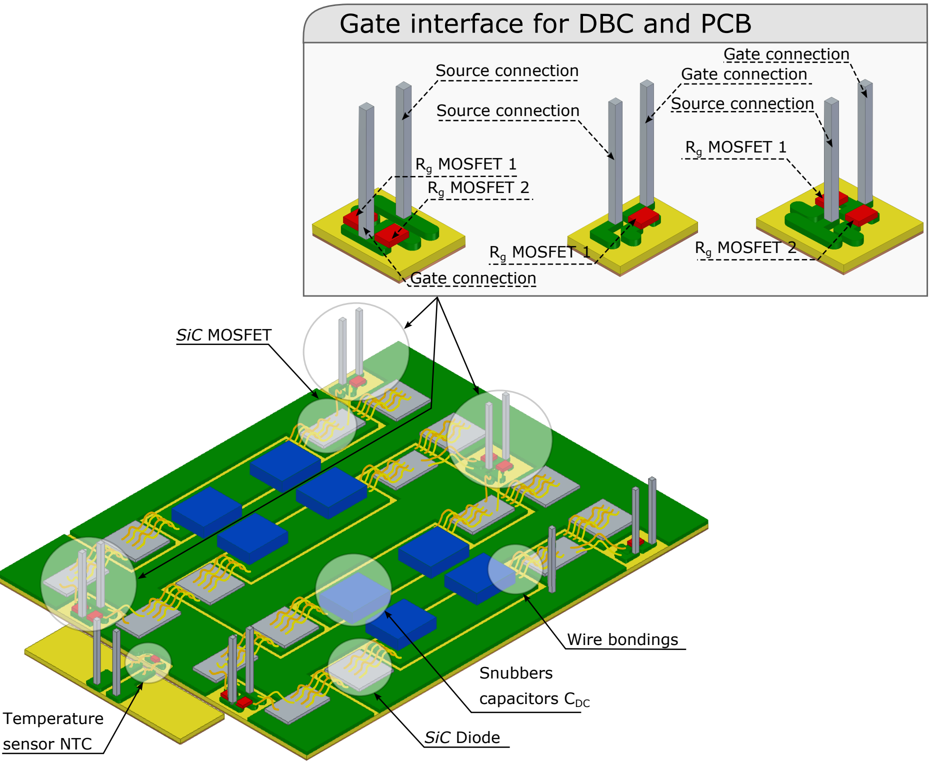
(b) Details of the *symmetric* DBC.

(*) Power connectors are excluded in order to improve the visibility of other design details.

Figure 7.7: Details of PCB and DBC for the *symmetric* power module design.



(a) Details of the *cell* embedded PCB.



(b) Details of the *cell* DBC.

(*) Power connectors are excluded in order to improve the visibility of other design details.

Figure 7.8: Details of PCB and DBC in the *cell* power module design

Applying these gate design criteria produces the symmetry of control loops whose equivalent circuit for top and bottom *SiC* MOSFETs are shown in the figures 7.11 and 7.12:

❒ *Symmetric* embedded PCB: the equivalent circuit[1] for top connections (figure 7.11(a)) describes a symmetric negative feedback effect, where parasitic elements of gate PCB signals (figure 7.11(a)-$\boxed{\text{A}}$) and gate interfaces (connections between PCB and DBC, figures 7.11(a)-$\boxed{\text{B}}$ and 7.11(a)-$\boxed{\text{C}}$) can be expressed as (7.1):

$$\begin{aligned} &\boxed{\text{A}}\ L_{Gt1} + L_{St1} \simeq L_{Gt2} + L_{St2};\\ &\boxed{\text{B}}\ L_{Gt1_1} + L_{St1_1} \simeq L_{Gt1_2} + L_{St1_2};\\ &\boxed{\text{C}}\ L_{Gt2_1} + L_{St2_1} \simeq L_{Gt2_2} + L_{St2_2}. \end{aligned} \tag{7.1}$$

Bottom PCB gate signals (figure 7.11(b)-$\boxed{\text{A}}$) and bottom gate interface connections (figures 7.11(b)-$\boxed{\text{B}}$ and 7.11(b)-$\boxed{\text{C}}$) behave equally, as the relations of (7.2) show:

$$\begin{aligned} &\boxed{\text{A}}\ L_{Gb1} + L_{Sb1} \simeq L_{Gb2} + L_{Sb2};\\ &\boxed{\text{B}}\ L_{Gb1_1} + L_{Sb1_1} \simeq L_{Gb1_2} + L_{Sb1_2};\\ &\boxed{\text{C}}\ L_{Gb2_1} + L_{Sb2_1} \simeq L_{Gb2_2} + L_{Sb2_2}. \end{aligned} \tag{7.2}$$

These expressions can be verified through the equivalent inductance and resistance values for the *symmetric* embedded PCB (figures 7.13(a) and 7.13(b)), where PCB top connections are identical between them. The same applies to the bottom connections. Additionally, there is only a difference of 1 nH and 1 mΩ between top and bottom PCB tracks.

The impedance values for gate interface connections are shown in the figures 7.13(c) and 7.13(d)). According to these results and the usage of the same structure for top and bottom gate interfaces, they can be simplified as the same circuit (7.3):

$$\begin{aligned} L_{Gt1_1} + L_{St1_1} &\simeq L_{Gt1_2} + L_{St1_2} \simeq\\ \simeq L_{Gt2_1} + L_{St2_1} &\simeq L_{Gt2_2} + L_{St2_2} \simeq\\ \simeq L_{Gb1_1} + L_{Sb1_1} &\simeq L_{Gb1_2} + L_{Sb1_2} \simeq\\ \simeq L_{Gb2_1} + L_{Sb2_1} &\simeq L_{Gb2_2} + L_{Sb2_2}. \end{aligned} \tag{7.3}$$

[1]The equivalent circuit only represents the inductive part of parasitic impedance.

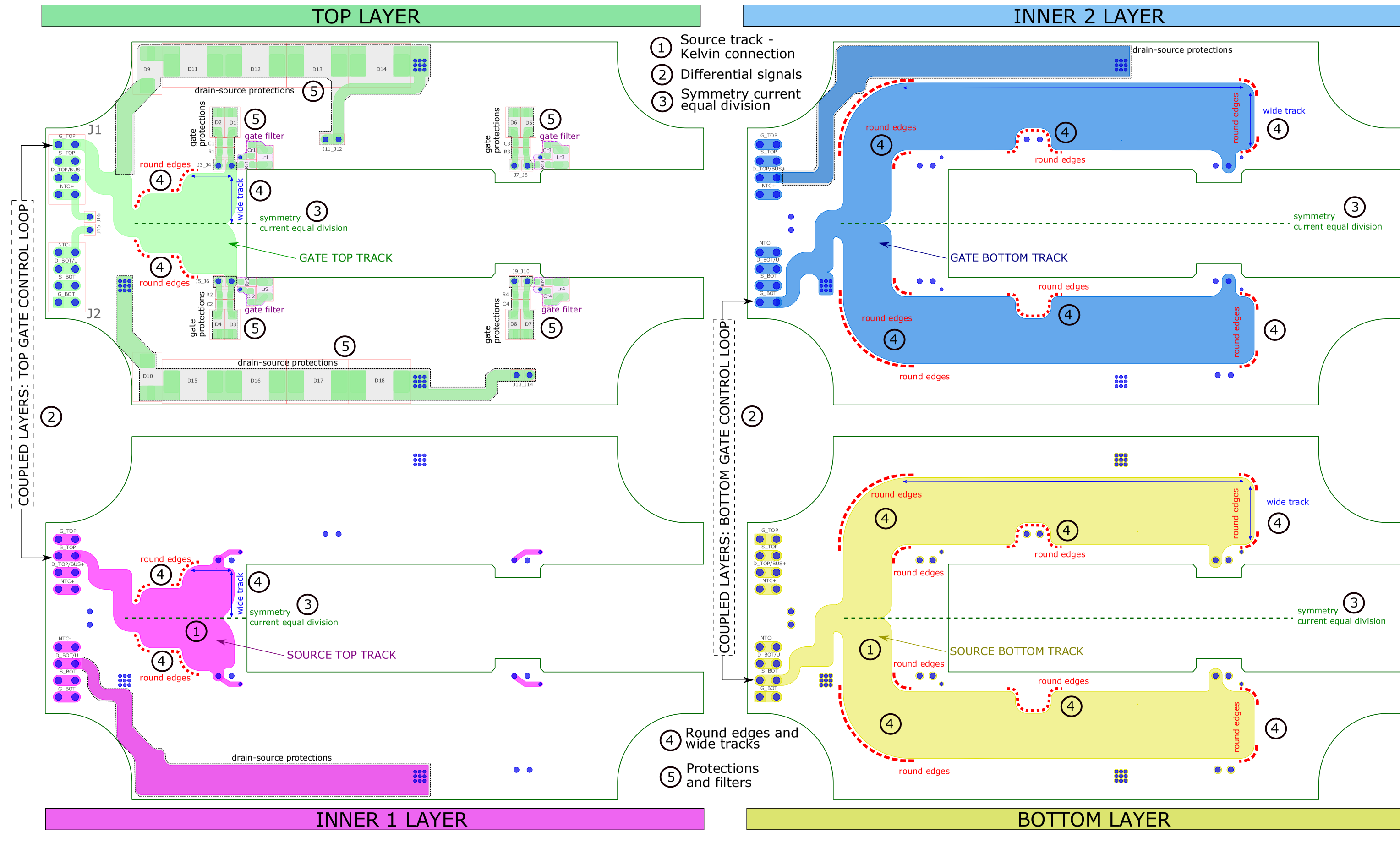


Figure 7.9: Gate attack PCB layer of the *symmetric* design.

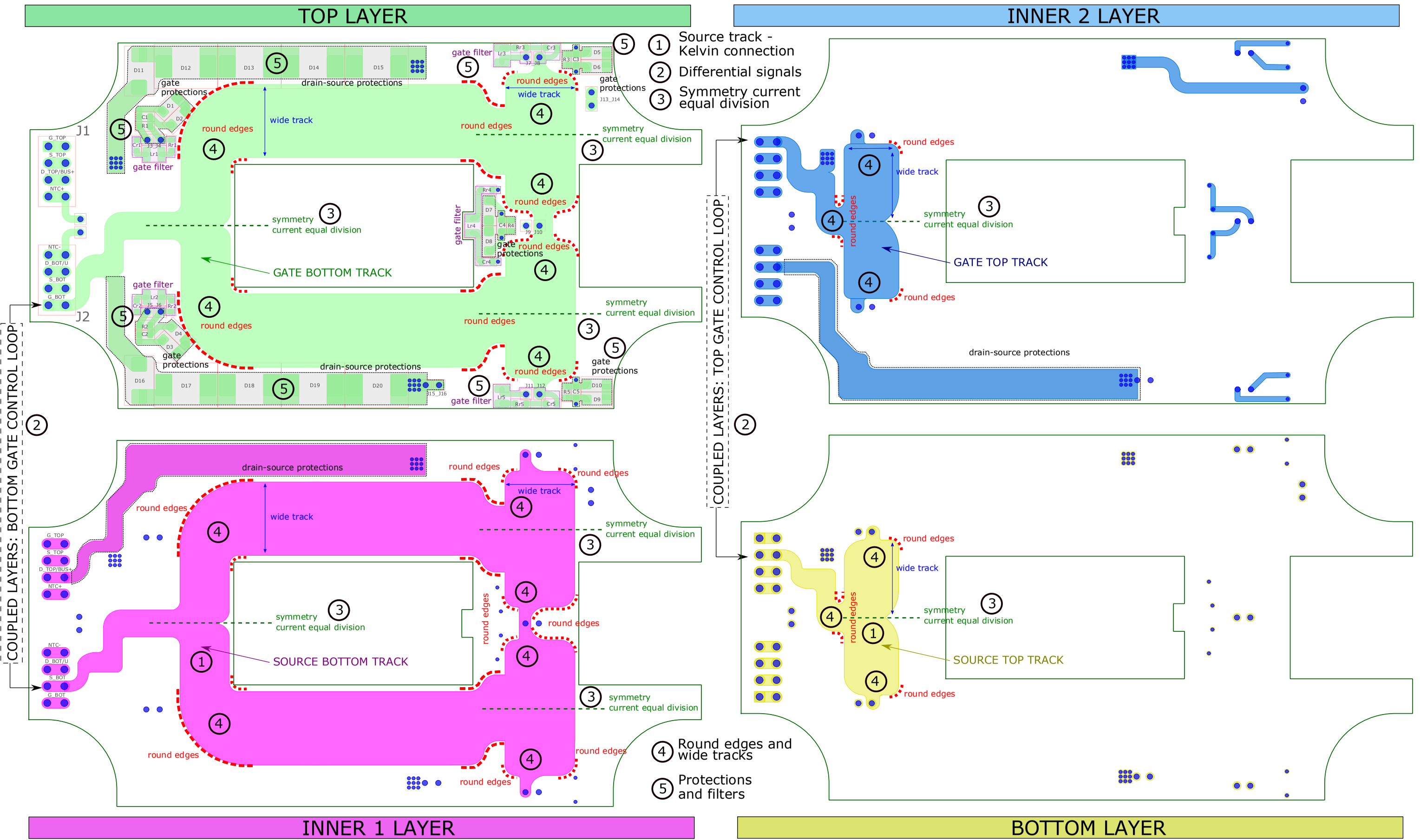


Figure 7.10: Gate attack PCB layer of the *cell* design.

- *Cell* embedded PCB: the equivalent circuit for top connections (figure 7.12(a)) also describes a symmetric negative feedback effect, where parasitic elements of gate PCB signals (figure 7.12(a)-$\boxed{\text{A}}$) and gate interfaces (figures 7.12(a)-$\boxed{\text{B}}$ and 7.12(a)-$\boxed{\text{C}}$) fullfill the same relation as the *symmetric* embedded PCB (7.1).

  However, bottom PCB gate signals (figure 7.12(b)-$\boxed{\text{A}}$) and gate interface connections (figures 7.12(b)-$\boxed{\text{B}}$, 7.12(b)-$\boxed{\text{C}}$ and 7.12(b)-$\boxed{\text{D}}$) show a different relation (7.4):

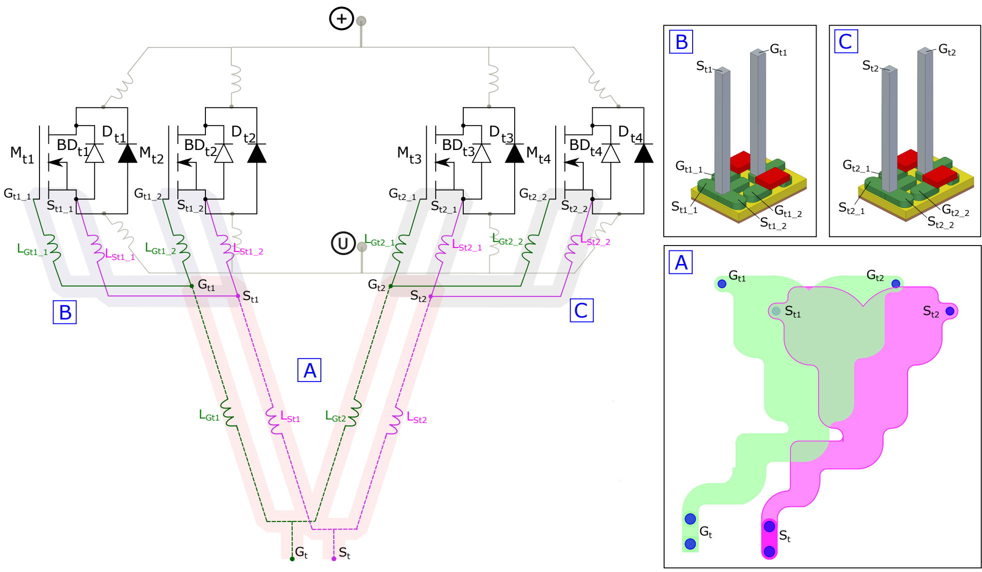
$$
\begin{aligned}
&\boxed{\text{A}}\; L_{Gb1} + L_{Sb1} \simeq L_{Gb2} + L_{Sb2};\\
&\boxed{\text{B}}\; L_{Gb1_1} + L_{Sb1_1};\\
&\boxed{\text{C}}\; L_{Gb2_1} + L_{Sb2_1} \simeq L_{Gb2_2} + L_{Sb2_2};\\
&\boxed{\text{D}}\; L_{Gb3_1} + L_{Sb3_1}.
\end{aligned}
\tag{7.4}
$$

  The equivalent inductances and resistances for the *cell* embedded PCB are shown in the figures 7.13(e) and 7.13(f), respectively. The top connections of the PCB are practically identical. Nevertheless, bottom connections are not equal, since the maximum difference is 1 nH and 0.5 mΩ between M1b-M4b and M2b-M3b connections. Moreover, the maximum difference between top and bottom tracks is 4.5 nH and 2 mΩ.

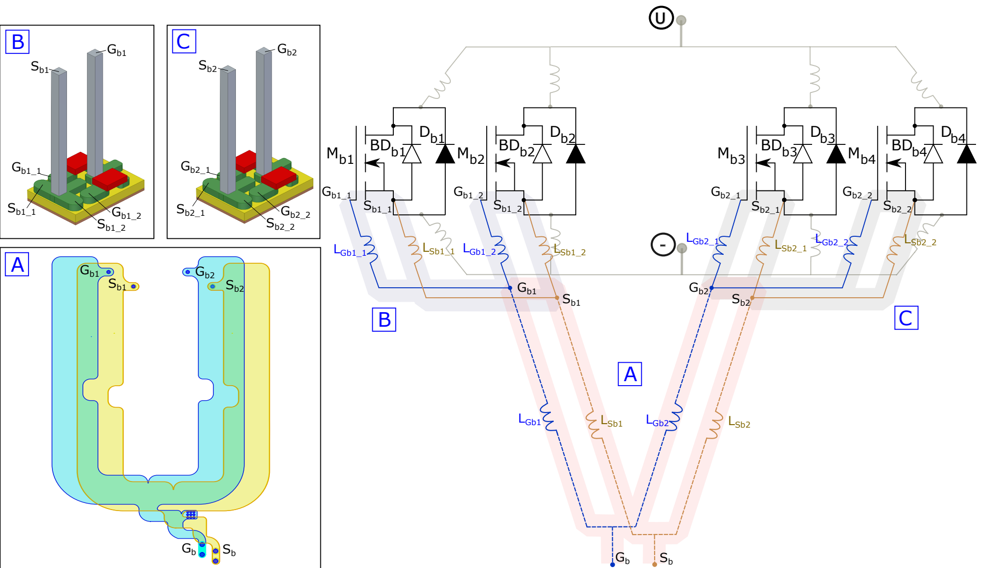
  In the case of gate interface connections, the three circuit options exhibit different inductance and resistance values, as the figures 7.13(g) and 7.13(h) show. Their maximum inductance difference is 0.2 nH, whereas the equivalent resistances are practically identical. Thus, gate interface circuits in the *cell* design can be simplified as in the case of the *symmetric* design (7.3).

These analyses, where the equivalent parasitic impedances of gate control loops for the *symmetric* and *cell* designs have been extracted through the expressions (7.1)-(7.4), conclude that top and bottom connections of each design are symmetrical, with the exception of cell bottom connection (a maximum difference of 1 nH and 0.5 mΩ), but it can be neglected. The figures 7.14(a) and 7.14(e) display the control voltage of each *SiC* MOSFET in the *symmetric* design, where no gate voltage difference is detected in circuit simulation. The same behaviour is observed from gate voltage signals in the *cell* design (figures 7.14(b) and 7.14(f)), where bottom impedance gate loops differences do not produce critical voltage drops.

In addition to the gate voltage analysed, the gate current is obtained for top and bottom MOSFET of the *symmetric* (figures 7.14(c) and 7.14(g)) and *cell*

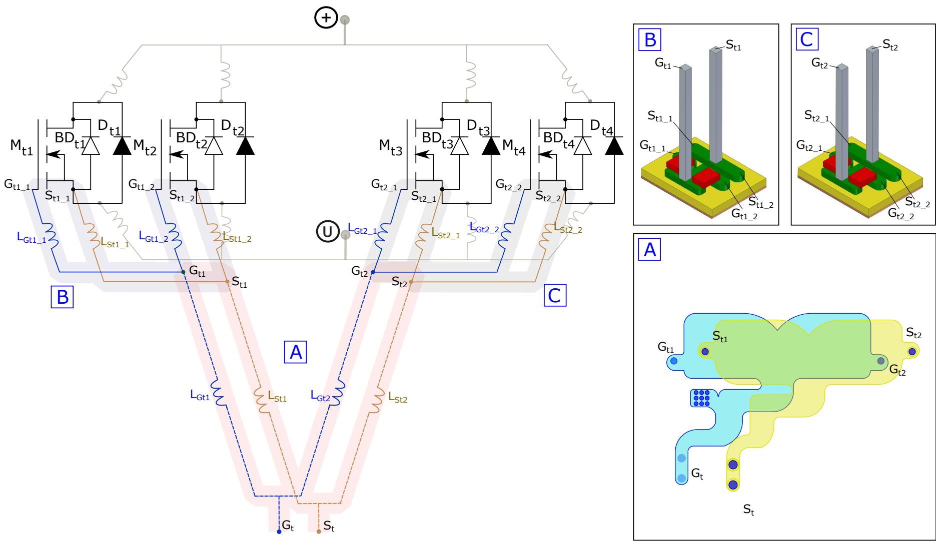


(a) Top *SiC* MOSFETs connection.

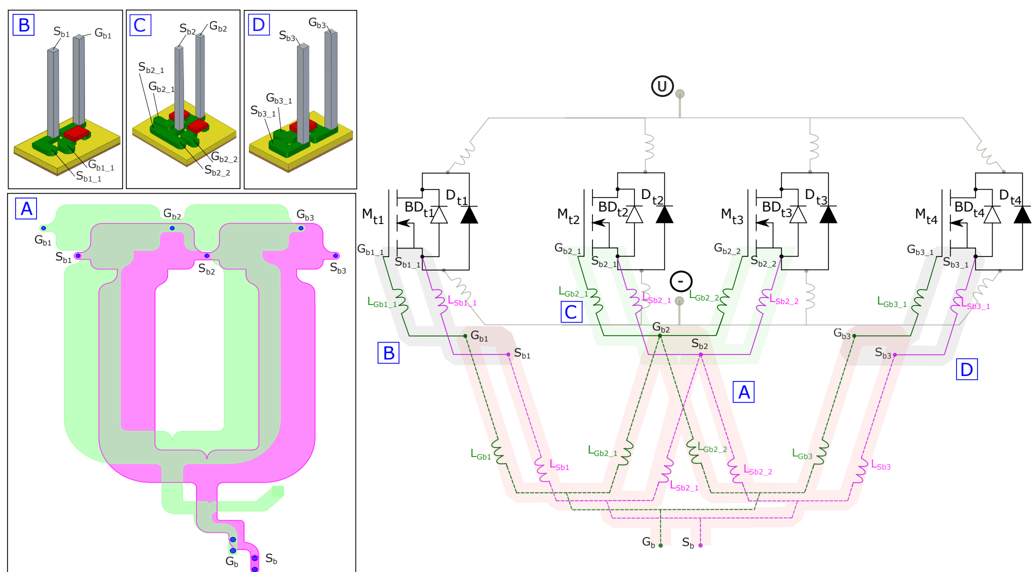


(b) Bottom *SiC* MOSFETs connection.

Figure 7.11: Gate attack circuit of the *symmetric* design.

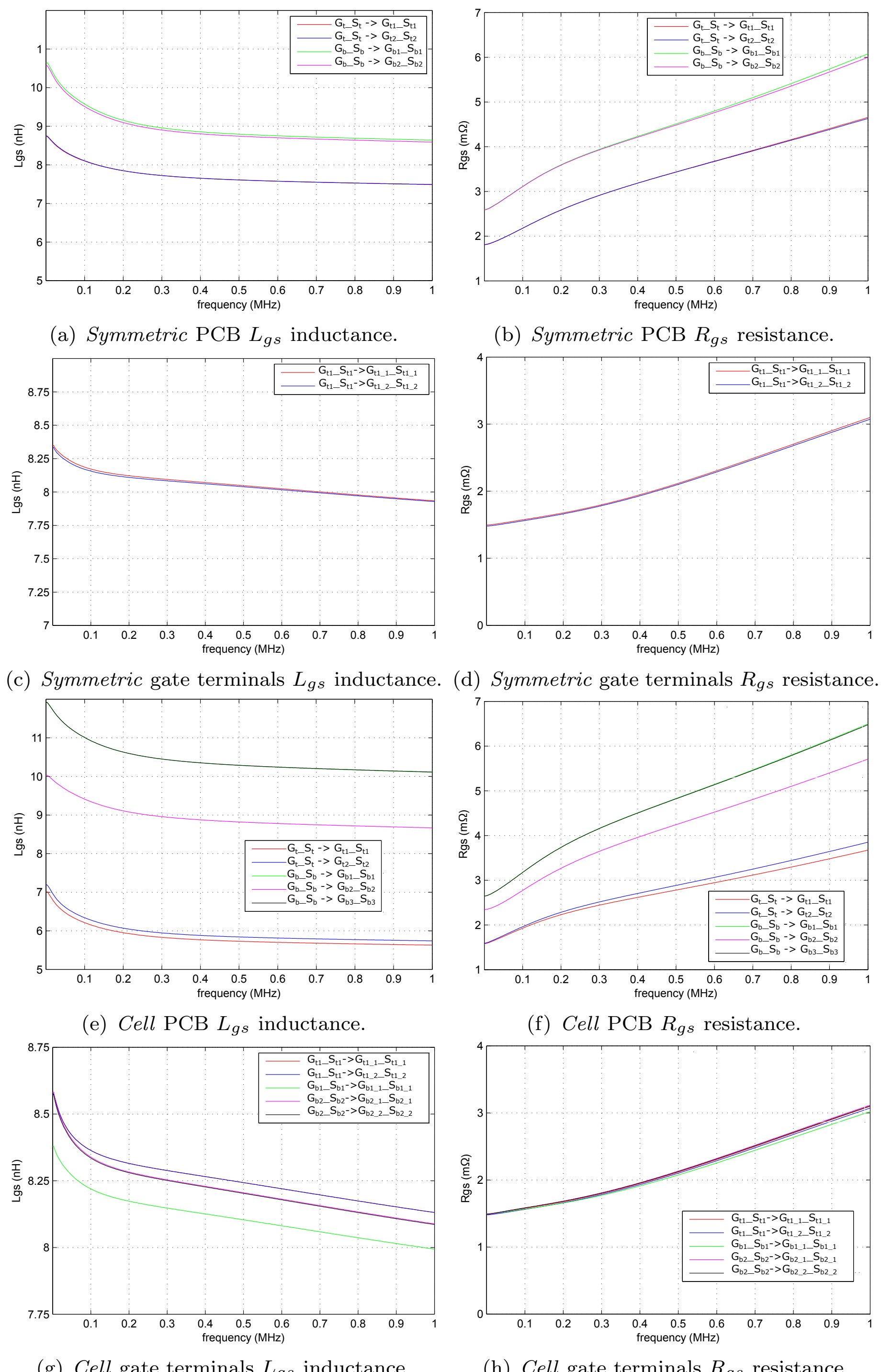


(a) Top *SiC* MOSFETs connection.



(b) Bottom *SiC* MOSFETs connection.

Figure 7.12: Gate attack circuit of the *cell* design.



(a) *Symmetric* PCB L_{gs} inductance.

(b) *Symmetric* PCB R_{gs} resistance.

(c) *Symmetric* gate terminals L_{gs} inductance.

(d) *Symmetric* gate terminals R_{gs} resistance.

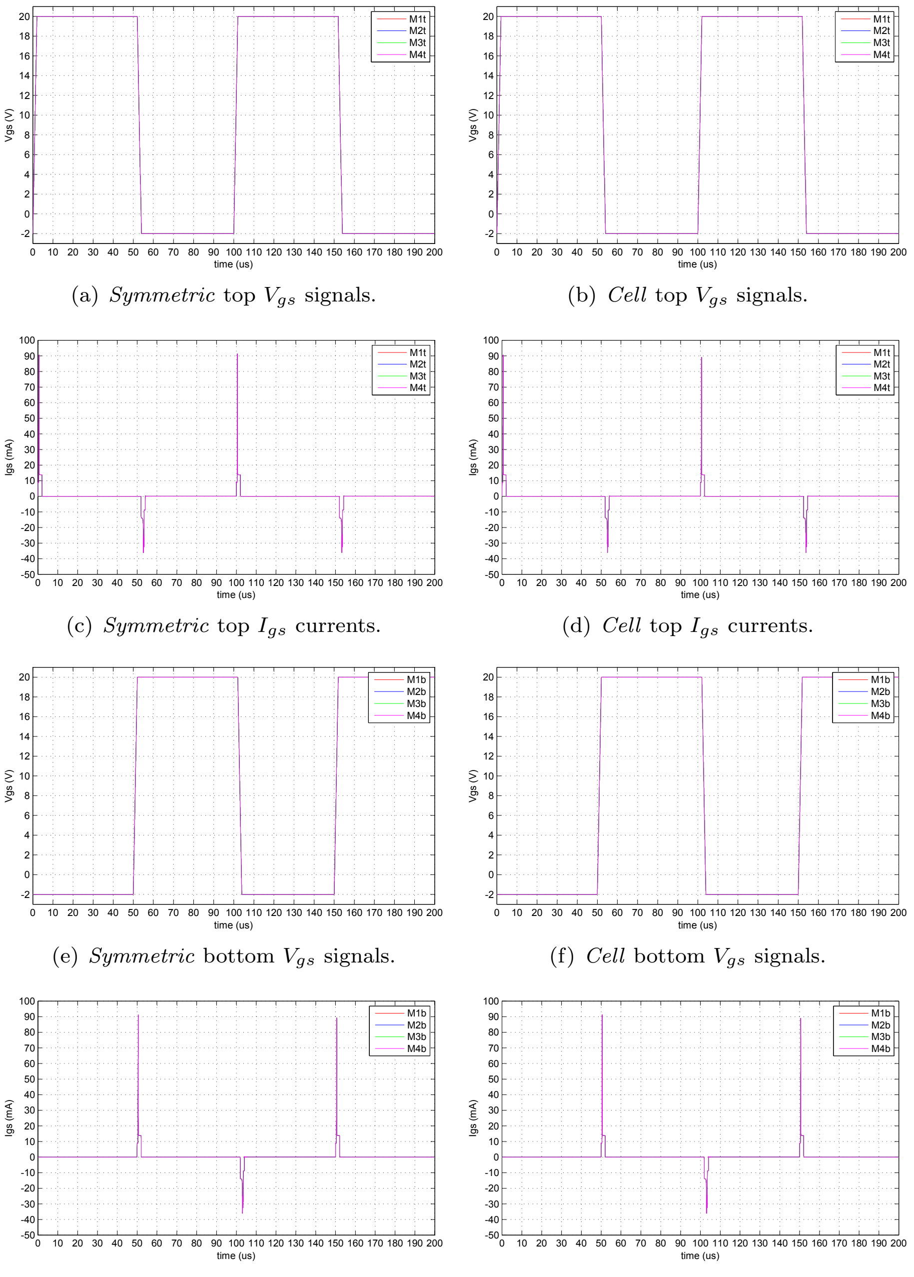
(e) *Cell* PCB L_{gs} inductance.

(f) *Cell* PCB R_{gs} resistance.

(g) *Cell* gate terminals L_{gs} inductance.

(h) *Cell* gate terminals R_{gs} resistance.

Figure 7.13: Gate attack impedances for *symmetric* and cell *designs*.



(a) *Symmetric* top V_{gs} signals.

(b) *Cell* top V_{gs} signals.

(c) *Symmetric* top I_{gs} currents.

(d) *Cell* top I_{gs} currents.

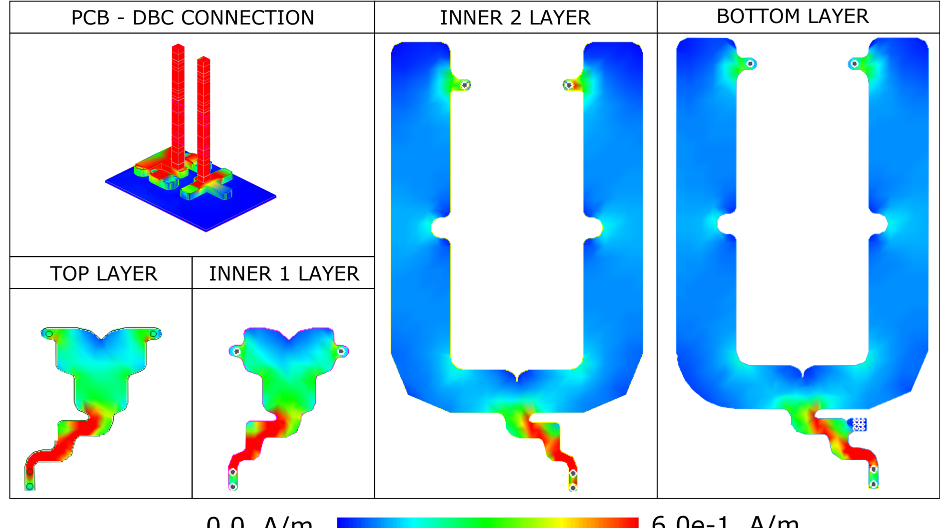
(e) *Symmetric* bottom V_{gs} signals.

(f) *Cell* bottom V_{gs} signals.

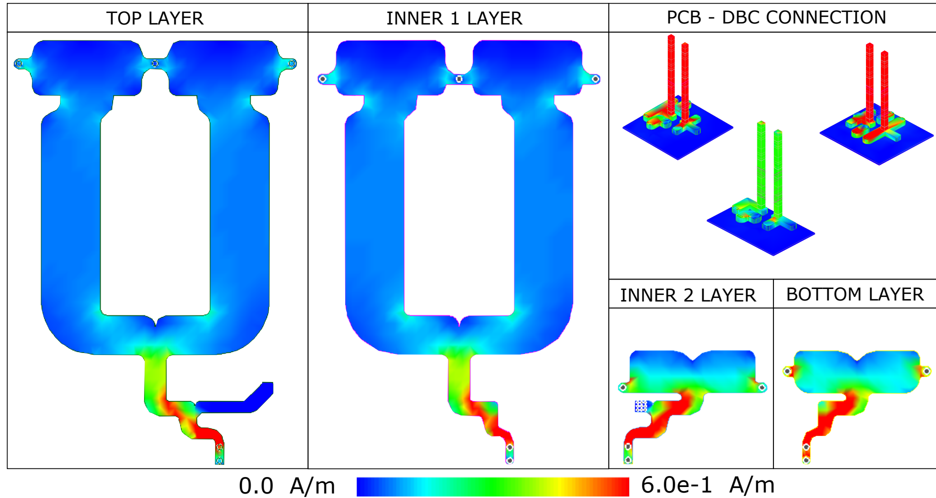
(g) *Symmetric* bottom I_{gs} currents.

(h) *Cell* bottom I_{gs} currents.

Figure 7.14: Gate attack voltage and current signals for *symmetric* and *cell* designs.



(a) *SiC* MOSFET connections of *symmetric* design.



(b) *SiC* MOSFET connections of *cell* design.

Figure 7.15: Gate attack current density distribution.

designs (figures 7.14(d) and 7.14(h)). As a result, the circuit impedance variations between parallelized MOSFETs are minimum, so the simulation results do not offer differences in gate control loops which produce turn *on*/*off* delays.

Finally, the current density distribution for 10 kHz[1] frequency is obtained. The results of figures 7.15(a) and 7.15(b) for the *symmetric* and *cell* designs, respectively, show a homogeneous current density distribution between top and bottom connections due to the symmetry and soft/round edge technique application.

7.2.4 Power layout: Direct Bonding Copper (DBC)

The vertical stack-up configuration, where gate control signals are routed through embedded PCBs, allows to use the DBC substrate for power signals except gate interfaces (vertical pins). In this regard, the following concepts have been taken into account:

1. In these half-bridge proposals, each circuit level (power switch) consists of 4 parallelized *SiC* MOSFETs. According to the proposed design criteria, having less power semiconductors eases the routing process, because the number of interconnections are reduced and there is more space to balance circuit tracks. Thus, the complete power half-bridge circuit could be developed with a total of 8 *SiC* MOSFETs, since they could use their internal body diodes to allow the current to flow backwards. However, using external *SiC* JBS diodes instead of body diodes improves the circuit efficiency. For this reason, the power layout consists of 8 *SiC* MOSFETs and also 8 *SiC* JBS diodes, as figures 7.16(a) and 7.16(b) show.

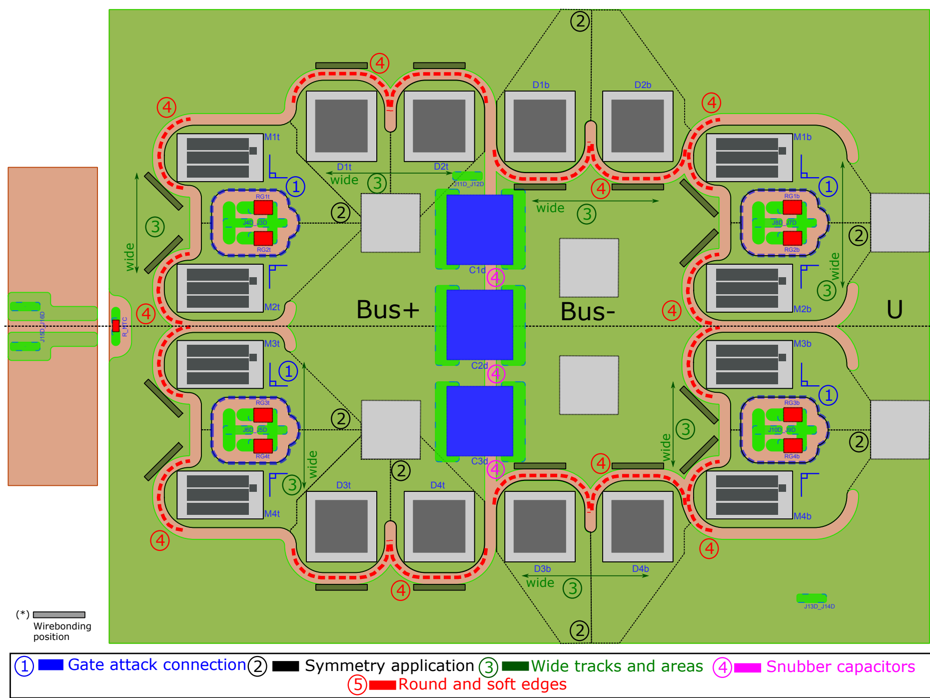
2. The position and orientation of semiconductor dies try to cancel out electromagnetic fields, especially between power and control signals (gate interface areas), where a perpendicular direction between signals is established (figures 7.16(a)-① and 7.16(b)-① for the *symmetric* and *cell* DBC, respectively)[2]. Moreover, a correct distribution of power layout components helps to reduce the number of interconnections, i.e. the number of wirebondings[3].

3. The electrical connections between parallel power loops, P-Cell (top MOSFET with bottom diode) and N-Cell (bottom MOSFET with top diode),

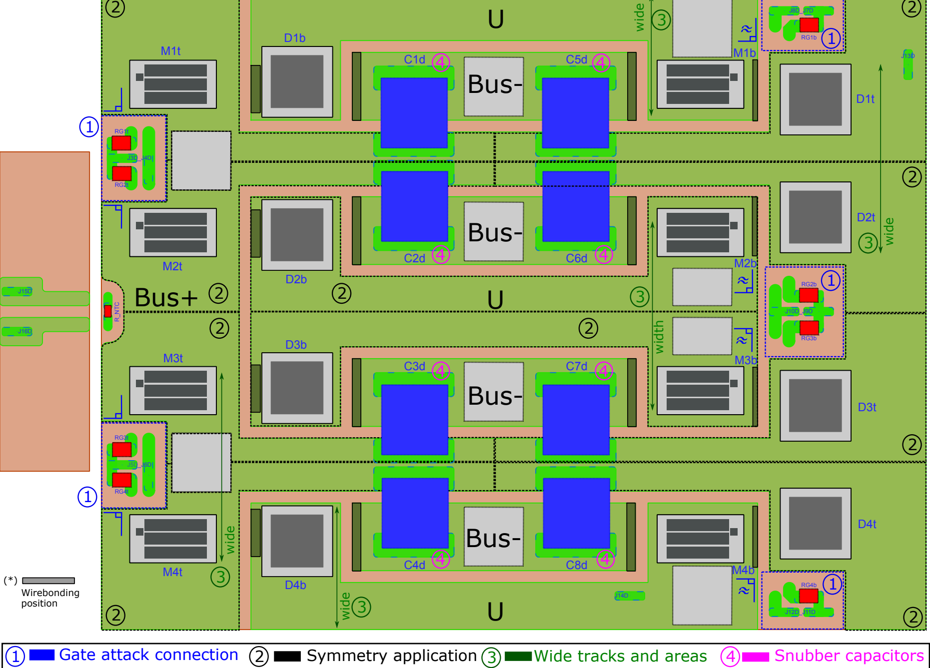
[1]This frequency reduces ADS^{TM} co-simulation convergence issues and computational load, due to the power semiconductor electrical model provided by manufacturer. The current switching frequencies of *SiC* devices are higher (30-50 kHz), but they lie in the same range.

[2]The *cell* design presents an exception in the bottom MOSFET connections, which are not totally perpendicular.

[3]The results extracted from simulations do not take into account these elements because their characteristics are part of the manufacturer's assembly technology.



(a) Details of the *symmetric* DBC.



(b) Details of the *cell* DBC.

(*) Power connectors are excluded in order to improve the visibility of other design details.

Figure 7.16: Details of each power layout proposal (*symmetric* and *cell* DBCs).

are as equal as possible through the symmetry applied in the layout, as figures 7.16(a)-② and 7.16(b)-② indicate. For this aim, an equal distribution of semiconductor dies (two-dimensional symmetry) through power terminal pads yields similar copper areas with similar stray impedances.

4. The copper areas and tracks try to be as wide and short as possible in the current flow direction (figures 7.16(a)-③ and 7.16(b)-③). In both the half-bridge proposals the electrically longer connections are focused on phase/output circuit tracks. The cell concept connection of MOSFETs and external diodes produce the parasitic inductance increment of output circuit, the point where the load is connected (figures 7.16(a) and 7.16(b)).

5. Radio frequency know-how is applied in order to reduce and balance power loops through round tracks (figure 7.16(a)-⑤), special cuts (specific forms in clearance areas) and the insertion of passive components as snubber capacitors (figures 7.16(a)-④ and 7.16(b)-④).

The application of these power layout design criteria produce the following results on the stray impedances and currents of each half-bridge solution:

- *Symmetric* DBC: the 4 power loops or switching cells, which form the half-bridge circuit, present average parasitic inductance and resistance values of 3 nH and 1 mΩ, as the figures 7.17(a) and 7.17(d) show. Moreover, the *SiC* MOSFETs parallelization between drain-source contacts are practically identical (figure 7.17(b) and 7.17(e)), because the power layout has an equal position, orientation and track connection of these devices. The *SiC* diodes are not located as symmetrically as MOSFETs along the current propagation direction (mechanical constrains), thus producing little impedance variations between *SiC* diodes (figures 7.17(c) and 7.17(f)) which are not relevant. These maximum average varitions are 1 nH and 1 mΩ.

  According to the stray impedance results between *symmetric* half-bridge power semiconductors, the power layout shows a symmetrical distribution where electrical connections of the parallelized devices are practically equal. For these reasons, the simulation of current behaviour through P-Cell (figures 7.19(a) and 7.19(b)) and N-cell (figures 7.19(c) and 7.19(d)) devices are practically equal.

- *Cell* DBC: these half-bridge power loops present an average parasitic inductance and resistance of 1.3 nH and 0.5 mΩ, as the figures 7.18(a) and 7.18(d) show. These values are lower than the *symmetric* case. However, the *SiC* MOSFETs parallelization shows some variations (figure 7.18(b) and 7.18(e)), because the layout tracks do not have the same dimensions. In the *SiC* diode case, a similar effect in impedance variation is produced

(figures 7.18(c) and 7.18(f)). In both semiconductors, these variations are negligible due to a maximum variation of 2 nH and 1 mΩ.

Although *SiC* MOSFETs and diodes are not located as symmetrically as in the *symmetric* case, the power layout does not show remarkable current imbalances. The current signals of P-Cell (figures 7.19(a) and 7.19(b)) and N-cell (figures 7.19(c) and 7.19(d)) switching loops are equal.

Hence, the *symmetric* design presents a better parallelization because differences between devices are smaller than in the *cell* design. Nevertheless, the *cell* design presents lower absolute parasitic impedance values than the *symmetric* design (approximately 2 nH and 1 mΩ). In both cases, the impedance variations and values do not cause current imbalances.

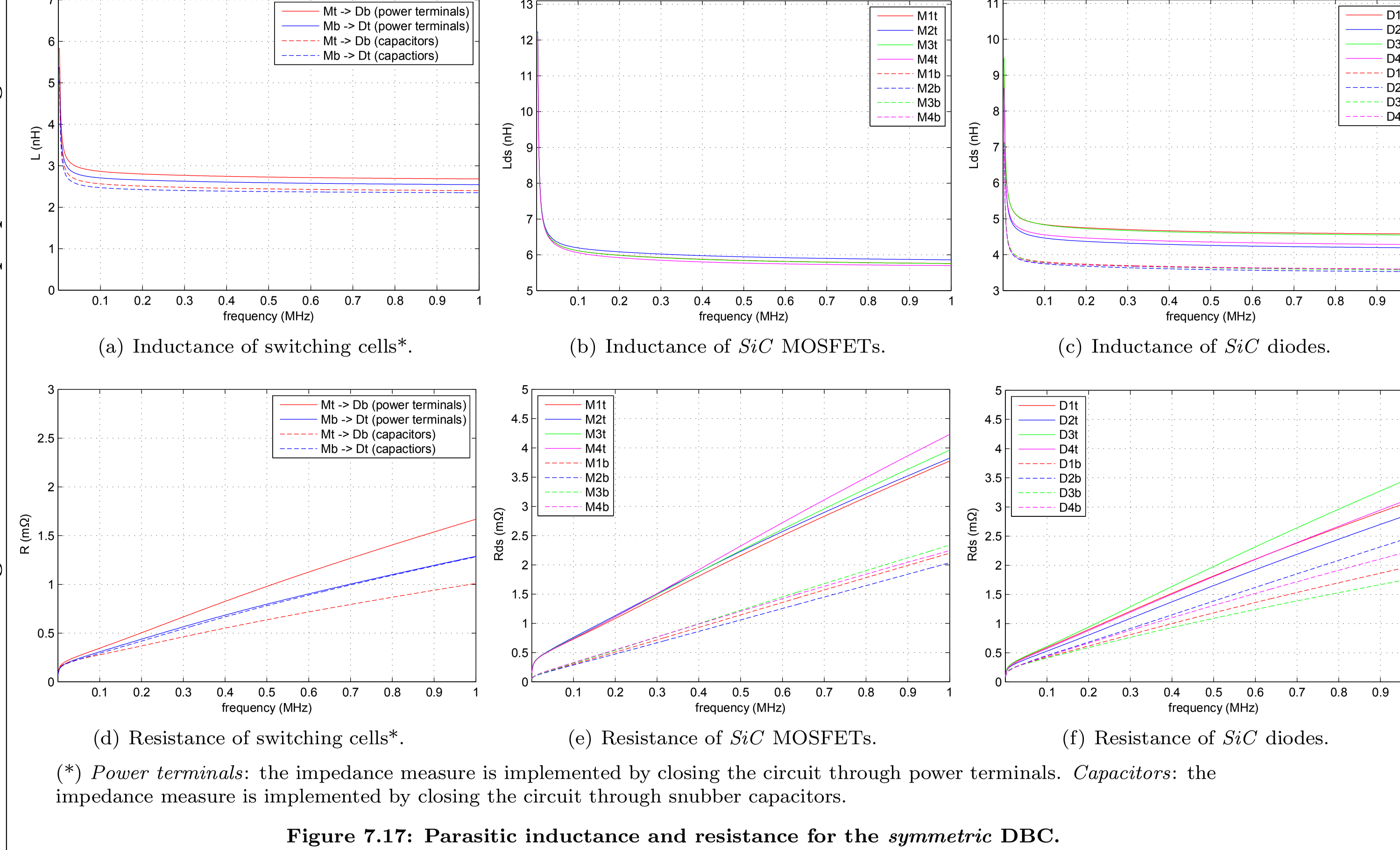
Finally, the current density distribution analysis (at 10 kHz) is the last point to evaluate the power layout of each half-bridge proposal. The results of switching cells for the *symmetric* and *cell* designs are shown in the figure 7.20(a) and 7.20(b), respectively. Both designs present an homogeneous current distribution, but the *symmetric* DBC presents a lower current density concentration due to the application of soft edge technique and a better semiconductor placement.

7.2.5 Terminals: DC bus and phase/output connectors

There are two kind of terminals in these designs: the auxiliary terminals, which are part of gate interfaces analysed in gate attack (section 7.2.3), and the power terminals proposed for each one of half-bridges. This section is focused on the three power terminals developed for the *symmetric* and *cell* solutions, where the following design criteria are met:

1. The quantity of terminals is minimized, in order to avoid the increment of power module stray impedances. Thus, there are only three terminals for each of *symmetric* and *cell* connections: positive DC bus, negative DC bus and phase (output) terminals (figures 7.21(a) and 7.21(b)).

2. The power terminals have an even number of pads (linking points between terminals and DBC substrate) in order to balance the current distribution and provide a higher mechanical robustness, as figures 7.21(a) and 7.21(b) show. Moreover, the terminal dimensions are also symmetric, in order to divide and distribute the current as equally as possible. The maximum reduction of terminal parasitic impedance is complicated because power layout, gate attack and power module mechanic constraints affect their design.



(a) Inductance of switching cells*.

(b) Inductance of *SiC* MOSFETs.

(c) Inductance of *SiC* diodes.

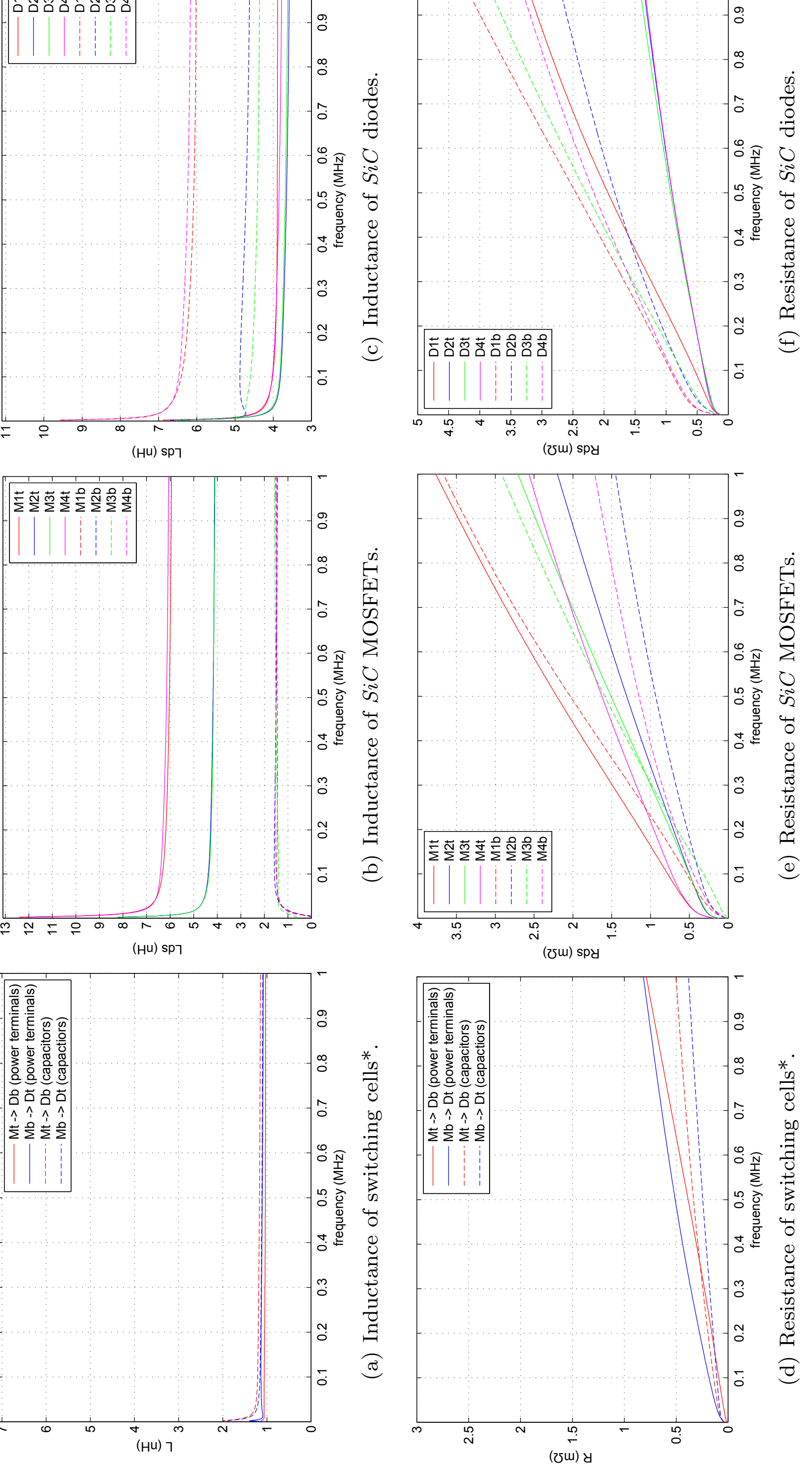
(d) Resistance of switching cells*.

(e) Resistance of *SiC* MOSFETs.

(f) Resistance of *SiC* diodes.

(*) *Power terminals*: the impedance measure is implemented by closing the circuit through power terminals. *Capacitors*: the impedance measure is implemented by closing the circuit through snubber capacitors.

Figure 7.17: Parasitic inductance and resistance for the *symmetric* DBC.



(a) Inductance of switching cells*.

(b) Inductance of *SiC* MOSFETs.

(c) Inductance of *SiC* diodes.

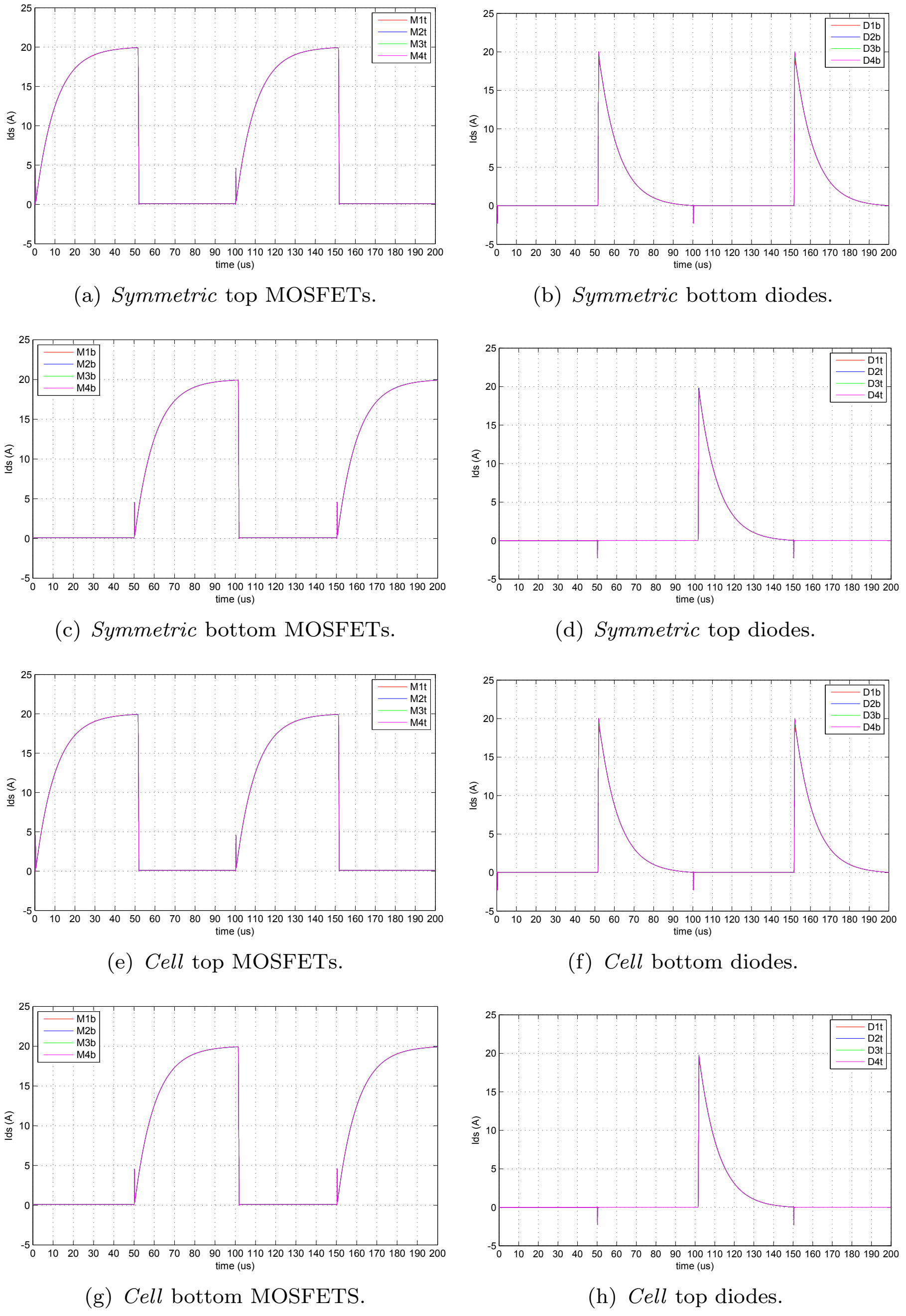
(d) Resistance of switching cells*.

(e) Resistance of *SiC* MOSFETs.

(f) Resistance of *SiC* diodes.

(*) *Power terminals*: the impedance measure is implemented by closing the circuit through power terminals. *Capacitors*: the impedance measure is implemented by closing the circuit through snubber capacitors.

Figure 7.18: Parasitic inductance and resistance for the *cell* DBC.



(a) *Symmetric* top MOSFETs.

(b) *Symmetric* bottom diodes.

(c) *Symmetric* bottom MOSFETs.

(d) *Symmetric* top diodes.

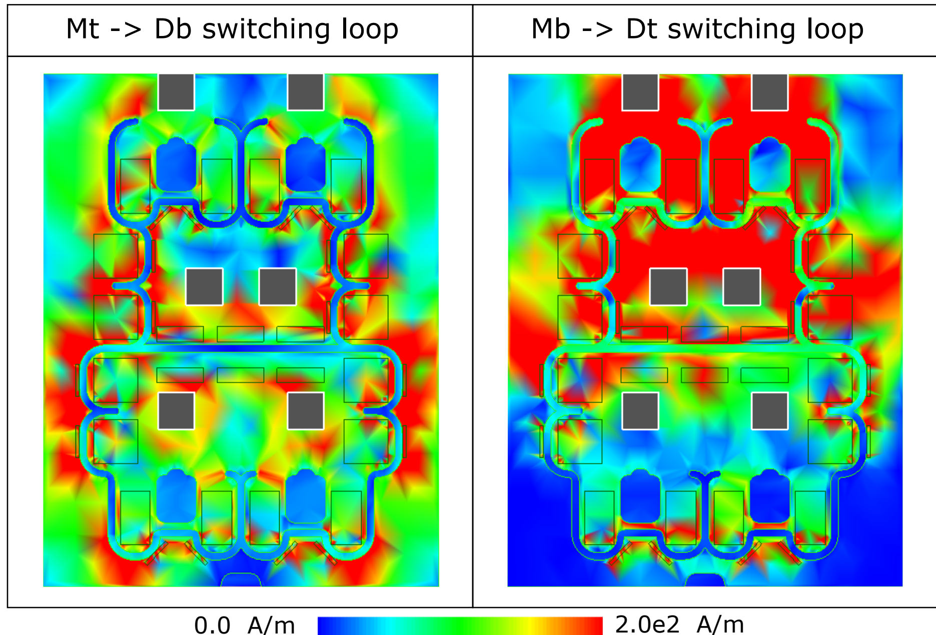
(e) *Cell* top MOSFETs.

(f) *Cell* bottom diodes.

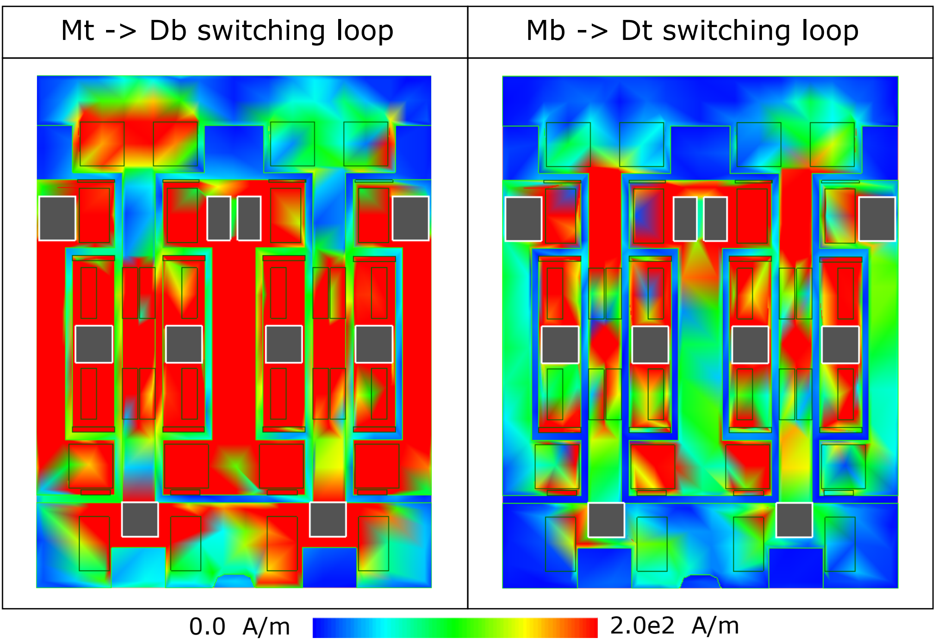
(g) *Cell* bottom MOSFETS.

(h) *Cell* top diodes.

Figure 7.19: Device switching loop currents for the *symmetric* and *cell* designs.



(a) *Symmetric* power layout switching cells.



(b) *Cell* power layout switching cells.

Figure 7.20: Power layout current density distribution for the *symmetric* and *cell* proposals.

3. The differential power connectors (positive and negative DC bus terminals) must be as close as possible each other in order to increase their coupling effect, which reduces parasitic inductance (figures 7.21(a) and 7.21(b)). Moreover, they should also be as wide and short as possible to decrease their equivalent stray impedances (the same approach than in power layout tracks).

The application of the design criteria explained in chapter 5 improves the power connector characteristics. The following simulations provide the impedance values of each terminal:

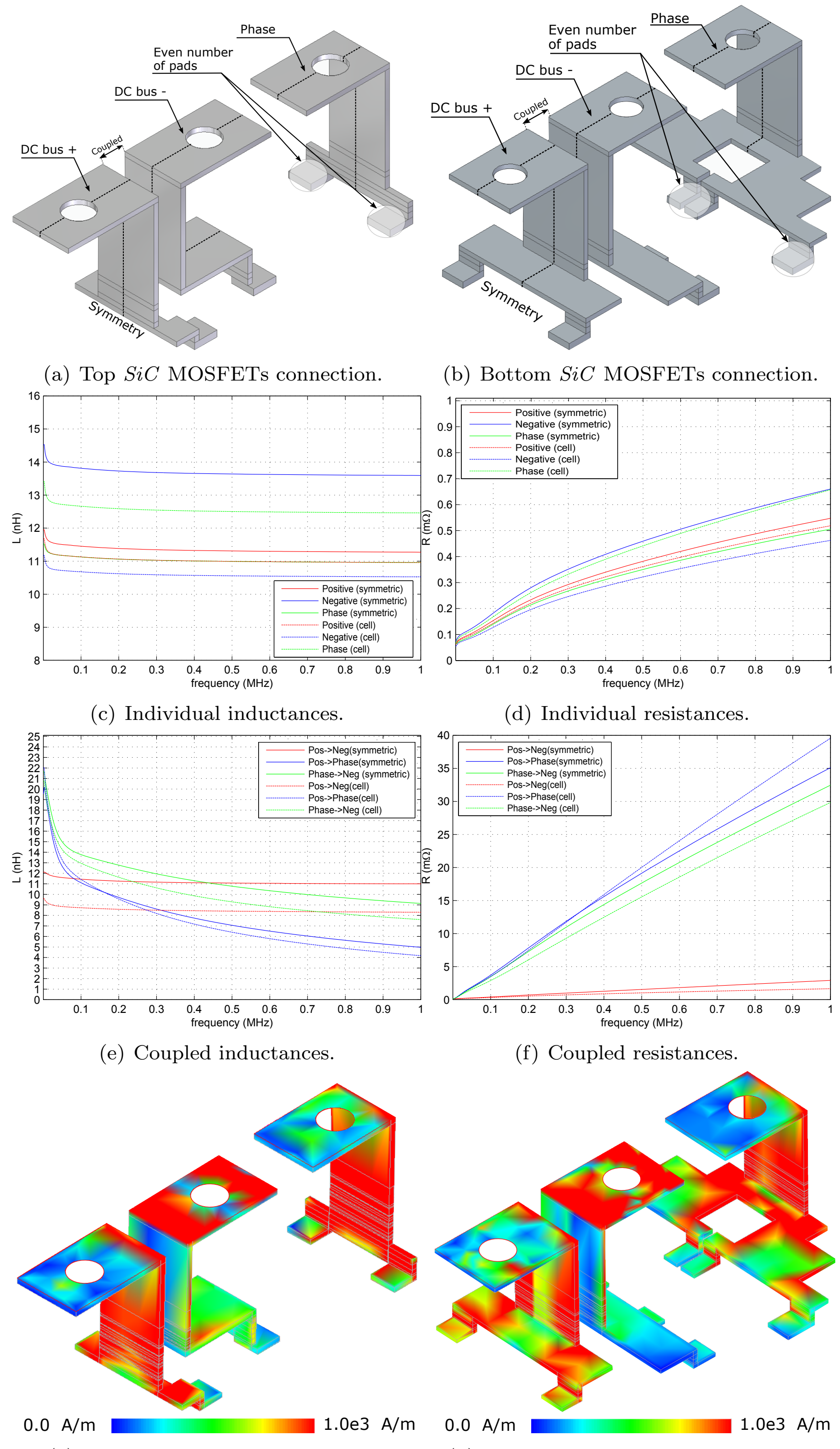
- *Symmetric* power terminals (figure 7.21(a)): the stray impedance values are shown in the figures 7.21(c) and 7.21(d), where the negative terminal has the highest value because it is the narrowest connector. These last data are taken individually, but there are coupling effects between power terminals. These effects are taken into account in the figures 7.21(e) and 7.21(f) where the impedance values are reduced due to this effect.

- *Cell* power terminals (figure 7.21(b)): in this configuration the power terminals are wider than in *symmetric* solution. For this reason, they present lower inductance values (<2 nH), as the figures 7.21(c) and 7.21(d) show. In this case, the wider power connector (negative terminal) has the lower impedance value (≃11 nH). As in the *symmetric* case, the coupling effects between power terminals reduce their parasitic values, as the figures 7.21(e) and 7.21(f) show. The resulting values are similar to those of the *symmetric* case.

Finally, the 3D current density distributions (10 kHz) from the figures 7.21(g) and 7.21(h) show that the symmetry applied in each power terminal enables to distribute homogeneously the current, which is the main goal to achieve in power connector design, together with the reduction of their stray impedance.

7.3 Thermal characterization: vertical substrate design

For an EV power module within a complete drive system, it is of great interest to study its dynamic performance under real or standardized driving conditions, as this will provide valuable information regarding system performance, reliability and life-cycle estimation. As it has been shown, a power module is a multilayer structure consisting of various materials, each with its particular Coefficient of Thermal Expansion (CTE). During thermal and power cycling, these CTE mis-



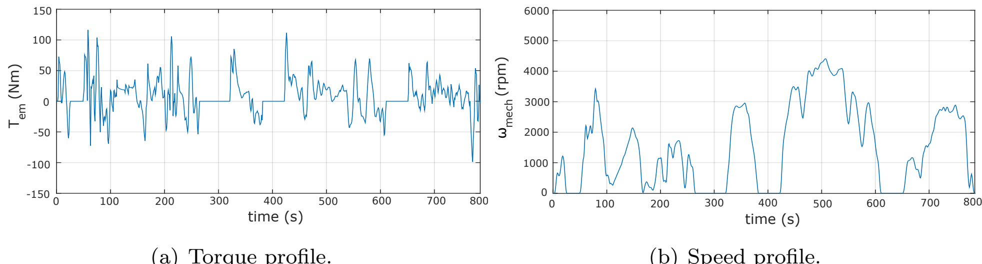
(a) Top *SiC* MOSFETs connection. (b) Bottom *SiC* MOSFETs connection.

(c) Individual inductances. (d) Individual resistances.

(e) Coupled inductances. (f) Coupled resistances.

(g) Top *SiC* MOSFETs connection. (h) Bottom *SiC* MOSFETs connection.

Figure 7.21: *Symmetric* and *cell* power connector impedances.



(a) Torque profile.

(b) Speed profile.

Figure 7.22: Torque and speed Fleet-BEV driving cycle profiles applied during the simulations.

matches produce thermo-mechanical fatigue, thus introducing possible mechanical failures over time and compromising the long term reliability of such critical elements. This issue is specially relevant in both solder layers and interconnection components.

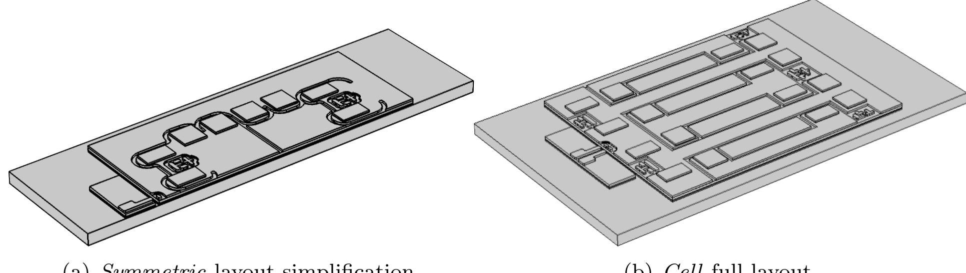
In this scenario, thermal simulations (electro-thermal) can be used to detect hot spots, (re)design and determine life-cycles of automotive power modules. In order to extract the thermal characterization of the proposed SiC half-bridges, the methodology proposed in appendix B is applied to get a hybrid electro-thermal simulation of an automotive power converter.

The converter of the simulated EV propulsion system is a two-level three-phase Voltage Source Inverter (VSI) that feeds a 64-kW automotive axial flux Surface Mounted Permanent Magnet Synchronous Machine (SM-PMSM). This inverter consists of three *SiC* half-bridge modules (*symmetric* or *cell* half-bridge solution). The electro-thermal data has been extracted from the power layouts, which are the part of *SiC* half-bridge more critical with the temperature.

The most significant mechanical parameters of the vehicle and the electrical and mechanical parameters of its particular propulsion system are shown in table 7.3. A driving cycle specifically created for EV driving characterization, named Flet-BEV-cycle, has been applied [380]. Such speed versus time driving profile has been processed considering the vehicular model in order to determine the instantaneous electric machine electromagnetic torque T_{em} (figure 7.22(a)) and mechanical speed ω_{mech} (figure 7.22(b)).

7.3.1 Definition of the power layout and initial approximation

In addition to the propulsion system set-up summarised in the table 7.3, the layout of the power module has to be well defined in order to apply the proposed thermal simulation methodology (appendix B). The geometry, the materials and



(a) *Symmetric* layout simplification. (b) *Cell* full layout.

Figure 7.23: Half-bridge power layouts used in COMSOL Multiphysics simulations.

the power semiconductors (heat sources) are the fundamental elements to be specified in the 3D model for the extraction of accurate Foster networks that provide the equivalent thermal behaviour.

The geometry of each *SiC* half-bridge solution is well defined throughout the section 7.2. Both the *symmetric* and *cell* power layout designs (figures 7.16(a) and 7.16(b), respectively) are horizontally symmetrical, which reduces the amount of Foster networks to be determined, because devices in symmetric positions will show equivalent thermal behaviours, as indicated in the following:

$$\begin{aligned} &M1t \equiv M4t;\;\; M2t \equiv M3t; M1b \equiv M4b;\;\; M2b \equiv M3b; \\ &D1t \equiv D3t;\;\; D2t \equiv D4t; D1b \equiv D3b;\;\; D2b \equiv D4b, \end{aligned} \tag{7.5}$$

where Mit and Mib represent the top and bottom *SiC* MOSFETs, respectively, and Dit and Dib represent the top and bottom SiC diodes, respectively, with $i = \{1...4\}$.

In the case of *symmetric* design (figure 7.16(a)), round and soft edges generate a mesh of higher resolution, which provokes the increase of computational load. Therefore, 3D model geometry can be simplified through the middle, as the figure 7.23(a)[1] show instead of the full layout of figure 7.23(b), reducing the amount of points to be evaluated. The symmetry allows to extrapolate directly the results to the other layout half.

The substrate of power module for the electrical characterization is defined in the figure 7.6. However, the thermal characterization requires a higher property definition of each material and solder/sinter layers[2], especially these last layers

[1]The COMSOL Multiphysics simulations requires a mesh reduction in order to process data. For this reason, a layout simplification is done, using design symmetry.

[2]The solder/sitner layers are excluded in the electrical simulations in order to reduce the computational load and simplify EM models.

Table 7.3: Main parameters of the simulated system for SiC half-bridge electro-thermal characterization.

Parameter	Symbol	Value	Units
Vehicle model parameters			
Vehicle total mass	M_{car}	1030	kg
Rotating mass	M_{rot}	5	%
Vehicle cross section	A_f	2.42	m^2
Wheel radius	r_{wheel}	0.29	m
Gravity acceleration	a_g	9.81	m/s^2
Rolling friction coefficient	μ	0.008	-
Air density	ρ	1.225	kg/m^3
Drag coefficient	C_d	0.367	-
Transmission model parameters			
Gear ratio	GR	6.2	-
Efficiency	η_{GR}	97	%
Idling losses	P_{Idling}	300	W
Electric machine parameters: AF130			
Maximum speed	ω_{max}	8000	rpm
Nominal torque	T_N	145	Nm
Peak torque (20 s)	T_p	350	Nm
Nominal power	P_N	64	kW
Peak power (20 s)	P_p	140	kW
Power converter nominal parameters			
DC link capacitance	C_{DC}	700	μF
Switching frequency	f_{sw}	10	kHz
Battery voltage	V_{batt}	360	V
Gate resistance (*on/off*)	R_G	5	Ω
SiC MOSFET parameters: CPM2-1700-0045B (Cree)			
Nominal current per switch	$I_{D,nom}$	48	A
Maximum blocking voltage	$V_{DS,max}$	1700	V
Operating junction temperature	T_{vj}	-40 to +150	^oC
SiC diode parameters: CPW5-1700-Z050B (Cree)			
Maximum current per switch	$I_{F,max}$	50	A
Repetitive peak reverse voltage	V_{RRM}	1700	V
Typical DC forward voltage	V_F	1.6	V
Operating junction temperature	T_{vj}	-55 to +175	^oC

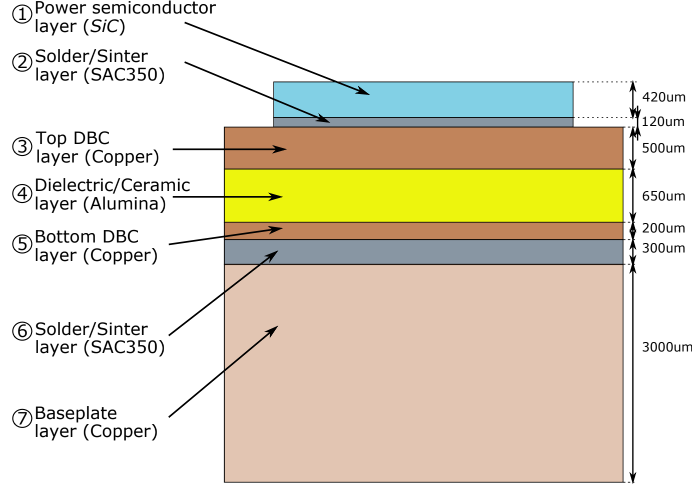


Figure 7.24: Power substrate for thermal simulations in COMSOL Multiphysics.

Table 7.4: Main properties of the DBC substrate for thermal simulation.

Property	Material/Layer (figure 7.24)			
	SiC ①	**SAC350** ② ⑥	**Copper** ③ ⑤ ⑦	**Alumina** ④
Heat capacity at constant pressure $(J/(kg \cdot K))$	1200	232	385	900
Density (kg/m^3)	3200	7370	8960	3900
Thermal conductivity $(W/(m \cdot K))$	450	55	400	27
Electrical conductivity (S/m)	1 e^3	61.6 e^6	5.998 e^7	-
Coefficient o thermal expansion (1/K)	-	18.9 e^{-6}	17 e^{-6}	8 e^{-6}

because of their relevance for thermal characterization, which are an assembly critical point. The stackup configuration for electro-thermal simulations is shown in the figure 7.24 and the material characteristics of each layer are summarised in the table 7.4.

As appendix B.1 details, a preliminary estimation of power losses is required prior equivalent Foster network extraction. In this context, the power loss distribution shown in figure 7.25 has been obtained for this particular case study.

7.3.2 Determination of the equivalent Foster networks

The power semiconductors are the points of interest to extract the equivalent Foster networks, as they are the heat sources of the power module. Besides, they

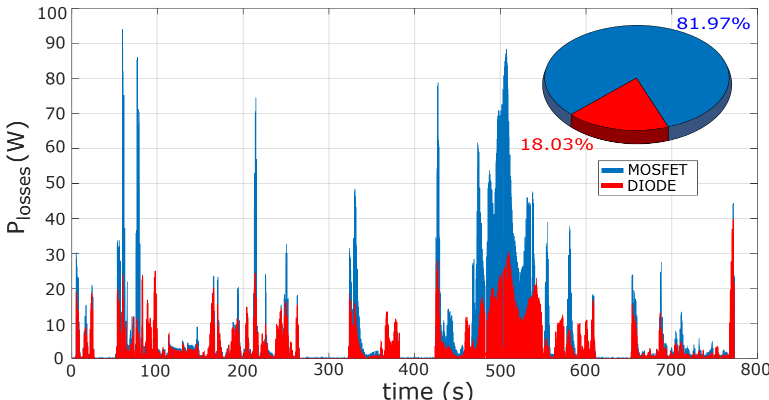


Figure 7.25: Initial power losses distribution between *SiC* MOSFETs and diodes.

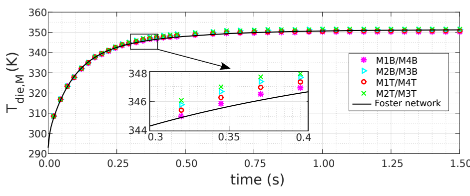
must be saved to avoid realiability issues. In order to obtain the RC networks of the *SiC* half-bridges, a power step (proportional to the previously determined power loss distribution) has been applied to each semiconductor in the 3D FEM model. As a result, the thermal transient responses of the devices have been obtained for each power module (figures 7.26(a) and 7.26(c) for the *symmetric* design and figures 7.26(e) and 7.26(g) for the *cell* design).

These results verify the layout symmetry application for each proposal (7.5). In addition and according to these results, the *symmetric* Foster representation of the devices can be simplified using a unique Foster representation for all the *SiC* MOSFETs of each half-bridge design, and another unique representation for all *SiC* diodes:

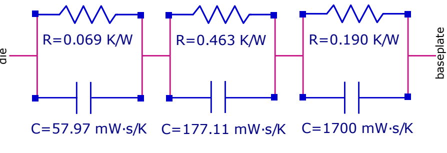
$$\begin{aligned} &M1t \equiv M2t \equiv M3t \equiv M4t \equiv M1b \equiv M2b \equiv M3b \equiv M4b;\\ &D1t \equiv D2t \equiv D3t \equiv D4t \equiv D1b \equiv D2b \equiv D3b \equiv D4b. \end{aligned} \tag{7.6}$$

Finally, by applying the RC network extraction procedure described in appendix B.3, an equivalent 3-stage Foster network has been calculated for the *symmetric* *SiC* MOSFETs (figures 7.26(b)) and equally for *SiC* diodes (figure 7.26(d)). In the *cell* case, top and bottom *SiC* MOSFETs and diodes are modelled as two RC networks (figure 7.26(f) and 7.26(h), respectively). The relative error of these RC networks is lower than 2 %[1]. Then, a quite good matching between the thermal responses and the fitted Foster network curves (figures7.26(a), 7.26(c), 7.26(e) and 7.26(g)) has been obtained.

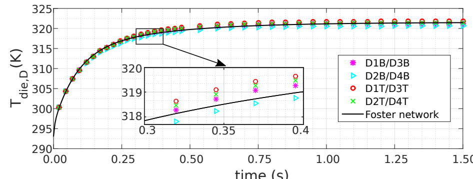
[1]The relative error has been extracted simultaneously during the extraction of equivalent RC networks.



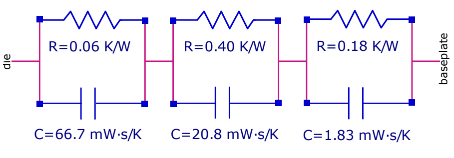
(a) Power step temperature response of the *symmetric SiC* MOSFET.



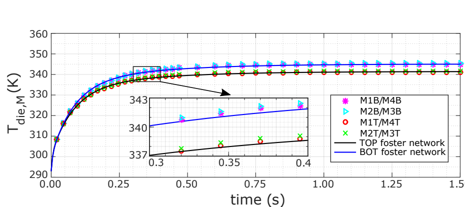
(b) Equivalent Foster network of *symmetric SiC* MOSFETs.



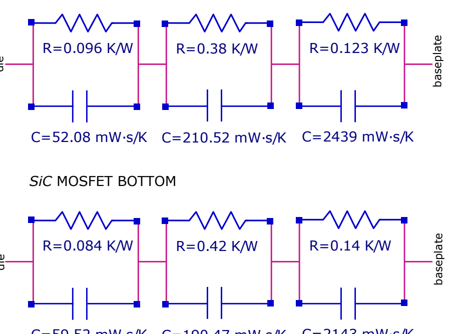
(c) Power step temperature response of the *symmetric SiC* diode.



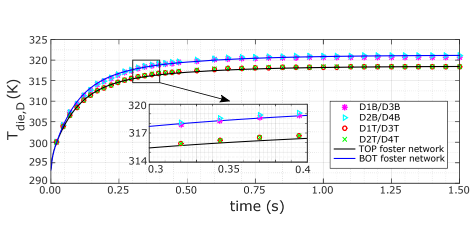
(d) Equivalent Foster network of *symmetric SiC* diodes.



(e) Power step temperature response of the *cell SiC* MOSFET.



(f) Equivalent Foster network of *cell SiC* MOSFETs.



(g) Power step temperature response of the *cell SiC* diode.

SiC Diode TOP

die R=0.065 K/W R=0.369 K/W R=0.156 K/W baseplate

C=56.92 mW·s/K C=222.22 mW·s/K C=2083 mW·s/K

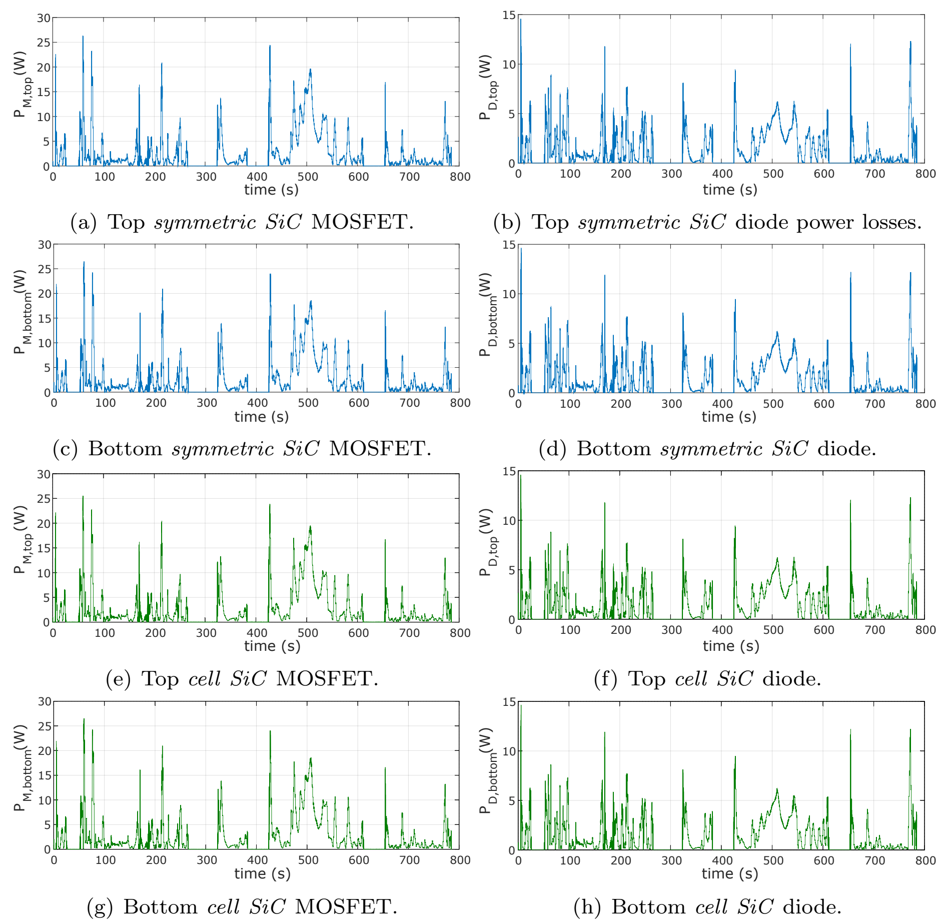
SiC Diode BOTTOM

die R=0.053 K/W R=0.42 K/W R=0.18 K/W baseplate

C=69.81 mW·s/K C=195.24 mW·s/K C=1806 mW·s/K

(h) Equivalent Foster network of *cell SiC* diodes.

Figure 7.26: Thermal responses and equivalent Foster networks for *symmetric* and *cell* half-bridge power layout.



(a) Top *symmetric SiC* MOSFET.

(b) Top *symmetric SiC* diode power losses.

(c) Bottom *symmetric SiC* MOSFET.

(d) Bottom *symmetric SiC* diode.

(e) Top *cell SiC* MOSFET.

(f) Top *cell SiC* diode.

(g) Bottom *cell SiC* MOSFET.

(h) Bottom *cell SiC* diode.

Figure 7.27: Power dissipation profiles of power semiconductors for *symmetric* and *cell* layouts: heat sources of the electro-thermal model.

7.3.3 Determination of power dissipation profiles by means of real-time simulation

The power dissipation profiles of the semiconductors have been later calculated using the 1D RT simulation platform of the proposed methodology in appendix B by introducing the equivalent Foster network extracted from the 3D FEM. Figure 7.27 shows such power dissipation profiles for a Fleet-BEV-cycle, where no significant differences between paralleled devices are found, as they are thermally modelled by identical Foster networks.

After obtaining such profiles, they have been imported into the 3D FEM in order to characterize the physical heat sources during the complete driving cycle. As the

FEM simulation has a much higher computational burden than a 1D model, an adequate averaging of the simulation inputs (power loss profiles) is fundamental to reduce the number of computed samples over the time without losing accuracy. The 1D RT simulation calculates power loss data with a high resolution (sampling time of 100 μs). Such data have been averaged applying a moving mean over a period of 50 ms.

7.3.4 3D temperature characterization of the power modules over the entire driving cycle

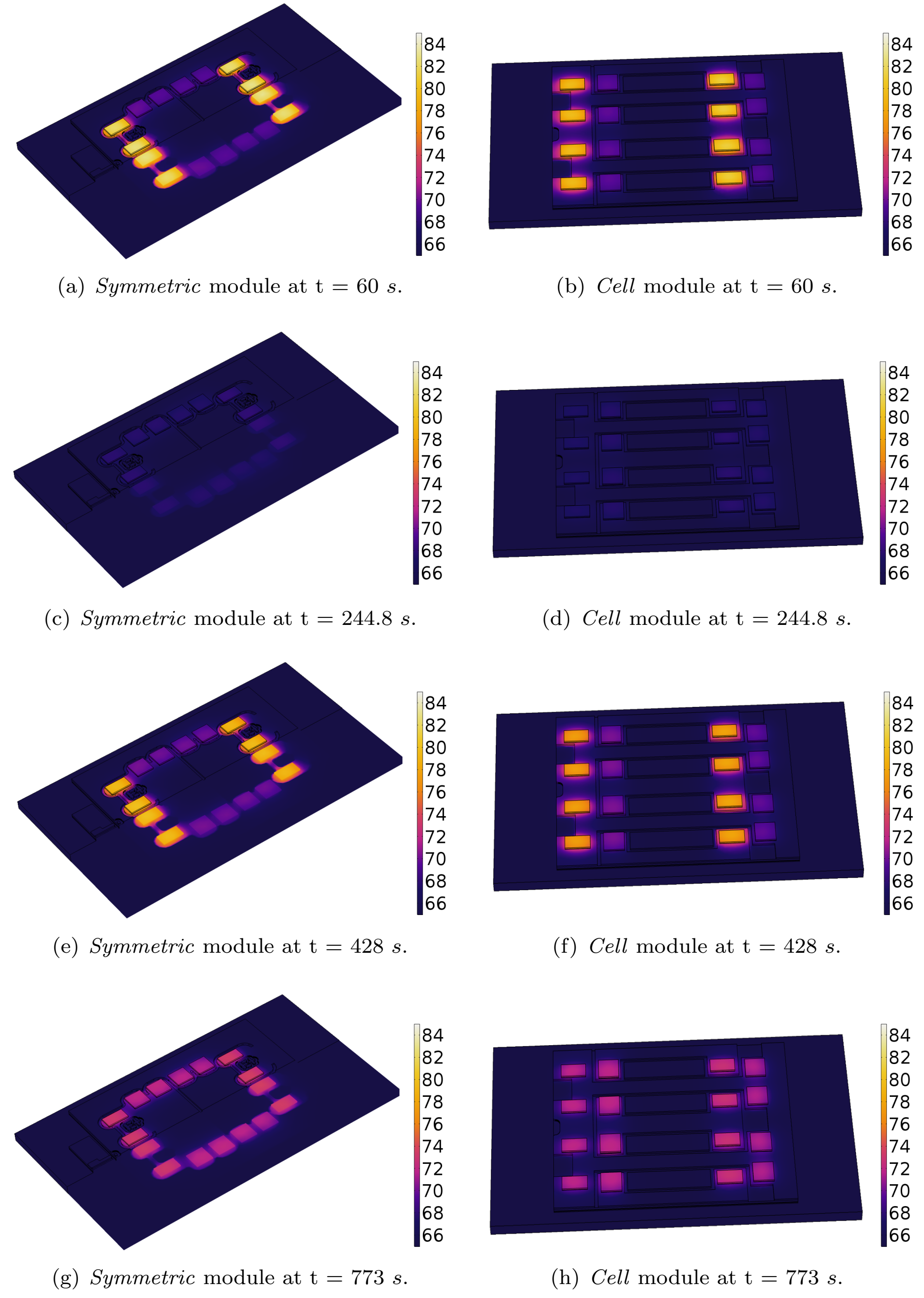
Considering the high computational resources requested by FEM transient simulations, simplifications based on the symmetry of the layout can be applied to significantly reduce the workload. In this case, considering the symmetry of the *SiC* half-bridges, it is possible to reduce the number of elements to be evaluated. For this reason, only one half of the power module needs to be simulated (using the symmetry axis, figures 7.23(a) and 7.23(b)), extrapolating the result to the other half.

From the application of the previously calculated power loss profiles over the 3D models, figures 7.28(a), 7.28(c), 7.28(e) and 7.28(g) show the thermal distribution of the *symmetric* half-bridge and figures 7.28(b), 7.28(d), 7.28(e) and 7.28(h) for the *cell* half-bridge in four relevant operation points during the application of the Fleet-BEV driving cycle. These results show that both power modules exhibit a good thermal distribution without significant asymmetries or excessive hot points.

As a final step and in order to validate the obtained results, the instantaneous temperature profiles calculated at each semiconductor junction by means of 1D and 3D simulation have been compared. A good matching between the temperature variations obtained by both methods can be observed in figure 7.29, where any power semiconductor of *symmetric* and *cell* power layout exceed the device maximum temperature during driving cycle. Additionally, the temperature results of both proposals are practically identical, thus indicating that the main factor of power module thermal behaviour is the substrate configuration. The power layout has a lower influence on thermal behaviour when power semiconductors are distributed symmetrically over the layout, and when distances between parallelized devices are minimal, as is the case of these power modules.

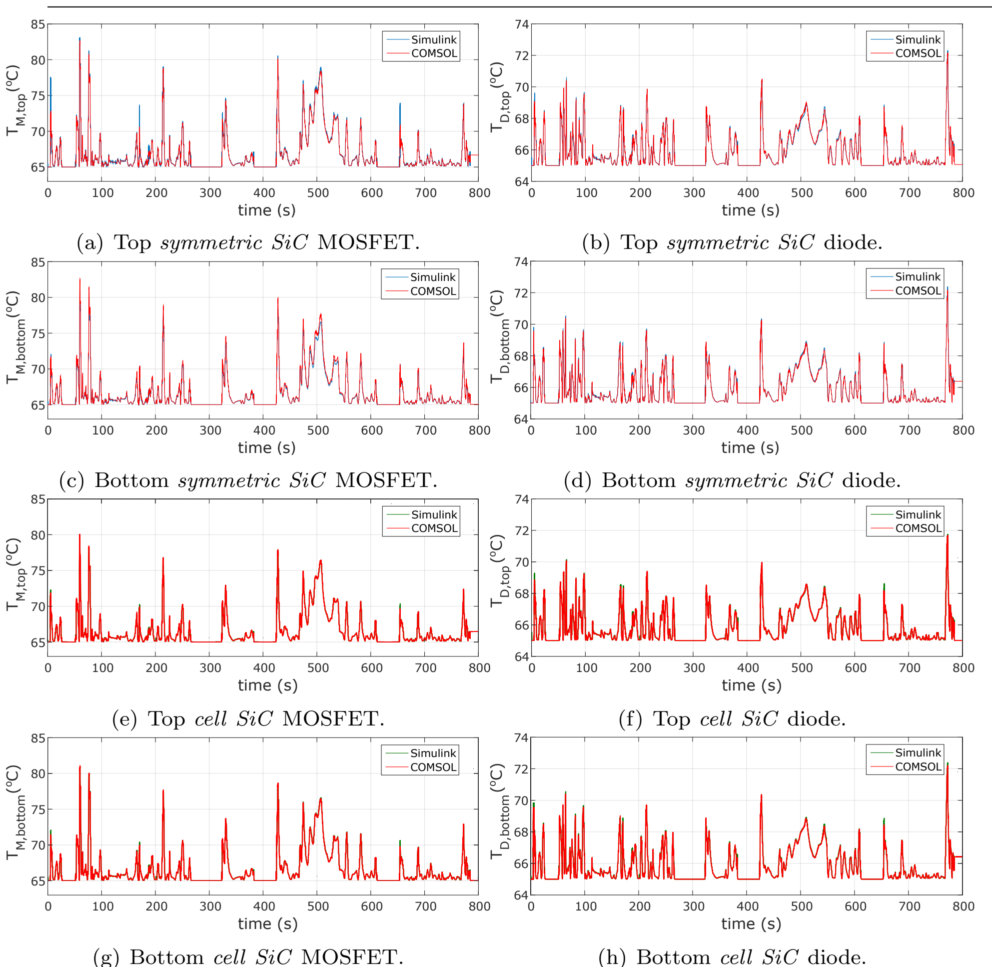
7.4 Conclusions

Considering the design of each half-bridge proposal, where parallelization and symmetry techniques are applied for *SiC* power semiconductors, the following



(a) *Symmetric* module at t = 60 *s*.
(b) *Cell* module at t = 60 *s*.
(c) *Symmetric* module at t = 244.8 *s*.
(d) *Cell* module at t = 244.8 *s*.
(e) *Symmetric* module at t = 428 *s*.
(f) *Cell* module at t = 428 *s*.
(g) *Symmetric* module at t = 773 *s*.
(h) *Cell* module at t = 773 *s*.

Figure 7.28: 3D temperature distributions (°C) obtained on the *symmetric* and *cell* power modules.



(a) Top *symmetric SiC* MOSFET.

(b) Top *symmetric SiC* diode.

(c) Bottom *symmetric SiC* MOSFET.

(d) Bottom *symmetric SiC* diode.

(e) Top *cell SiC* MOSFET.

(f) Top *cell SiC* diode.

(g) Bottom *cell SiC* MOSFET.

(h) Bottom *cell SiC* diode.

Figure 7.29: Junction temperature profiles of power semiconductors during the complete driving cycle for both *symmetric* and *cell* power modules.

conclusions can be drawn from the electrical characterization:

1. The two-level three-phase topology is the most common for medium HEV/EV applications, so the development of these *SiC* half-bridge prototypes are interesting solutions in order to test new solutions in the automotive market.

2. The usage of *SiC* power semiconductors makes the design task more difficult, where the reduction of stray impedances and track imbalances are the main design goal. However, these strict requirements provide new solutions such as hybrid substrates, power semiconductor placement and new

routing concepts based on RF technology in order to balance the electrical connections.

3. The mechanics imposes the main constrains in the development of these prototypes. For this reason, a common package (SEMITRANS) reduces the development process and provides a proven and mature technology instead of developing a new encapsulation.

4. The usage of a hybrid substrate based on two mature solutions, PCB and DBC, improves the traditional solution used in automotive, where the same DBC is employed for control and power signals. This hybrid stack-up gives more space and freedom for the routing of gate attack and power layout.

5. For interconnections, both half-bridge proposals use wirebonding technology. These wires are excluded from simulations due to the lack of information that is only provided by assembly companies. The *symmetric* and *cell* power modules have been designed with standard arrays of aluminium bonds in mind (typical power module solution). However, other solutions can be implemented without changing the layouts such as the usage of copper bonds or ribbon bonding, which present lower stray impedances.

6. The usage of embedded PCBs for control signals allows to route symmetrical tracks as wide and short as possible, reducing stray impedance effects. In both *symmetric* and *cell* proposals the maximum differences between parallelized connection are 1 nH and 0.5 mΩ, which causes negligible control signal imabalances. Moreover, the Kelvin connections isolate control signals from power loops and the PCB vertical stack-up allows implementing these signals in differential mode, thus mitigating EMI effects.

7. The number of power semiconductors is studied in order to have the best power module efficiency, taking into account the criteria of minimizing the amount of circuit components. The proposed power layouts reduce track stray impedances applying symmetry, wide connections, electromagnetic coupling and RF techniques without current imbalances, but attaining homogeneous current distributions. The *symmetric* power layout presents a better parallelization than the *cell* proposal, a maximum variation of 1 nH and 1 mΩ between devices. However, the *cell* solution exhibits lower absolute values than the *symmetric* alternative, approximately a reduction of 2 nH and 1 mΩ. In both proposals, meaningful current imbalances are not detected, as these variations are negligible.

8. The power connectors have been designed according to mechanic and layout constraints, making their stray impedances as low as possible. The *cell* terminals have lower inductance values than the *symmetric* design, but their

manufacture is more complicated due to their dimensions. The symmetry is also applied in their design, distributing the current as homogeneously as possible through power circuit contacts. However, in both *symmetric* and *cell* designs the power terminals imply an increment of design stray inductance of approximately 12 nH.

In addition to the electrical characterization, the thermal behaviour of the power substrate has been analysed in order to detect possible thermal imbalances. The proposed hybrid methodology (appendix B) can be considered as an useful tool for the thermal characterization of power automotive power converters, and also for the detection of reliability problems and design errors.

Hence, the following conclusions can be drawn from the thermal characterization:

9. The usage of a unique physical domain (thermal) in the 3D FEM reduces the computational burden and the number of convergence problems. This makes it possible to simulate long EV driving profiles with a duration of hundreds of seconds.
10. Accurate equivalent RC networks can be obtained according to the specific layout and layer materials. This is of great interest when studying novel power modules under design, as well as when analysing commercial power modules where no thermal data are provided.
11. The usage of a 1D RT platform significantly reduces the required time to carry out simulations without any significant accuracy loss.
12. The matching between the semiconductor temperature profiles obtained by 1D RT and 3D FEM simulations guarantees the confidence on the obtained results.
13. Critical differences between thermal impedances of the semiconductors are not detected through the thermal responses of the power devices in both proposals. Therefore, correction actions are not necessary to obtain more reliable systems.

Finally, after gaining knowledge on electrical and thermal behaviour by simulations, it is concluded that *symmetric* and *cell* half-bridges present similar values.

Chapter 8

Conclusions and future work

8.1 Conclusions

The environmental awareness received by diverse European, American and Asian agencies agree that the electrification of traditional vehicle fleet can help to reduce greenhouse gases and pollution effects. The replacement of combustion vehicles by Hybrid Electric Vehicles (HEV) or Electric Vehicles (EV) arises many challenges for the automotive industry, covering from legal aspects to new technical developments. From the technological point, the development of HEV/EV with the same capabilities or performance as fossil fuel requires the application of the newest technological advances in each part of the vehicle power train, that is, the battery pack, the power converter and the electric motor.

This thesis has been completely focused on the HEV/EV power converter, contributing to solve the lack of information for the design and the development of the power modules, proposing a specific design criteria. According to the literature, the main HEV/EV circuit architectures are based on multiphase conversion topologies where the inverter is the prevalence solution in industry. As it is described, this topology is constituted by three branches (three phases) of two-level, being the branch the constituting element in order to configure any multiphase topology. For this reason, the two-level branch, also known as half-bridge, is chosen as the power module topology of reference in this thesis.

The first part of this thesis document evaluates the power semiconductor technology alternatives suitable for HEV/EVs according to their technical requirements such as battery voltage and capacity, nominal and maximum currents, switching

frequencies, nominal operation, cooling architecture and others. In the power semiconductor market, there are two main trends which in principle can meet the HEV/EV requirements: Silicon (*Si*) and *Wide Bangap* (WBG) technologies. The *Si* material represents the alternative with the greatest maturity, being the IGBTs the semiconductors which dominate the power electronic market. For this reason, the IGBT technology evolution and trends have been analysed in detail in order to get an updated vision recalling its advantages and disadvantages.

Regarding the internal architecture of the IGBTs, there are two main blocks or parts, emitter side or IGBT cell and collector side or IGBT vertical structure. On the one hand, planar and trench technologies are used in the manufacturing of the IGBT cell in order to improve the emitter carrier conductivity. On the other hand, epitaxial or float zone wafers are employed in the collector side trying to control the device carrier lifetime. In the vertical structure, three main technologies are identified: PT (epitaxial), NPT (float zone) and FS (float zone). By default, these three vertical structures use planar cell technology, but the trench cell can be also applied over these vertical structures, as the Trench FS IGBT. Finally, the most modern IGBT developments are based on Trench FS, where advanced planar and trench technologies allow the integration of new functionalities as *freewheeling* diodes, the reduction of the device power losses and the improvement of its thermal behaviour.

Although the *Si* IGBT technology has reached an important maturity state, the *Si* material technology has certain limits such as switching frequencies and thermal conductivity which affect directly the development and future trends of HEV/EVs applications. For this reason, the WBG materials with possibilities to be exploited in automotive applications are studied in depth, being Silicon Carbide (*SiC*) and Gallium Nitride (*GaN*) the main options. In this study, *GaN* devices present good behaviours for high switching frequencies, but their lateral structure, the low thermal conductivity (similar to *Si*), the low voltage (650 V)/current ranges (10-20 A), the lack of maturity and reliability discard them for their current implementation for the power train. *SiC* devices provides a different perspective, because there is a major development level with a wider variety of devices (unipolar and bipolar devices) and voltage (600-1700 V)/current (10-50 A) ranges. Among the *SiC* devices analysed, *SiC* MOSFETs and *SiC* JBS diodes are the most suitable semiconductors for their implementation in HEV/EVs, not only their current status, but also their future perspectives of development. For these reasons, they are chosen as the power semiconductor of reference for the proposed power module design criteria in this thesis.

The second part of this research work has been focused on the analysis of the power module internal configuration in order to get the voltage and current ranges

that HEV/EV applications demand (approximately 300-400 V/255-480 A). The aforementioned voltage levels are obtained through two-level topologies, but the current ranges are extracted through the power semiconductor parallelization. In this thesis, the parallelization technique is analysed taking into account:

- The static and dynamic behaviour of the power semiconductors, where $V_{ce(sat)}$, $V_{ge(th)}$, $t_{d_{(on)}}$ and $t_{d_{(off)}}$ are the most remarkable device parameters, which are variable with semiconductor temperature (T_{vj}).
- The control signal connections (driver), where the definition of the gate impedance is paramount, specially the gate parasitic inductance ($L_{\sigma g}$).
- The power signal connections (power layout), where DC bus parasitic inductance ($L_{\sigma bus}$) and, specially, the emitter inductance ($L_{\sigma E}$) must be defined in order to avoid critical current peaks and feedback effects (decoupling power and control circuit parts).

After identifying the main problems that affect these parameters and the solutions which provide the scientific literature and commercial/industrial documents. It is detected that there are not complete technical references to implement parallel connections between power semiconductors. In fact, there are general concepts and ideas where the symmetry application is the main solution, without specific tips or examples to put into practice this concept. An important contribution of this thesis is the proposed design criteria for the design of power modules based on the research literature and industrial/commercial solutions. All this information has been processed in order to develop HEV/EV power modules taking into account the previous power semiconductor knowledge. The reference design is the half-bridge topology composed by parallelized *SiC* MOSFETs and *SiC* JBS diodes. The design criteria have been organised and classified taking into account the power module constituting parts: mechanics, substrate, gate attack, power layout and terminals. In each part the specific strategies are described through examples in order to balance electrical connections and reduce circuit stray impedances.

The last part of this PhD thesis is based on the practical application of the proposed design criteria and their validation through simulation techniques. The design of power modules requires multidisciplinary knowledge and the application of advanced concepts, so before exposing this development, three initial power circuits have been proposed and simulated according to the proposed design criteria. These circuits, which are parts of a power converter, have been designed in order to understand the parallelization and symmetry application at different levels such as a power switch, a half-bridge and a DC-link. These initial circuits are implemented on a PCB substrate because it eases the development of a power

design due to the substrate design flexibility and availability. In general, the simulation results show that the circuit alternatives with the best parallelization and symmetry application guarantee the balance of electrical connections. Focusing on each case of study:

- The power switch shows that the connections between the parallelized devices are critical in order to avoid feedback effects.
- The half-bridge topology shows that circuit tracks can be managed in order to get the best current balance without modifying the total parasitic inductance value and improving the current density distribution, where the application of RF techniques such as round and soft edges provides technical advantage.
- The DC bus circuit shows that a combination of two substrate technologies can reduce circuit parasitic inductance due to the increase of layers mutual coupling effect. Moreover, this circuit also shows that the proposed power module design criteria can be applied to other power circuits.

As indicated, the PCB has been used in preliminary designs. However, the usage of PCB stack-ups increases stray impedance values than other substrates configurations (e.g. DBC/DBA and AMB). Moreover, the current flowing capacity of PCB substrate is lower than DBC technologies and insufficient for HEV/EV medium power applications. For this reason, HEV/EV power circuits must be developed over a power module format. This thesis proposes two power module design alternatives, using the experience of the previous PCB circuits. The proposed half-bridge power modules (*symmetric* and *cell* configurations) have been designed trying to reduce electrical length connections and balancing (maximum variation of 1-2 nH between devices) the parallel *SiC* MOSFETs and *SiC* diodes connections on an hybrid substrate (a combination of DBC and embedded PCB). This stack-up configuration allows to route isolated gate attack from power layout, avoiding dangerous feedback effects and taking advantage of each substrate technology. Both the power modules implement the design criteria proposed in this thesis, but the *symmetric* power module applies an stricter symmetry concept than the *cell* design where connections are practically identical. In the case of the *cell* power module, the main benefits are due to the implementation of P- and N- Cells with snubber capacitors to reduce the electrical length between MOSFETs and diodes, aside from balancing power closed loops. According to the simulation results, both solutions do not show critical control signal delays and current imbalances. Moreover, a thermal study for each solution does not show hotspots that compromise the design integrity. This thermal characterization has been obtained thanks to a specific methodology developed in this thesis for the extraction of an electro-thermal model, where the combination of 1D and

3D simulation methods extracts the thermal behaviour of the power module proposals according to real operation conditions (specific driving cycle profiles for HEV/EVs).

Finally, the results extracted from this PhD thesis circuits and power modules highlight the utility of the proposed design criteria, thus obtaining power circuits with low stray impedances, electrically and thermally balanced. The application of this knowledge helps to reduce the prototyping design period, which constitutes the working basis where many electrical and thermal checks have been realised, which reduces the total design process time.

8.2 Main contributions

In this section, the main PhD thesis contributions are summarised, each contribution is related with the scientific publications and its corresponding document chapter:

1. **Analysis of silicon (*Si*) power semiconductor technology for medium power applications or automotive market: IGBT technology evolution.**

   An important point of this research is focused on the incorporation of new semiconductor materials (WBG) in the power electronics, specially in automotive industry. Nevertheless, the current status of power electronics based on silicon technology is necessary to know, where IGBTs are the proven solution. A deep technological review has been made, multiple IGBTs architectures and technologies have been studied, where each manufacturer uses its own nomenclature and developments, making difficult the designer task. For this reason, in this work the IGBT evolution and main architectures have been extracted, providing to the engineer a point of view without a deep knowledge of semiconductor physics.

   After studying the main IGBT architectures and properties, this work has been published in two article of a national conference (SAAEI - $N2$ and $N6$) and two international conferences (ISIE - $I2$ and IECON - $I3$).

2. **Updating state of commercial *wide bangap* (WBG) power semiconductors, specially *SiC* and *GaN*, providing range classifications and general view.**

   The present work highlights the WBG power semiconductors as a promising alternative for HEV/EV applications whereas *SiC* and *GaN* materials are the most relevant technologies for their introduction in automotive sector.

In addition to presenting each material advantage and disadvantage compared with silicon, the main commercial power devices of each material have been identified. On the one hand, *GaN* power devices are an interesting option due to the high switching frequencies and voltage ranges (650 V) and material expectations. However, a thorough study of *GaN* technology and its latest advances shows a trend change focus on high frequency research rather in power electronics. Additionally, the lack of maturity, the lateral structure of devices and the difficulty to find normally *off* transistors (HEMT/HFET) discard, nowadays, the usage of *GaN* technology for the present HEV/EV power train. On the other hand, *SiC* technology has a wider portfolio of power devices with commercial solutions such as BJTs, JFETs and MOSFETs. Thus, an exhaustive analysis of commercial *SiC* devices has been made in order to be applied in automotive applications. A general vision for each device of voltage and current ranges and their main characteristic parameter values have been reported. The analysis of *SiC* and *GaN* technology concludes that the most suitable devices to be applied in HEV/EV applications are *SiC* MOSFETs and *SiC* JBS diodes due to material, device development and future perspectives.

This work has been published in two international journal publications (RSER - $J1$ and $J3$) and three national conference publications (SAAEI - $N1$, $N2$ and $N5$).

3. **Development of power module design criteria, trends and technical aspects for HEV/EV applications.**

Apart from the analysis of *Si*, *SiC* and *GaN* power semiconductor for the development of power modules, the interconnections between these semiconductors need to be studied. Obtaining the voltage and current ranges required by HEV/EV through unique devices is a difficult task that provides poor results. Focusing on HEV/Ev application, the parallelization of power semiconductors is mandatory in order to get application power densities.

In the present thesis, it has been noted that in both scientific and industrial/commercial literature there is no exhaustive and detailed information about the design of power modules. Most of the aforementioned literature provides limited descriptions of specifics about substrate configuration, interconnection technologies and routing of gate control signals. Moreover, this information is partial, being limited to the electrical, mechanical and thermal information reported in the datasheets and application notes. There is not a reference document where a global vision of power modules main issues and solutions are collected. Thus, in this research work

local and particular solutions have been collected and processed in order to establish a complete and practical design criteria for the development of power module parts: mechanics, substrate, gate attack, power layout and terminals.

This contribution has been presented in two international journal publications (RSER - $J1$ and $J3$), two international conferences (IECON - $I3$ and PCIM - $I4$) and seven national conferences (SAAE - $N1$, $N2$, $N3$, $N4$ and $N8$).

4. **Practical application and data simulation extraction of the proposed design criteria on PCB technology.**

   Three power circuits have been proposed and simulated according to the proposed design criteria before introducing them on a whole power module. These circuits have been used to implement the parallelization and symmetry concepts exposed in the design criteria at different power converter levels: power switch, half-bridge and a DC-link.

   These circuits have been implemented on a PCB substrate as it provides more flexibility and freedom to develop each proposed design criteria concept. The obtained simulation results, using a co-simulation technology to extract electromagnetic models, show that the current imbalances are practically null or negligible in the circuits where the parallelization and symmetry levels are higher. Moreover, the usage of advanced RF techniques such soft and cutting edges provide a further improvement level, specially in the circuit current density distribution.

   This work has been reflected in two international conferences (PCIM - $I1$ and ISIE - $I2$) and two national conferences (SAAEI - $N1$ and $N2$), as the previous knowledge for the power module design final step.

5. **Design and simulation of half-bridge power modules according to the proposed design criteria, taking into account electrical and thermal characterization.**

   This thesis proposes two power module design alternatives, both designs are half-bridges with hybrid substrates made of DBC and embedded PCB, and with mechanic requirements based on SEMITRANS power modules. The two alternatives, *symmetric* and *cell* designs, have been designed reducing electrical length connections and balancing power semiconductors in parallel thanks to the application of the tips and concepts shown in the defined design criteria.

   The internal structure of these power module allows to isolate control sig-

nals from power layout, avoiding dangerous feedback effects and taking advantage of each substrate technology. Both the proposed power modules implement the thesis design criteria, but the *symmetric* power module applies an stricter symmetry and the *cell* design receives their main benefits from the implementation of P- and N- Cells with snubber capacitors. Each power module substrate, gate attack, power layout and terminals have been designed and simulated, without detecting critical control signal delays and current imbalances, and with good circuit current density distributions.

Apart from the electrical characterization of power module, their thermal characterization is also important. For this reason, an electro-thermal methodology has been developed in order to extract the thermal data for the two proposed power modules in order to detect reliability problems as hotspots. This methodology combines 1D and 3D simulations in order to reduce the computational load. Moreover, the two proposals have been evaluated through real operation conditions by means of the usage of HEV/EV driving cycle profiles. Both the proposals do not shown critical temperature concentrations over each proposed power layout.

All these contributions are been presented in two international journals (MR - $J2$ and RSER - $J1$), a national conference (SAAEI - $N7$) and a website publication (National Instruments - $W1$).

8.3 Scientific publications in the context of this work

The work developed in this thesis has been published partially in different journals, international conference and national congresses. In the table 8.1, the work published is related with each corresponding thesis chapter. The publications resulted from this thesis are the following:

❒ Publications in scientific-technical journals:

$J1$. **A. Matallana**, E. Ibarra, I. López, J. Andreu, J. I. Garate, X. Jordà and J. Rebollo. *"Power module electronics in HEV/EV applications: new trends in wide-bandgap semiconductor technologies and design aspects"*, Renewable & Sustainable Energy Reviews, vol. 113 (109264), pages 1-33, 2019. DOI: 10.1016/j.rser.2019.109264.

Impact Factor **(JCR): 10.556** (2018). Rankings: Q1 (1/35) *Green and Sustainable Science and Technology*, Q1 (7/103) *Energy and Fuels.*

*J*2. **A. Matallana**, E. Robles, E. Ibarra, J. Andreu, N. Delmonte and P. Cova. *"A methodology to determine reliability issues in automotive SiC power modules combining 1D and 3D thermal simulations under driving cycle profiles"*, Microelectronics Reliability, vol. 102 (113500), pages 1-9, 2019. DOI: 10.1016/j.microrel.2019.113500.

Impact Factor **(JCR): 1.483** (2018). Ranking: Q3 (179/265) *Engineering, Electrical and Electronic.*

*J*3. I. López, E. Ibarra, **A. Matallana**, J. Andreu and I. Kortabarria. *"Next generation electric drives for HEV/EV propulsion systems: Technology, trends and challenges"*, Renewable & Sustainable Energy Reviews, vol. 114 (109336), pages 1-23, 2019. DOI: 10.1016/j.rser.2019.109336.

Impact Factor **(JCR): 10.556** (2018). Rankings: Q1 (1/35) *Green and Sustainable Science and Technology*, Q1 (7/103) *Energy and Fuels.*

❒ Publications in international conferences:

*I*1. **A. Matallana**, J. Andreu, J. I. Garate, I. Aretxabaleta and I. Kortabarria. *"Analysis and design of a multilayer DC bus with low stray inductance and homogenous current distribution"*, Power International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), pages 1652-1659, Nuremberg (Germany), 2018.

*I*2. **A. Matallana**, J. Andreu, J. I. Garate, I. Martínez de Alegría and I. Kortabarria. *"Analysis of impedance and current distributions in parallel IGBT design"*, International Symposium on Industrial Electronics (ISIE), pages 616-621 , Edinburgh (United Kingdom), 2017. DOI: 10.1109/ISIE.2017.8001317

*I*3. **A. Matallana**, J. Andreu, J. I. Garate, I. Aretxabaleta and E. Planas. *"Analysis and modelling of IGBTs parallelization fundamentals"*, Annual Conference of the IEEE Industrial electronics Society (IECON), pages 3247-3252, Florence (Italy), 2016. DOI: 10.1109/IECON.2016.7793367

*I*4. I. Aranzabal, **A. Matallana**, O. Oñederra, I. Martínez de Alegría and D. Cabezuelo. *"Status and advances in Electric Vehicle's power modules packaging technologies"*, Power International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), pages 1785-1791, Nuremberg (Germany), 2016.

❒ Publications in national conferences:

$N1$. **A. Matallana**, J. Andreu, J. I. Garate, I. Kortabarri and E. Robles. *"Análisis y aplicación de simetría sobre diseños de layouts de convertidores de potencia con dispositivos SiC en paralelo"*, Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), pages 1-6, Valencia (Spain), 2017.

$N2$. **A. Matallana**, J. Andreu, J. I. Garate, , I. Martínez de Alegría and E. Ibarra. *"Análisis de las impedancias y distribuciones de corriente en diseños con IGBTs en paralelo"*, Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), pages 1-6, Valencia (Spain), 2017.

$N3$. I. Aranzabal, **A. Matallana**, O. Oñederra, I. Martínez de Alegría and D. Cabezuelo. *"Estado actual y avances en las tecnologías de ensamblado de los módulos de potencia asociados al vehículo eléctrico"*, Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), pages 1-6, Elche (Spain), 2016.

$N4$. **A. Matallana**, J. Andreu, E. Planas, J. I. Garate and D. Cabezuelo. *"Fundamentos para la paralelización de IGBTs"*, Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), pages 1-6, Elche (Spain), 2016.

$N5$. **A. Matallana**, J. Andreu, I. Kortabarria, E. Planas and I. Martínez de Alegría. *"Estado de la tecnología de dispositivos SiC y GaN"*, Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), pages 1-6, Elche (Spain), 2016.

$N6$. **A. Matallana**, J. Andreu, I. Aranzabal, V. López and A. Pérez-Basante. *"Estado del arte de la tecnología planar y trench de IGBTs de silicio"*, Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), pages 1-6, Zaragoza (Spain), 2015.

$N7$. **A. Matallana**, I. Kortabarria, J. Andreu, N. Arandia and J. Gutierrez. *"Metodología de implementación de un modelo tiempo real en LabVIEW"*, Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), pages 1-6, Zaragoza (Spain), 2015.

$N8$. J. Alcibar, E. Ibarra, J. Andreu, **A. Matallana** and I. Kortabarria. *"Vehículos eléctricos e híbridos: estado de la tecnología."*, Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), pages 1-6, Tangier (Morocco), 2014.

Table 8.1: Publications extracted form this PhD thesis and document chapters.

Chapter	Title	Publications
2	Silicon (*Si*) power semiconductor technology.	$I2$, $I3$, $N2$, $N6$
3	*Wide bandgap* (WBG) technology.	$J1$, $J3$, $N1$, $N2$, $N5$
4	Parallelization of power semiconductors.	$J1$, $J3$, $I3$, $N1$, $N2$, $N4$
5	Analysis and definition of the power module design criteria.	$J1$, $J3$, $I4$, $N1$, $N2$, $N3$, $N4$, $N8$
6	Parallelization of power converter circuits (PCC) according to the proposed design criteria.	$I1$, $I2$,$N1$, $N2$
7	*SiC* half-bridge module development based on the proposed design criteria.	$J2$, $J1$, $N7$, $W1$

Publications category	Number
Scientific-technical journals	3
International conferences	4
National conferences	8
Website publications	1
TOTAL	**16**

Table notes:
Jx: Publication in scientific-technical journal.
Ix: Publication in international conference.
Nx: Publication in national conference.
Wx: Publication on website.

❒ Publications on websites:

$W1$. **A. Matallana**, I. Kortabarria, J. Andreu, N. Arandia and J. Gutiérrez. *"Simulación en Real Time de una máquina PMSM conectada a un inversor en modo fuente de tensión"*, `http://sine.ni.com/cs/app/doc/p/id/cs-16522`, 2015.

8.4 Future work

This section identified the research lines that provides continuity the present work. The future proposed work lines are the following:

❒ **Tracking the *SiC* and *GaN* device evolution: new device generations, encapsulation technologies and commercial solutions.**

The analysis of WBG power semiconductors done in this work highlight

a fast evolution in the devices technologies, that it is specially remarkable in *SiC* devices, where new semiconductor generations have appeared during this PhD thesis development. Apart from more efficient and reliability devices, the new improvements are being focused on new packages and encapsulations in order to take advantage of *SiC* properties. Regarding *GaN* devices, it is to be expected improvements in reliability and device structure. Moreover, the first commercial *GaN* power module should appear soon. Therefore, the state of the art of the technology requires a continuous updating.

❒ **Manufacturing of the proposed power module prototypes and their starting up.**

There are few manufacturers in order to produce the proposed power modules. An identified partner for this task could be *Heraeus*. The communication with the assembly manufacturer is essential because the sinterization technology and wirebonding assembly must be defined. In addition to the technological challenges that the power module production imposes, the other circuits which constitutes the power module must be designed, such as the cooling system, the driver and the protections.

❒ **Development of a methodology to extract data from the prototypes in order to compare simulation and experimental data.**

The measurement procedures should be devised ad hoc because the power module is a complex and compact design where extra free space is not contemplated. It is expected deviation between simulation and experimental data because the results are directly dependent on the materials properties and surface contact, especially in terms of absolute values. Finally, the physical characteristic coefficients must be defined through experimentation in order to a calibrate simulation models, so this improvement of model accuracy helps to predict power module behaviours with simulation tools.

❒ **Application of the proposed design criteria in new power module trends, specially double side designs.**

The need to develop more efficient and compact applications is causing the emergence of new assembly techniques as double side power modules, where the routing space is incremented at two DBC levels. Doubled the DBC routing area provides advantages and, at the same time arises new technical challenges. This new design environment can produce unforeseen working states of the former designs, that must be dealt with.

8.5 Acknowledgements

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- The technical and human support provided by IZO-SGI SGIker of UPV/EHU and European funding (ERDF and ESF).

Appendix A

Extraction of parasitic elements from the designed power electronic modules

Power printed circuit board (PCB) or direct bonded copper (DBC) presents structural parasitic impedances such as path inductances and resistances with their corresponding substrate capacitances (figure A.1) [381]. It is important to consider the parasitic inductance effects because the $L \cdot di_L/dt$ generates overvoltages and other effects which affect circuit operation [382, 383]. In a power module design, controlling layout physical dimensions is fundamental to use each chip at maximum ratings. For this reason, layout needs to be as symmetrical as possible disposing power semiconductors, linking traces and external pins, so overvoltages and current imbalances are reduced [384]. Nowadays, power modules operate at higher frequencies and designs are more compact, so the effects of parasitic inductance coupling increase electromagnetic emissions [337].

In order to understand current distributions and to predict circuit behaviour [376, 385], an analytical model is necessary to obtain, taking into account non ideal effects of layouts [386]. For this, the Partial Element Equivalent Circuit (PEEC) or Electromagnetic Method (EM model) can be applied.

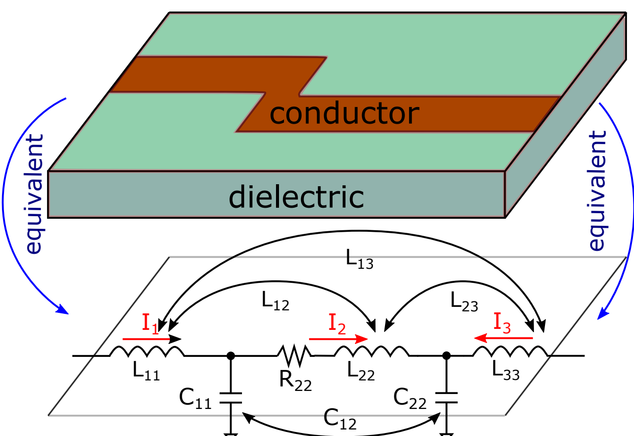


Figure A.1: Parasitic elements of paths in power layouts.

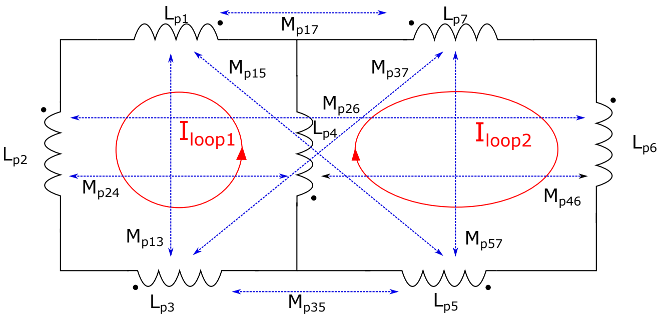
A.1 Partial Element Equivalent Circuit (PEEC)

The parasitic elements in a power circuit can be represented by partial element equivalent circuit (PEEC) where each layout structure can be modelled by resistance (R), autoinductance (L_p) and mutual coupling inductance (M_p) between traces [347, 383, 387, 388]. Figure A.2(a) shows the PEEC equivalent circuit of two rectangular loops with one segment in common. The electrical loop behaviour depends on circuit elements proportional to coplanar physical l, w and t dimensions (figure A.2(b)) and some material characterisitics as resistivity (ρ) and permeability (μ). Therefore, each path or trace is simplified as R (A.1), L_p (A.2) and M_p (A.3) for low frequencies (<1 MHz) [369, 389, 390]. Moreover, M_p depends on current direction to be added or subtracted in the total loop inductance value (L_{loop}). In the circuit shown in figure A.2(a), M_p values are added because loops have the same current direction through inductances, so L_{loop_1} and L_{loop_2} can be obtained as (A.4) and (A.5), and total mutual inductance M_{12} is (A.6).

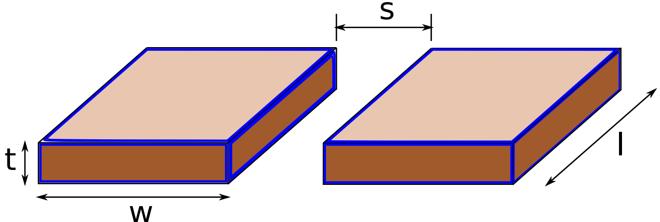
$$R = \rho \cdot l \cdot 10^3 \cdot w/t; \tag{A.1}$$

$$L_{pi} = 0.00508 \cdot \left(\frac{l}{25.4}\right) \cdot \cdot \left(2.303 \cdot log_{10}\left(\frac{2 \cdot l}{w+t}\right) + 0.5 + 0.2235 \cdot \frac{w+t}{l}\right); \tag{A.2}$$

$$M_{pij} = \frac{\mu}{\pi} \cdot cosh^{-1}\left(\frac{w+s}{w}\right) \cdot l. \tag{A.3}$$



(a) Two loops with one common segment solving with PEEC.



(b) Coplanar plate inductance geometrical dimensions.

Figure A.2: Extraction of parasitic elements of a circuit.

$$\begin{aligned} L_{loop1} &= L_{p1} + L_{p2} + L_{p3} + L_{p4} + 2M_{p24} + 2M_{p13}; \\ &where\ M_{p24} = M_{p42};\ M_{p13} = M_{p31}; \end{aligned} \tag{A.4}$$

$$\begin{aligned} L_{loop2} &= L_{p4} + L_{p5} + L_{p6} + L_{p7} + 2M_{p46} + 2M_{p57}; \\ &where\ M_{p46} = M_{p64};\ M_{p57} = M_{p75}; \end{aligned} \tag{A.5}$$

$$\begin{aligned} M_{12} = M_{21} = &M_{p15} + M_{p17} + M_{p24} + \\ &+ M_{p26} + M_{p37} + M_{p35} + M_{p46} + L_{p4}. \end{aligned} \tag{A.6}$$

However, in the layout design there are several number of interconnections with their coupling inductances. The electrical model becomes very complex to be solved analitically and only provides a constant current density [391, 392]. For this reason, other methods are necessary to calculate stray elements effects even though, they suppose a higher computational load.

A.2 Mesh model development for non ideal circuit simulations

An electrical simulator is necessary to process thousands of equivalent component connections. With a 3D mesh is possible to show non uniformities in current distribution taking into account two perpendicular directions [346, 391]. Keysight ADS^{TM} software provides a tool to analyse the design equivalent impedances. The software is based on input/output microwave technology to get the scattering matrix (A.7) [393] for a particular frequency.

$$S_{ij} = \left. \frac{V_i^-}{V_j^+} \right|_{V_k^+=0 \ for \ k \neq j} \tag{A.7}$$

It is necessary to transform S-parameters in Y-parameters (A.8), since Y_{11} parameter gives directly the equivalent admittance value short-circuiting the load [393]. The R and L values are calculated applying (A.9).

$$Y_{ij} = \left. \frac{I_i}{V_j} \right|_{V_k=0 \ for \ k \neq j}; \tag{A.8}$$

$$R = \Re\left(\frac{1}{Y_{11}}\right); \ L = \frac{\Im\left(\frac{1}{Y_{11}}\right)}{2 \cdot \pi \cdot freq}. \tag{A.9}$$

The mesh is formed by a lot of cells which include parasitic elements (figure A.1), taking into account the mutual interaction of cell elements. Then, a co-simulation between power semiconductor electrical models and the layout S-parameters give a non ideal circuit behaviour during transit simulation which helps to understand voltage and current distributions.

The S-parameters are extracted through Momentum tool, based on the technique of moments method [394, 395]. This technique solves the Maxwell equations for embedded planar structures over multilayer substrates. For low frequencies (<1 MHz), the Green ($G(r, r')$) substrate functions are obtained, extracting real L and C elements. The basic equations (A.10) - (A.14) allow to calculate the system current. These equations express the electrics ($E(r)$) and magnetics ($B(r)$) field as functions that depend on potential ($A(r)$) and scalar ($V(r)$) vectors.

$$\sum_{i=1}^{N} Z_{i,j} \cdot I_j = V_i; \tag{A.10}$$

$$V_i = \iint_S dSB_i(r) \cdot E(r); \tag{A.11}$$

$$Z_{i,j} = j\omega L_{i,j} + \frac{1}{j\omega C_{i,j}}; \tag{A.12}$$

$$L_{i,j} = \iint_S dSB_i(r) \cdot \iint_{S'} dS'G^A(r,r')B_j(r'); \tag{A.13}$$

$$\frac{1}{C_{i,j}} = \iint_S dS\nabla \cdot B_i(r) \cdot \iint_{S'} dS'G^V(r,r')\nabla \cdot B_j(r'). \tag{A.14}$$

A.3 *Arina* (SGIker)

The computational load in order to extract EM models from circuits is very high. For this reason, the usage of a High Performance Computing (HPC) system is necessary. The figure A.3 shows the data transfer process between the local host and the distributed system. Moreover, this figure also shows some details and simulation setup parameters in order to run the calculation of the equivalent EM model. In the particular case of this thesis, the SGIker HPC (*Arina*) has been used. It gives service to the entire scientific community of the Basque Country, including researchers from the UPV/EHU, but also to the entire scientific and industrial community. The service holds, since 2004, an HPC cluster that has regularly been expanded to meet the growing demand of HPC resources by the wide variety of research groups covering all areas of science.

A.3.1 Infrastructure

An HPC cluster is not standard IT equipment, it is a complex scientific equipment assembled with very specific elements. As that, it requires highly qualified personnel and should be placed in a space designed to guarantee its optimal performance. The HPC cluster of the IZO-SGI has been designed internally to satisfy the needs of a broad spectrum of researchers as a single heterogeneous computing entity. The resources are summarized below:

- ❒ Bianual resources update policy.
- ❒ 3728 computational cores with IA64 and x86-64 architectures that allow the execution of standard and massive calculations..
- ❒ 6 Nodes with 2 Nvidia GPGPUs each to exploit the programs that use this new technology.

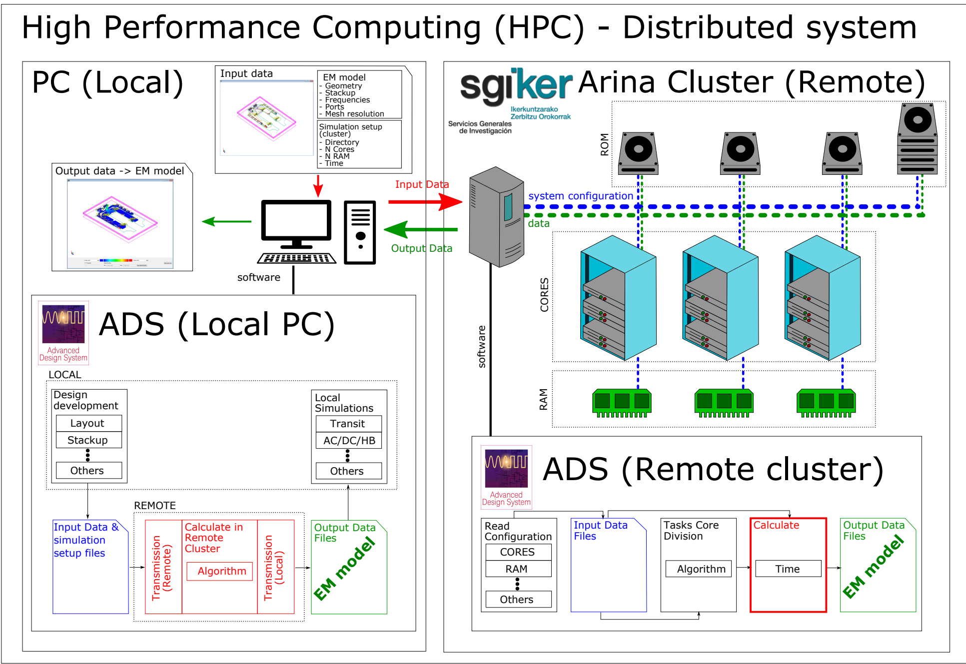


Figure A.3: Communication and processes diagram between local host and *Arina* cluster.

- Nodes with large RAM for jobs with these specific requirements (up to 512 GB of RAM).
- High performance, high capacity and high read/write speed file systems based on Lustre. Three different systems with up to 40 TB of storage and 7 GB/s read and write speed.
- Everything interconnected with a high bandwidth and low latency InfiniBand network. The last acquisition with 56 Gb/s Infiniband FDR.
- Management servers under high availability to ensure 24h*365 operation.
- Everything installed in the Data Processing Center (DPC) of the UPV/EHU with a all the elements to ensure optimal performance of the cluster (see next point for details of the DPC).

A.3.2 Data processing center

The equipment is installed in the DPC of the UPV/EHU newly built in 2006. The DPC has 450 m^2 and is intended to guarantee the proper and continuous functioning of the computers hosted therein. For that, it is fully equipped with elements that makes possible the 24x7x365 functioning of the cluster:

- Precision air conditioning systems exclusive and direct expansion water softening system. 7 air conditioning units with an aggregate capacity of 208 kW, ensuring N+1 redundancy against failure.
- Fire detection system using optical and thermal detectors. HI-FOG water mist extinguishing system that preserves the integrity of computer equipment in case of activation.
- Connection to two separate electrical power transformers.
- Double electric branch for IT equipment, each with independent UPS (uninterruptible power supplies) and separate low voltage boxes. It allows redundancy and maintenance without power off of the electrical installation.
- 75 kVA power generator with two days of autonomy without refuelling.
- Access control, alarms and security by closed circuit TV. Apart from user and systems data backup.
- Monitoring, management and control by in-situ operators with 5S method to improve the quality.

The facilities are monitored in-situ and remotely with maintenance and periodic revisions in order. The ICT department has a secondary DPC in another building, that keeps duplicate the basic services to prevent operation failures in an event of a major disaster.

Appendix B

Thermal 1D and 3D simulations for driving cycle profiles

A power module is a multilayer structure consisting of various materials (silicon, copper, ceramic materials, etc.), each with its particular Coefficient of Thermal Expansion (CTE) [319]. During thermal or power cycling, these CTE mismatches produce thermo-mechanical fatigue, introducing possible mechanical failures over time and compromising the long term reliability of such critical elements [396]. This issue is specially relevant in both solder layers and interconnection components (i.e, bond wires) [397]. In this scenario, electro-thermal simulation can be considered a powerful tool to analyse, determine hot spots, (re)design and determine life-cycles of the power modules during early development stages [396, 398–401] following a DfR approach [396]. In this way, design errors and reliability problems can be found and solved before the expensive prototyping stage, accelerating the whole R&D process and meeting the life-cycle requirements of the automotive industry (i.e., about 10 to 15 years of failure-free operation [396]).

When performing electro-thermal simulations of an EV power module within a complete drive system, it is of great interest to study its dynamic performance (electrical and thermal) under real or standardized driving conditions [402], as this will provide valuable information regarding system performance, reliability and life-cycle estimation [401]. In this context, a number of standardized driving cycles have been proposed in the last decades to evaluate the system behaviour

Table B.1: Qualitative comparison between 3D FEM, 1D Cauer/Foster and the proposed hybrid simulation procedures.

Features	3D FEM	1D Cauer/Foster	Proposed hybrid methodology
Computational load	✗	✓✓	✓
Simulation complexity	✗	✓✓	✓
Integration of thermal properties(1)	✓✓	✗	✓✓
Integration of electrical properties(2)	✗	✓	✓
Number of evaluation points(3)	✓✓✓	✗	✓✓✓

Table notes:
(1) The 3D FEM uses thermal physics, the 1D procedure uses equivalent Cauer/Foster networks (simplification and loss of information).
(2) The 3D FEM uses electrical physics, the 1D Cauer/Foster procedure uses the power semiconductor loss models.
(3) The 3D FEM evaluates the complete layout, while the 1D Cauer/Foster procedure only evaluates only some points of it.

under real operation conditions. For example, the New European Driving Cycle (NEDC) [403] has been used in Europe, although it is being substituted by the Worldwide Harmonized Light-Duty Vehicles Test Procedure (WLTP) [404]. Such cycles are suitable for gasoline and diesel vehicles; however, various specific cycles are being defined in order to characterize the driving conditions of EVs, as the way of driving such vehicles is heavily conditioned by the range anxiety phenomena [405].

Finite Element Method (FEM) simulation is commonly used for the realization of accurate 3D electro-thermal simulations [406, 407], allowing full layout characterization (table B.1). However, there are significantly different time-constants involved in the model (ranging from microseconds to characterize the electric machine, power system behaviour and instantaneous power losses, to hundreds of seconds to characterize the vehicular model and the driving cycle itself), and also various physics to be simulated; thus, the complexity and computational burden becomes excessive to exclusively rely on 3D FEM for long driving cycle simulation [408, 409]. On the other hand, simplified thermal simulation approaches based on equivalent 1D Foster and Cauer (RC) networks [400, 410] can be conducted, as the computational burden is significantly lower (table B.1). However, if only this simulation method is used, the designer is not able to characterize the thermal distribution of the whole power module.

In order to simplify, speed up the whole electro-thermal simulation stage and achieve highly accurate and representative full layout results, a complete methodology that combines the usage of 3D FEM, simplified 1D modelling and real-time (RT) simulation is proposed in this thesis. In this way, the accuracy of physical

simulation (for power module thermal characterization) and fastness of real-time simulation (for vehicular and drive system simulation) are mixed, obtaining the best features of both worlds. In order to show the benefits of the proposal, such methodology has been implemented during the electro-thermal simulation stage of a *SiC* based half-bridge power module (composed by four *SiC* MOSFETs with their corresponding anti-parallel freewheeling *SiC* JBS diodes). In particular, COMSOL Multiphysics software has been used to solve 3D thermal FEM simulations, while an OPAL-RT OP4510 digital platform has been used to conduct real-time simulations with 1D thermal characterization over the standardized driving cycles. The obtained results of chapter 7.3 show the convenience of the proposed work-flow, as accuracy for thermal characterization is guaranteed while reducing the time required to carry out all the simulations.

In the following, the work-flow of the proposed modelling and simulation procedure and its associated tools are described.

B.1 Proposed hybrid 1D/3D electro-thermal procedure

Figure B.1 shows the general diagram of the proposed hybrid 1D/3D electro-thermal simulation procedure. The block of the left hand of figure B.1 (in blue) represents the steps to be carried out by 1D RT simulation, while the block of the right hand (in green) shows the steps to be carried out using 3D FEM analysis. Between both blocks, a number of steps that must be carried out in order to process data from 1D to 3D, and vice versa, are represented.

As a first step, a preliminary estimation of the power losses is conducted using the RT electro-thermal model. This model must consider the driving profiles of the vehicle, together with the controller, power electronics and electric machine model to estimate such losses under realistic driving conditions. As the virtual junction temperature of the devices $T_{v,j}$ has a significant influence on the instantaneous transistor ($P_{loss,M}$) and diode ($P_{loss,D}$) power losses, its influence must be modelled to achieve sufficiently accurate results. In this step, the 1D equivalent network is not yet available; thus, constant nominal temperatures are considered as a first approximation. Once the power loss profiles of all semiconductors during the whole driving cycle have been obtained, the average power loss distribution between the elements is determined ($\%_{loss}$). Thanks to this, adequate power steps are defined as inputs for the 3D FEM heat source characterization stage. From the thermal response results ($T_{die,M}$, $T_{die,D}$) of such power loss steps obtained by FEM, the equivalent thermal impedances of the

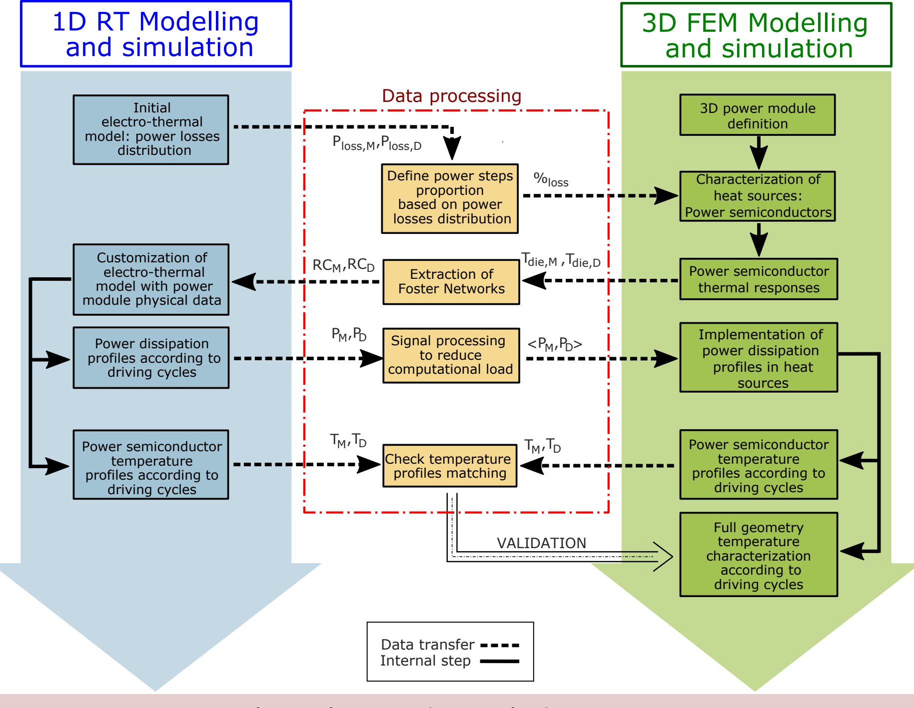


Figure B.1: General diagram of the proposed methodology to characterize the electro-thermal behaviour of an automotive power module through driving cycles.

power semiconductors are extracted by their post-processing. Being this point of particular importance for the accuracy of the results, the post-processing procedure is thoroughly explained in section B.3. Once the equivalent Foster networks (RC_M, RC_D) are calculated, they are implemented in the 1D RT model and the power loss profiles (P_M, P_D) are re-calculated, also obtaining the temperature profiles (T_M, T_D) corresponding to the $T_{v,j}$ of all the semiconductors (and the ones corresponding to the intermediate points that are represented by the simplified 1D Foster network).

In the following step, the power dissipation profiles are averaged ($< P_M, P_D >$) (by post-processing), and they are introduced for the complete driving cycle simulation in the FEM model, significantly reducing the required computational burden. As a result, a complete figure of the power module thermal distribution through the driving cycle is obtained, which allows the detection of hot points and incorrect thermal distributions through the designed layout. This information will be used to detect reliability problems and support the design process of the module.

As a final step, the matching between the temperature profiles (T_M, T_D) obtained by means of the 1D and 3D methods over the driving cycles is carried out, as this can be used to confirm the correct characterization of the heat sources and power module. The details of the 1D RT and 3D FEM modelling and simulation are explained in sections B.2 and B.3, respectively.

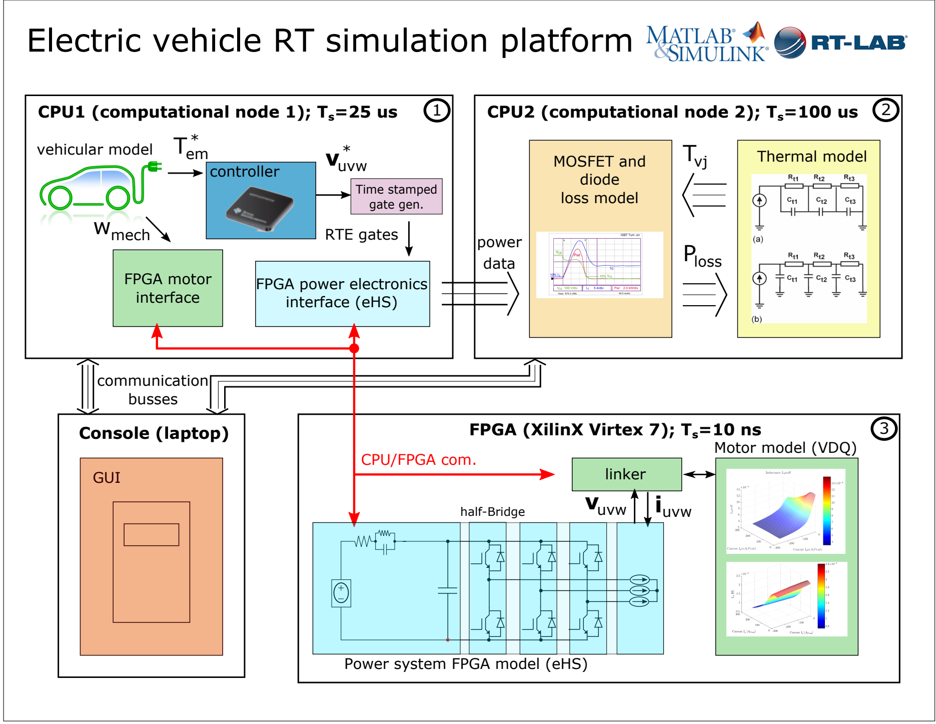
B.2 Real-time 1D electro-thermal simulation platform

In order to accurately determine the power losses and power semiconductor junction temperatures over standardized driving cycles, a complete EV propulsion system model is required, including a vehicular model, digital controller, power electronics model (with the corresponding loss and 1D thermal models per device) and electric machine model. Details regarding such implementation can be found in [411]. Considering the duration of the driving cycles and the complexity and computational load of such model, conventional simulation procedures become almost infeasible. However, the usage of high performance real-time digital simulation can overcome such problems.

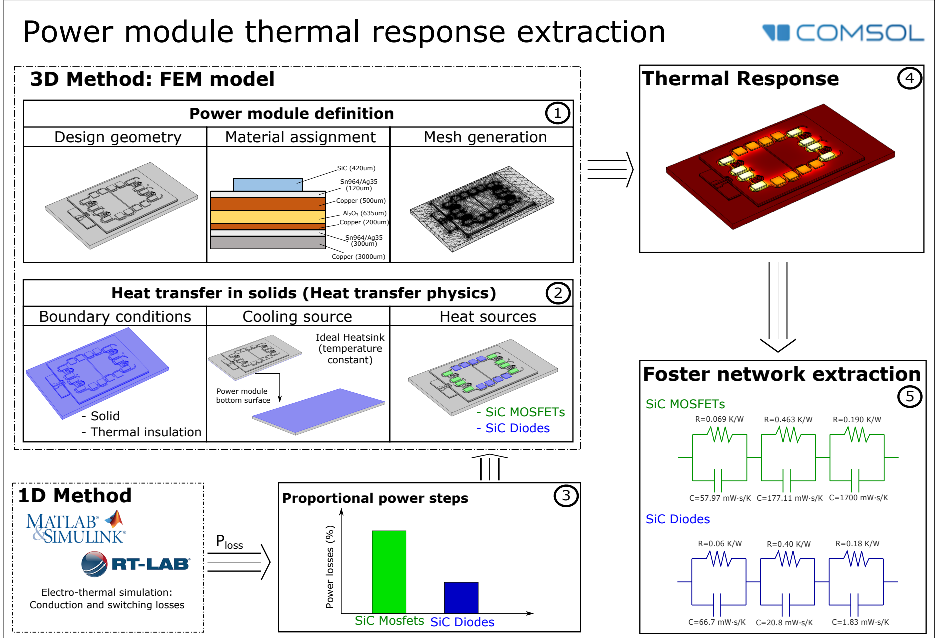
In this work, an RT-Lab OP4510 digital real-time simulation platform [412] consisting on four CPUs (3.5 GHz) and a Xilinx Kintex7 FPGA has been used to conduct the real-time simulations. The elements that constitute the model have been distributed as shown in figure B.2(a) between the computational nodes available in the OP4510 device. The vehicular digital controller (figure B.2(a)-①) and 1D thermal and loss models (including temperature dependency) have the slowest time-constants (figure B.2(a)-②); thus, such models have been distributed between the two available CPUs for their computation in parallel. On the other hand, the power converter and the electric machine models with short simulation step requirements have been implemented in the FPGA ((figure B.2(a)-③)) using the eHS solver [413]. In this way, real-time execution has been guaranteed, greatly reducing the time required to perform such simulations.

B.3 Equivalent RC network extraction procedure

The equivalent thermal network extraction is capital to obtain accurate results. This requires a number of steps, as shown in figure B.2(b). As a starting point, the power module must be represented in 3D (figure B.2(b)-①), implementing the



(a) General diagram of the 1D RT EV propulsion system model based on FPGA and CPU co-simulation.



(b) General diagram of the 3D FEM simulation work-flow for thermal network extraction.

Figure B.2: General diagrams of the 1D RT and 3D FEM simulations.

layout geometry, the layer material assignment (taking into account the surface contact characteristics) and the mesh generation (determining the number of elements) [398]. Additionally, the input signals for the characterization must be defined, so that boundary conditions, cooling and heat sources have to be implemented (figure B.2(b)-②). After that, the preliminary weighted power dissipation steps obtained by real-time simulation (figure B.2(b)-③) must be applied over the heat sources, and the transient responses (figure B.2(b)-④) must be analysed to extract the equivalent 1D Foster networks (figure B.2(b)-⑤). In this context, the power device time-dependant thermal impedance $Z_{j-c}(t)$ can be expressed by a finite sum of exponential terms [414]:

$$Z_{j-c}(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}}\right), \tag{B.1}$$

where R_i and τ_i are the thermal resistance and the time constant of the i-th stage of the thermal network. The time constant is given by $\tau_i = R_i \cdot C_i$, where C_i is the thermal capacitance of the i-th stage. Typically, the thermal impedance can be well fitted considering an equivalent thermal network composed by 3 to 5 stages [415].

The Foster network R_i and C_i couples can be evaluated by using a variety of methods, such as the perturb and observe approach combined with a least square minimization [416], the Levenberg-Marquardt nonlinear fit-routine [417], the identification by deconvolution [414], and the particle swarm optimization [418]. However, in this particular case, the procedure described in [419] and depicted in figure B.3 has been selected, where the degrees of freedom are reduced by choosing a logarithmically-spaced set of time constants (τ_i) in a reasonable interval. The procedure can be automated with a Matlab or Python script in order to reduce the computational load. The steps of the recursive procedure are the following:

1. Set as input data the simulated (or measured) time dependant thermal impedance between the points of interest and the reference temperature, applying a power step to the module devices.

2. Choose a number (e.g. 10 or more) of logarithmically spaced time constants τ between a very small instant (e.g. 1 ps or 1 ns) and an instant when the transient can be considered terminated (steady state reached).

3. Set positive reasonable values (e.g. values whose sum gives a fitting steady state temperature near the one obtained by simulations) of R_i as a starting point for the next optimization step.

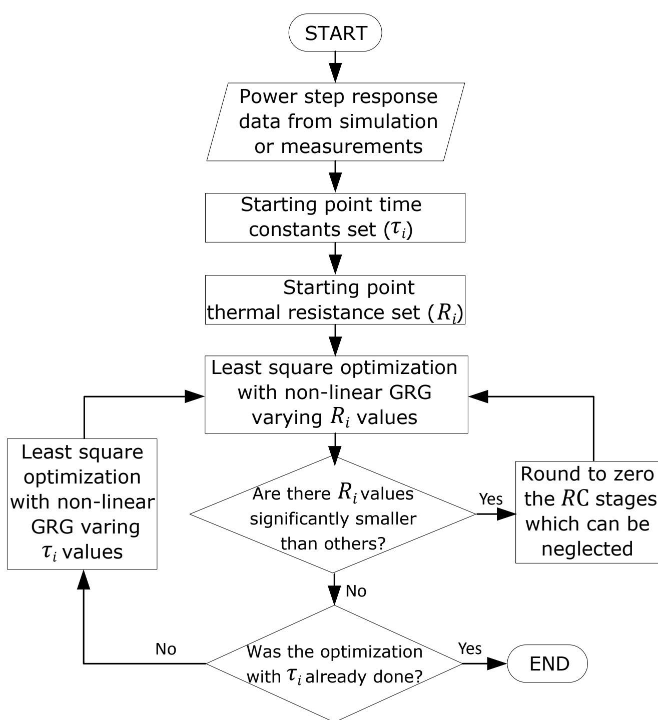


Figure B.3: Flowchart of the procedure applied to extract the Foster networks.

4. Use the R_i set as variable for a least square minimization using the Generalized Reduced Gradient (GRG) method [420] in a non-linear optimization tool (e.g. in Matlab).

5. Decimate the time constants, erasing those with the smaller thermal resistances obtained at step 3. At this step, the non-zero time constants, which do not change significantly the sum of squared residuals (obtained as result of optimization step), are neglected.

6. Introduce the decimated τ_i set as variable for a least square minimization using the GRG method in a non-linear optimization tool.

7. Run step 4 again.

Once the most relevant aspects of the proposed methodology have been presented, its application is provided over the two power module proposals in the chapter 7, where these two *SiC* half-bridges (*symmetric* and *cell* design) are electro-thermally simulated following this methodology proposal, specifically in the section 7.3.

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