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Interleaving Modulation Schemes in Asymmetrical Dual Three-Phase Machines for the DC-Link Stress Reduction

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Abstract: The DC-Link capacitor plays a crucial role as far as power density and reliability are concerned: it occupies approximately 40% of the inverter, and causes approximately 30% of its failures. Asymmetrical dual three-phase (ADTP) multiphase arrangements are gaining relevance in the automotive sector for powertrain applications. This work focuses on reducing the impact that the widely used double zero sequence injection (DZSI) family of PWM techniques have on such a bulky and failure-prone component in an ADTP arrangement by means of interleaving techniques. By using the double Fourier integral formalism, the input current spectra and the overall performance of these PWM techniques have been derived, in terms of current rms value and voltage ripple in the DC-Link capacitor. Simulations have shown that choosing an adequate interleaving scheme and angle considerably relieves both current and voltage stresses on the DC-Link capacitor compared to noninterleaved operation. Reductions of 84% current rms and 86% voltage ripple have been achieved at static operating points. Finally, by averaging the rms current over WLTP standard driving cycle, reductions up to 26% have been obtained under more realistic conditions. All this would enhance the reliability and reduce the size of the onboard capacitors in future electric vehicles.

Keywords: multiphase; interleaving; asymmetrical dual three-phase; double zero-sequence injection (DZSI) PWM; DC-Link capacitor; DC-Link current spectrum

Citation: DeMarcos, A.; Robles, E.; Ugalde, U.; Martinez de Alegria, I.; Andreu, J. Interleaving Modulation Schemes in Asymmetrical Dual Three-Phase Machines for the DC-Link Stress Reduction. *Machines* **2023**, *11*, 267. https://doi.org/10.3390/machines11020267

Academic Editor: Krzysztof Pienkowski

Received: 13 January 2023
Revised: 1 February 2023
Accepted: 7 February 2023
Published: 10 February 2023

1. Introduction

The electric vehicle (EV) powertrain is experimenting a huge change. WBG semiconductors, motors without dependence on rare earth materials and new converter architectures are being introduced. Automotive manufacturers and international programs such as Horizon Europe, USCAR, DOE, and UN ESCAP are focusing on improving specific power (kW/kg), power density (kW/ℓ), efficiency (%), and cost ($/kW) [1]. In this context, multiphase propulsion systems provide several advantages at an affordable cost compared with classic three-phase electric motor-driven systems. Such benefits include power splitting between phases (lower currents and power losses for the same rated output power), reduction of the torque ripple (enhanced efficiency), torque density improvement using harmonic current injection (in concentrated winding machines), lower DC-Link current ripples (smaller DC-Link capacitor), and intrinsic fault-tolerant operation [2–5].

In order to benefit from the abovementioned advantages of multiphase systems, the recent scientific literature shows that the dual three-phase topology (Figure 1) is probably the most widespread multiphase solution [6–10]. Although odd phase number multiphase star-connected arrangements offer a better relationship between the degrees of freedom and the phase number and semiconductor device number, they have lower fault tolerance regarding short circuit and power supply faults (when dual three-phase arrangements are supplied independently) and their modulation scheme is more complex [11]. Therefore, multiple three-phase winding machines are preferred. Theoretically, any number of three-phase winding sets can constitute this kind of electric machine; the most common is to

find dual three-phase arrangements with two isolated neutral points known as "dual three-phase" [12]. These configurations are the most interesting because (i) they represent a good tradeoff between performance and complexity; (ii) easy migration from three-phase technologies is possible because multiple generic and modular three-phase inverters can feed the two three-phase winding sets independently [13]; and (iii) they have very good performance in terms of fault tolerance (open and short circuit faults as well as on the DC power supply) [6,7,14,15]. Generally, 0°, 30°, and 60° are the preferred angle displacements between the two sets. However, the 30° type, which is commonly called asymmetrical six-phase or asymmetrical dual three-phase (ADTP) machine (Figure 1), provides higher torque density and lower torque ripple than the others [16] because it eliminates the sixth torque harmonic pulsation through the synchronization of the two winding sets [17,18].

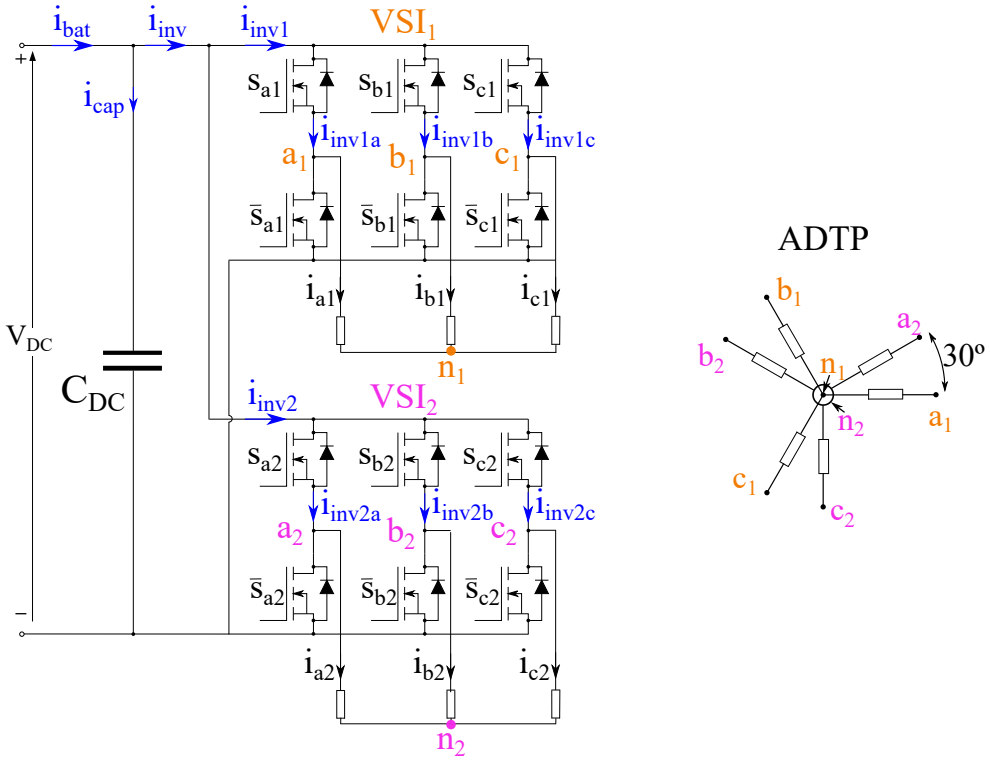
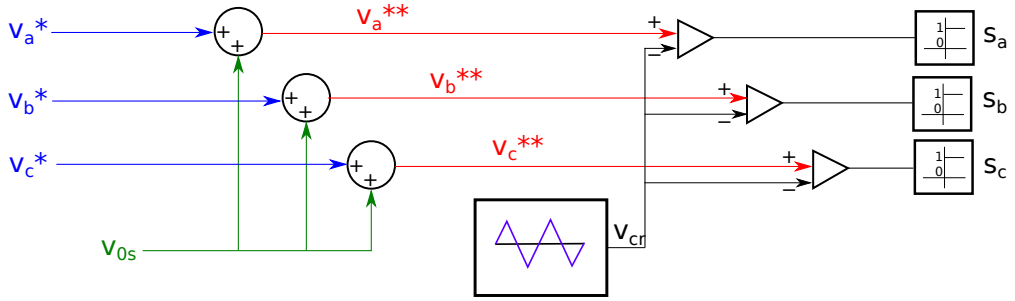
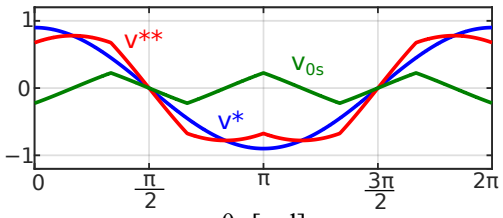


Figure 1. Asymmetric dual three-phase electric machine with two parallel three-phase VSIs.

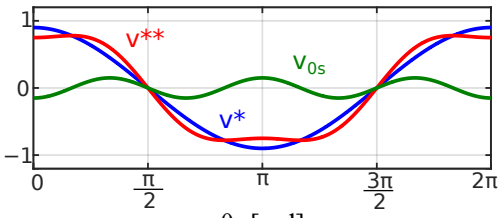
Thus, ADTP-specific voltage-source inverters (VSIs) have been developed, which show great potential in safety-critical applications, and when high power density is needed, such as in electric vehicle (EV) drivetrains [19]. These VSIs (Figure 1) can be controlled by using either appropriate space vector (SV) [20–24] or carrier-based (CB) [25–30] PWM techniques. There is a wide variety of SV-PWM techniques for the ADTP topology; some of them utilize two large adjacent active vectors to synthesize the reference voltage vector [20], and others use four large active vectors [20,21], three large active vectors plus one medium active vector [22], or two large and two medium active vectors [23]. In contrast, CB-PWM strategies are usually treated as a dual three-phase structure (VSI_1 and VSI_2, Figure 1), instead of a six-phase system. This implies an advantage over the SV-based approach because conventional CB-PWM techniques can be exploited. Figure 2 shows how these three-phase CB-PWM techniques are implemented, where $v^* = M\cos(\theta_1)$ is the modulating signal, v_{0s} is the injected zero-sequence component, $v^{**} = v^* + v_{0s}$ is the modified modulating signal, θ_1 is the modulating signal's angular position and the modulation index (M) is defined as $M = \hat{V}_1/(0.5 \cdot V_{DC})$ [31], where $\hat{V}_1$ is the peak phase-neutral voltage and V_{DC} is the DC-Link voltage (Figure 1).



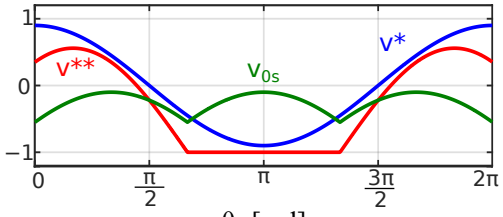
(**a**) CB-PWM block diagram.



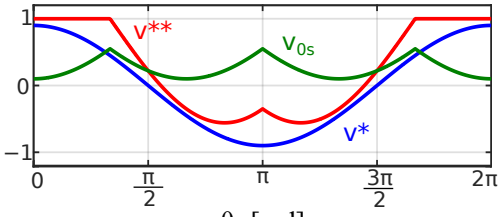
(**b**) MINMAX-PWM.



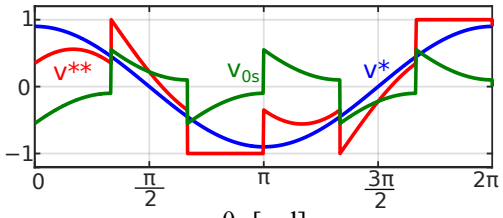
(**c**) THI-PWM.



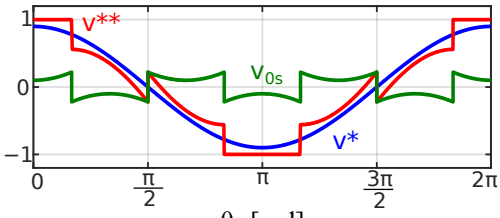
(**d**) D-PWMMIN.



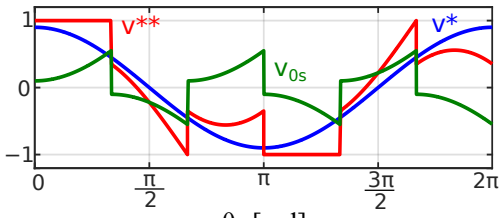
(**e**) D-PWMMAX.



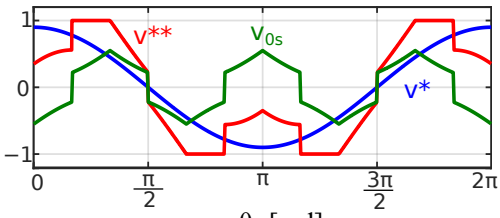
(**f**) D-PWM0.



(**g**) D-PWM1.



(**h**) D-PWM2.



(**i**) D-PWM3.

Figure 2. CB-PWM block diagram as well as their voltage references and zero sequence signals.

CB-PWM techniques applied in a "split" six-phase inverter are commonly known as double zero-sequence injection (DZSI) PWM techniques because this implies injecting one zero-sequence component (v_{0s}) into each three-phase structure [25]. They can be classified into continuous and discontinuous modulation techniques [31]. Sinusoidal PWM (SPWM, as the zero sequence signal which is injected in SPWM is 0, sometimes it is not considered

as DZSI-PWM technique), third harmonic injection PWM (THI-PWM) and min-max PWM method (MINMAX-PWM, sometimes also called symmetrical SV-PWM) are known as continuous modulations (C-PWM), in which all the inverter branches switch continuously. D-PWMMIN, D-PWMMAX, D-PWM0, D-PWM1, D-PWM2, and D-PWM3 are known as discontinuous PWM (D-PWM) techniques, in which one branch does not switch over a whole switching period (while the modulating signal is clamped to ± 1, Figure 2). Thus, the switching power losses in the semiconductors of the VSI are reduced for discontinuous PWM techniques because only two out of the three branches are actually switching and the average equivalent switching frequency is reduced to $^2/_3 f_{sw}$. Finally, all these carrier-based PWM techniques allow a maximum modulation index $M_{max} = 1.15$ working in the linear region except for SPWM technique in which $M_{max} = 1$.

At hardware level, the DC-Link capacitor (C_{DC}, Figure 1) is a crucial element of the VSI. This capacitor is responsible for reducing the low-frequency voltage ripple at the input of the converter, in both steady and transient states, as well as storing the necessary energy to allow an instantaneous power balance between the converter input and output. It must provide a low impedance path for high-frequency currents in order to decouple and reduce the current ripple from the battery. More importantly, in traction applications, the DC-Link capacitor is a bulky and expensive component because it amounts to up to 40% of the total volume of the VSI [32–35]. In addition, DC-Link capacitors are also considered to be one of the most critical elements in power electronics because they cause 30% of the total failures in power electronic inverters [36–38]. For this reason, the reliability of these reactive components has been discussed deeply during the last several years [39–42].

The selection of the DC-Link capacitor (technology, capacitance, size, weight, cost, etc.) is highly dependent on the DC voltage rating of the application where they are integrated [40]. To date, light EV batteries ranged from 250 to 450 V [43], whereas for heavy vehicles the rated voltage is about 800 V. In this context, a trend change is taking place in which electric mobility manufacturers are committed to offering more solutions for these 800-V systems, because this permits the utilization of lighter wiring [44] and also produces smaller on-state power losses, higher efficiency and power density motors, and faster charge of the battery pack [45]. At higher DC voltages, the capacitance of C_{DC} decreases for the same size or encapsulation [46], and its lifetime is significantly reduced. For example, AVX automotive film capacitors of the FHC1 series has a lifetime of an order of magnitude of 10,000 h at 400 V, whereas at 900 V the lifetime drops to approximately 1000 h [46].

In addition to the DC voltage rating, there are other important specifications to select an appropriate DC-Link capacitor: voltage ripple, which is inversely proportional to the capacitance and the size of the DC-Link capacitor [47,48], and current ripple [32,34,49]. Any voltage ripple on the DC-Link produces an additional current ripple on the phase currents, which worsens torque ripple in the electric machine. In this context, there is often a specification for the maximum allowable voltage ripple on the DC-Link (typically ranging from 5–10%).

The current ripple is conditioned by the maximum hot-spot temperature of the DC-Link capacitor. This internal temperature depends on the power losses due to the equivalent series resistance (ESR) and is inversely proportional to the lifetime of the component. Thus, manufacturers typically specify the maximum rms ripple current rating at an ambient temperature and a specific frequency.

Because the DC-Link capacitor is a critical component, significant efforts are being made to enhance its performance. Some works propose to minimize the DC-Link capacitor's current stress by the synchronization of parallel-interleaved single-phase inverters [50,51] and three-phase inverters [52–59]. In ADTP machines, constant interleaving angles can be used to reduce the DC-Link capacitor current for the MINMAX-PWM and some discontinuous PWM techniques [49,60–62]. Ref. [63] proposes a dynamic interleaving method to reduce the DC-Link current ripple, which is only applicable to discontinuous PWM techniques.

However, it is not common to find research works that analyse in-depth the effect of the interleaving angle on the input harmonic cancellation and the rms current minimization of the ADTP arrangement. Furthermore, the few existing contributions usually focus on one or two specific PWM techniques, which makes it hard to compare and quantify the performance of the various DZSI-PWM techniques. As a result, identifying the best interleaving angle for each DZSI-PWM technique applied in an ADTP arrangement is also missing in the scientific literature.

This paper focuses on reducing the current and voltage stress in the DC-Link capacitor by using a multiphase VSI and DZSI-PWM techniques suitable for ADTP arrangement. Different aspects are discussed throughout the paper. In Section 2, DC-Link current spectra are analysed by using the double Fourier integral method for DZSI-PWM techniques in ADTP converters, which are directly related to the main voltage and current stress variables (rms current and peak-to-peak voltage ripple) for the DC-Link capacitor. The figure-of-merit considered in the scientific literature is the output current quality, which is directly related to the total harmonic distortion (THD) or the flux harmonic distortion factor (HDF). However, this ignores how the modulation technique affects the converter input. Thus, Section 3 mathematically analyses and simulates the effect of the DZSI-PWM techniques on the input current spectrum and how it affects the DC-Link capacitor in an ADTP arrangement. Due to the need to reduce the rms value of the DC-Link capacitor current, Section 4 expresses different interleaving schemes and how the relationship between the input current harmonic spectrum and the constant interleaving can be exploited in order to cancel certain dominant harmonics. Next, in order to display the importance of using this type of interleaving techniques, Section 5 shows both the rms current and the peak-to-peak voltage of the DC-Link capacitor applying the optimal interleaving scheme for each DZSI-PWM technique. Finally, Section 6 draws the corresponding conclusions, emphasizing that the performance of the DC-Link capacitor can be significantly improved by applying a suitable interleaving scheme.

2. DC-Link Capacitor Current and Voltage Stress in Asymmetrical Dual Three-Phase Inverters

Voltage ripple and DC-Link capacitor current (i_{cap}, Figure 1) rms value play a crucial role in the selection of an appropriate DC-Link capacitor. The current in the ADTP inverter determines the capacitor current. Figure 3 shows the detailed flow chart followed in this work in order to obtain the harmonic spectrum of the DC-Link capacitor for the described ADTP system. Here, two parallel procedures have been implemented: (i) in Matlab executing the corresponding code for the mathematical equations synthesized in this section; and (ii) in Matlab–Simulink by using a higher-level block environment. The current harmonic spectra obtained from both procedures have been compared to each other in order to check the result matching. In the next lines, the harmonic spectrum of the ADTP inverter is studied in detail.

2.1. Current Spectrum Theoretical Basics for an ADTP Inverter

2.1.1. Input Current of One Branch of VSI_1 (i_{inv1a})

The double Fourier integral formulation characterizes a double periodic function in the frequency domain [64]. Such is the case of a generic analog PWM waveform $g[x(t), y(t)]$, where $x(t) = 2\pi f_{sw} t$ and $y(t) = 2\pi f_1 t = \theta_1$ are two time variables, with f_{sw} the carrier frequency and $f_1 < f_{sw}$ the fundamental frequency.

Thus, according to that formulation,

$$g(x,y) = \underbrace{\frac{A_{00}}{2}}_{\text{DC offset}} + \sum_{n=1}^{\infty} \underbrace{\left[A_{0n}\cos ny + B_{0n}\sin ny\right]}_{\text{Fundamental, and Baseband Harmonics}} + \sum_{m=1}^{\infty} \underbrace{\left[A_{m0}\cos mx + B_{m0}\sin mx\right]}_{\text{Carrier Harmonics}} + \sum_{\substack{n=-\infty \\ \text{but } n\neq 0}}^{\infty} \sum_{m=1}^{\infty} \underbrace{\left[A_{mn}\cos(mx+ny) + B_{mn}\sin(mx+ny)\right]}_{\text{Sideband Harmonics}}, \tag{1}$$

where

$$A_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi}\int_{-\pi}^{\pi} g(x,y)\ \cos(mx+ny)\ dx\,dy, \tag{2}$$

$$B_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi}\int_{-\pi}^{\pi} g(x,y)\ \sin(mx+ny)\ dx\,dy, \tag{3}$$

or, in complex form,

$$C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi}\int_{-\pi}^{\pi} g(x,y)\, e^{j(mx+ny)}\ dx\,dy. \tag{4}$$

Thus, $|C_{mn}| = \sqrt{A_{mn}^2 + B_{mn}^2}$ represents the spectral magnitude of each harmonic, which arises at frequency values equalling $f_h = m\,f_{sw} + n\,f_1$, where m is the carrier index variable and n is the baseband index variable.

Figures 2 and 4 show how the voltage patterns of a PWM-driven inverter are synthesized as a function of the reference and carrier voltages, i.e., $v^{**}$and v_{cr}, respectively. As is usual [65,66], let us assume that $f_{sw} \gg f_1$; therefore, the phase currents are sinusoidal, with amplitude $\hat{I}_{out}$ and phase lag ϕ without any high-frequency ripple current, so

$$i_{a1} = \hat{I}_{out}\cos(2\pi f_1 t - \phi) = \hat{I}_{out}\cos(y-\phi); \tag{5}$$

then, because i_{inv1a} results from the sampling of i_{a1} by following the same voltage PWM pattern, Equations (1)–(4) can be applied with

$$g(x,y) = \begin{cases} 0 & \text{when } v^{**} \le v_{cr}, \\ \hat{I}_{out}\cos(y-\phi) & \text{when } v^{**} > v_{cr}. \end{cases} \tag{6}$$

As Figure 4 shows, the limits of the inner integral for the rising and falling portions of $g(x,y)$ equal $x_r = -\frac{\pi}{2}[1+v^{**}(y)]$ and $x_f = \frac{\pi}{2}[1+v^{**}(y)]$. Therefore, from (1)–(4) the harmonic coefficients of i_{inv1a} result [65,66] in

$$C_{mn}^{inv1a} = \frac{\hat{I}_{out}}{2\pi^2} \int_0^{2\pi} \left(\int_{-[1+v^{**}(y)]\frac{\pi}{2}}^{[1+v^{**}(y)]\frac{\pi}{2}} \cos(y-\phi)\cdot e^{j(mx+ny)} dx \right) dy. \tag{7}$$

Thus, Equation (7) quantifies the spectrum of the current i_{inv1a}, emphasizing its dependance on the PWM technique and modulation index M through the limits of the inner integral $v^{**}(y)$ as well as on the phase lag ϕ.

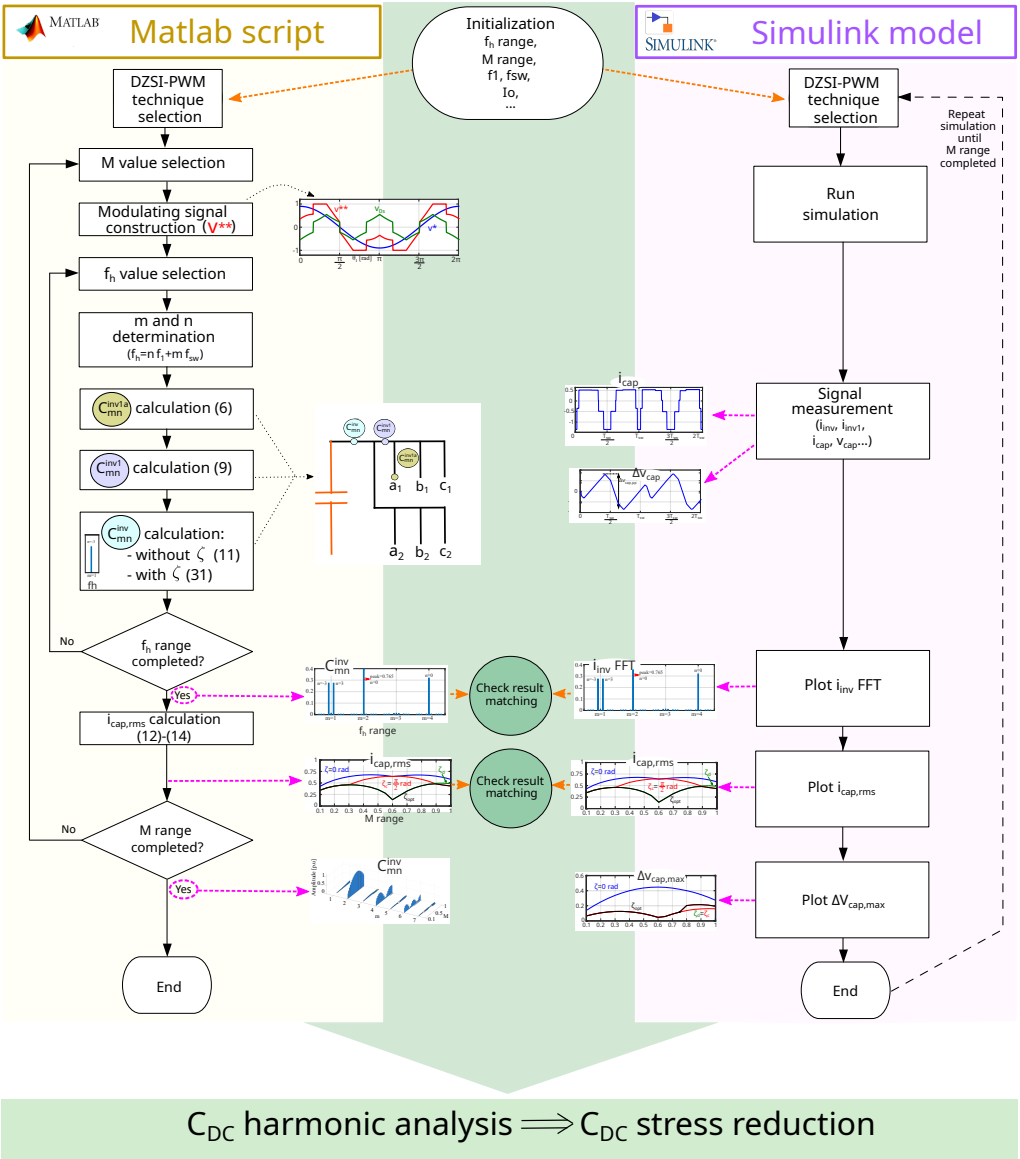


Figure 3. C_{DC} harmonic analysis and rms calculation flow chart.

2.1.2. Input Current of VSI_1 (i_{inv1})

The Fourier coefficients for the consecutive branches *'1b'* and *'1c'* ($C_{mn}^{i_{inv1b}}$ and $C_{mn}^{i_{inv1c}}$) of the VSI_1 (Figure 1) can be obtained by taking (7) and replacing ny with $n(y+\frac{2\pi}{3})$ and $n(y+\frac{4\pi}{3})$, respectively (the current pulses of this branches are phase shifted $2\pi/3$ rad $4\pi/3$ rad concerning the branch *'1a'*). Likewise, it can be phase shifted $C_{mn}^{i_{inv1a}}$ as

$$C_{mn}^{i_{inv1b}} = C_{mn}^{i_{inv1a}} \cdot e^{jn\frac{2\pi}{3}}, \tag{8}$$

$$C_{mn}^{i_{inv1c}} = C_{mn}^{i_{inv1a}} \cdot e^{jn\frac{4\pi}{3}}. \tag{9}$$

However, because $i_{inv1} = i_{inv1a} + i_{inv1b} + i_{inv1c}$ (Figure 1),

$$C_{mn}^{i_{inv1}} = C_{mn}^{i_{inv1a}} \cdot \left[1 + e^{jn\frac{2\pi}{3}} + e^{jn\frac{4\pi}{3}}\right] = C_{mn}^{i_{inv1a}} \cdot \left[1 + 2\cos\left(n\frac{2\pi}{3}\right)\right], \tag{10}$$

where, it can be inferred that $C_{mn}^{i_{inv1}} = 0$ for all values of n except for 0 and multiples of 3. This means that at the output phase currents of each three-phase VSI within the ADTP, where the harmonics multiples of 3 times the fundamental cancel each other out, at the

input, the opposite happens. Thus, there only exist high-frequency carrier and sideband triplens harmonics at the converter input because the PWM methods eliminate all the low-order baseband harmonics.

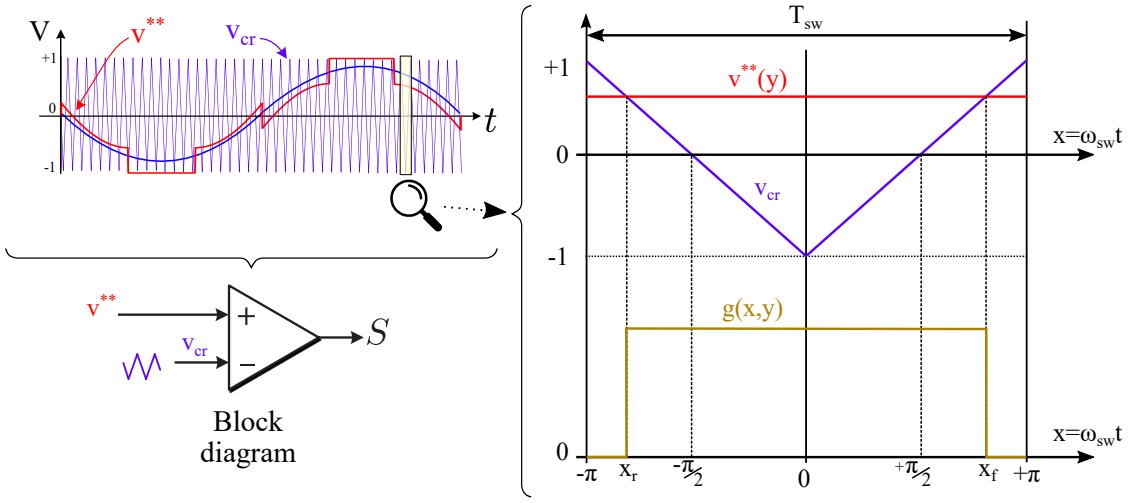


Figure 4. CB-PWM and integration limits of (7).

2.1.3. Input Current of ADTP (i_{inv})

The ADTP is composed of two three-phase stator windings displaced spatially by 30 electrical degrees ($\pi/6$ rad). Usually, each three-phase subsystem has its own isolated neutral point (n_1 and n_2, Figure 1). Thus, following a similar analysis to (10), the Fourier coefficients for the input current harmonics of the second three-phase stator winding ($C_{mn}^{i_{inv2}}$) result in

$$C_{mn}^{i_{inv2}} = C_{mn}^{i_{inv1a}} \cdot \left[1 + 2\cos\left(n\frac{2\pi}{3}\right)\right] \cdot e^{jn\frac{\pi}{6}}, \tag{11}$$

where $e^{jn\frac{\pi}{6}}$ corresponds to the 30° displacement of the second stator winding with respect to the first one. From (10)–(11), the Fourier coefficients of the input current of the ADTP result in

$$C_{mn}^{i_{inv}} = C_{mn}^{i_{inv1a}} \cdot \left[1 + 2\cos\left(n\frac{2\pi}{3}\right)\right] \cdot \left[1 + e^{j\left(n\frac{\pi}{6}\right)}\right]. \tag{12}$$

The difference among the input current harmonics of a three-phase system (10) and an asymmetrical dual three-phase VSI (12) is the $\left[1 + e^{j\left(n\frac{\pi}{6}\right)}\right]$ term, which equals 0 for $n = 6(2k+1)\ \forall k \in \mathbb{Z}$. This leads to the cancellation of some of the existing high-frequency carrier and sideband triplens harmonics at the input of each of the ADTP converter.

2.2. Definition of RMS Current and Voltage Ripple in DC-Link Capacitor

The worst scenario for the DC-Link capacitor is when the whole input current ripple of the ADTP comes from the DC-Link capacitor ($i_{cap} = i_{inv,AC}$) and the battery only supplies the average current of the inverter ($I_{bat} = I_{inv,avg}$) [53,67–70]. Thus, the rms value of the DC-Link current (Figure 1) can be expressed as

$$I_{cap,rms} = \sqrt{I_{inv,rms}^2 - I_{inv,avg}^2}, \tag{13}$$

where the rms value of the input current is

$$I_{inv,rms} = \sqrt{\sum_{n=0}^{\infty}\left(\frac{\left|C_{0n}^{i_{inv}}\right|}{\sqrt{2}}\right)^2 + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left(\frac{\left|C_{mn}^{i_{inv}}\right|}{\sqrt{2}}\right)^2}, \tag{14}$$

and the average value of the input current of the ADTP is

$$I_{inv,avg} = \frac{6}{4} M \hat{I}_{out} \cos\phi. \tag{15}$$

Assuming that at the dominant current harmonic's frequency the capacitor has a predominantly capacitive reactance, the RL impedance can be neglected, so the DC-Link voltage variation can be expressed as

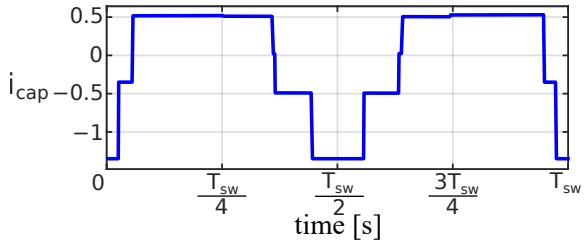
$$\Delta v_{cap}(t) = \frac{1}{C} \int_0^t i_{cap}\, dt = \frac{1}{C} \int_0^t (i_{inv} - I_{inv,avg})\, dt. \tag{16}$$

Considering this, Figure 5a shows the current through the DC-Link capacitor and Figure 5b its voltage ripple according to (16). Applying a normalization factor $\Delta v_{base} = \hat{I}_{out} \cdot T_{sw}/C$ to the voltage ripple of (16), the peak-to-peak value of the voltage ripple in every switching period (T_{sw}) can be obtained by

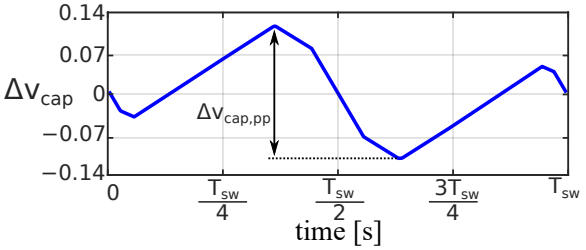
$$\{\Delta v_{cap,pp}\}_{T_{sw}} = max\{\Delta v_{cap}(t)\}_{T_{sw}} - min\{\Delta v_{cap}(t)\}_{T_{sw}}, \tag{17}$$

which makes it possible to determine the maximum value of the switching voltage ripple over T_1 (or $\theta_1 = 2\pi$ rad). Because the input current to the ADTP is repeated every $2\pi/6$ rad (Figure 5c), it is sufficient to perform the analysis during this interval, so

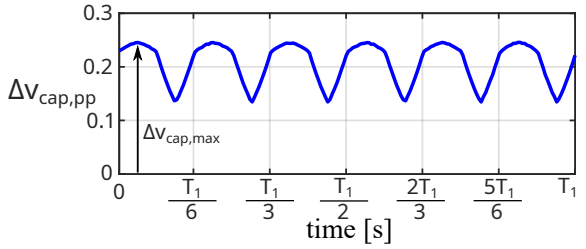
$$\Delta v_{cap,max} = max\{\Delta v_{cap,pp}\}_{2\pi} = max\{\Delta v_{cap,pp}\}_{2\pi/6}. \tag{18}$$



(**a**) Current waveform over two T_{sw}.



(**b**) Voltage waveform over two T_{sw}.



(**c**) Voltage waveform over a T_1.

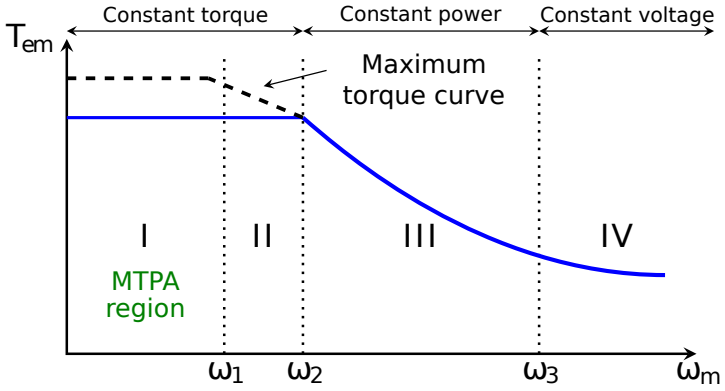
Figure 5. Normalized current and voltage in the DC-Link capacitor with SPWM technique, $M = 0.9$ and $\cos\phi = 1$.

3. Influence of the Modulation Technique on the Input Current Harmonic Spectrum

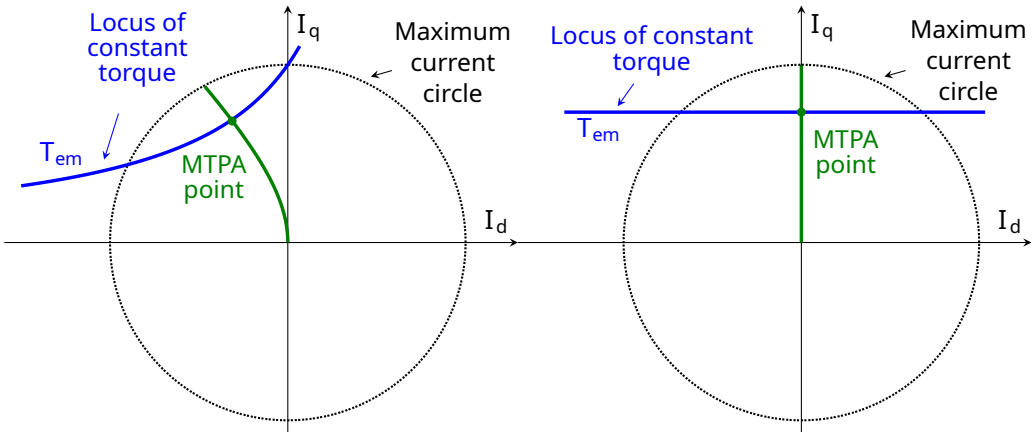
Current harmonics mainly depend on the selected PWM technique, as well as on M, f_h, and $\cos\phi$. Nevertheless, in most cases EV traction machines operate with a unitary $\cos\phi$ [57] (this is demonstrated in Section 3.1). With the objective of simplifying the study, the input current spectra for different PWM techniques are obtained in Sections 3.2 and 3.3 as a function of M, f_h for $\cos\phi = 1$.

3.1. Operating Point in EVs: $\cos\phi$

Permanent magnet synchronous motors (PMSMs) are the most efficient and power-dense type of traction motors [71]. For this reason, this is the prevailing type of electrical machine for automotive traction [72]. Four operating regions are distinguished in this type on machines [73,74]: maximum torque per ampere (MTPA, Figure 6a—region I); field weakening region without and with torque reduction (Figure 6a—regions II and III, respectively); and maximum torque per volt (MTPV, Figure 6a—region IV). As MTPA operation of synchronous motors have become an indispensable part of highly efficient motor drives [75], this work is based in this operation region.



(**a**) Torque vs speed curve and operating regions of PMSMs [73].



(**b**) MTPA point for IPMSMs ($L_d < L_q$). (**c**) MTPA point for SPMSMs ($L_d = L_q$).

Figure 6. Characteristicregions for PMSMs.

The electrical dynamic equations of PMSMs can be represented by using the rotating synchronous reference frame (dq), wherein the permanent magnetic flux is aligned with the d-axis, as

$$v_d(t) = R_s i_d(t) + L_d \frac{di_d(t)}{dt} - \omega_e(t) L_q i_q(t), \tag{19a}$$

$$v_q(t) = R_s i_q(t) + L_q \frac{di_q(t)}{dt} + \omega_e(t)[L_d i_d(t) + \Psi_{PM}], \tag{19b}$$

where v_d and v_q are the dq-axis time-dependent stator voltages, i_d and i_q are dq-axis time-dependent currents, L_d and L_q are the dq-axis inductances, R_s is the stator resistance, Ψ_{PM} is the permanent-magnet flux linkage, and $\omega_e(t) = N_p \omega_m(t)$ is the time-dependent electrical speed of the machine where $\omega_m(t)$ is the time-dependent mechanical speed and N_p is the number of pole pairs.

At steady-state conditions, (19a) and (19b) can be simplified as

$$V_d = R_s I_d - \omega_e L_q I_q, \tag{20a}$$

$$V_q = R_s I_q + \omega_e L_d I_d + \omega_e \Psi_{PM}; \tag{20b}$$

in addition, the electromagnetic torque at steady-state conditions is expressed as

$$T_{em} = 3N_p \left[\Psi_{PM} + \left(L_d - L_q\right) I_d\right] I_q. \tag{21}$$

It should be noted that (20) and (21) are described assuming that $L_d < L_q$, which is typical for interior PMSMs (IPMSMs). For surface-mounted PMSMs (SPMSMs), where $L_d = L_q$, the electromagnetic torque of (21) is only dependent on the q-current and can be simplified as

$$T_{em} = 3N_p \Psi_{PM} I_q. \tag{22}$$

Minimum copper losses and maximum torque per applied current modulus are guaranteed to track this MTPA region, which prevails at low speeds [75,76]. To perform a satisfactory torque control in PMSMs, the maximum torque per ampere (MTPA) point must be found.

The MTPA trajectory for three-phase IPMSMs is described in [76]. Following the same procedure for a six-phase IPMSMs, a fourth-order polynomial can be obtained in terms of I_d

$$I_d^4 + K_3 I_d^3 + K_2 I_d^2 + K_1 I_d + K_0 = 0, \tag{23}$$

where,

$$\begin{aligned} K_0 &= -\frac{T_{em}^2}{9N_p^2(L_d - L_q)^2}, & K_1 &= \frac{\Psi_{PM}^3}{(L_d - L_q)^3}, \\ K_2 &= \frac{3\Psi_{PM}^2}{(L_d - L_q)^2}, & K_3 &= \frac{3\Psi_{PM}}{L_d - L_q}; \end{aligned} \tag{24}$$

solving (23), the d-current corresponding to the MTPA point is obtained, and then the q-current is calculated by using (21).

For SPMSMs, the MTPA point is always defined as $I_d = 0$, and I_q is proportional to the electromagnetic torque; recall (22). Figure 6 depicts the MTPA trajectory for both IPMSMs and SPMSMs.

From the above, $\cos\phi$ can be obtained considering the dq voltage equations of the machine (20) and the dq-currents corresponding to the MTPA curve. $\cos\phi$ is expressed as

$\cos\phi = \cos\phi_v - \cos\phi_i$, where ϕ_v is the angle corresponding to the dq voltages and ϕ_i is the angle corresponding to the dq currents. These angles can be calculated as follows:

$$\phi_v = \arctan(V_q/V_d), \quad \text{for PMSMs,} \tag{25}$$

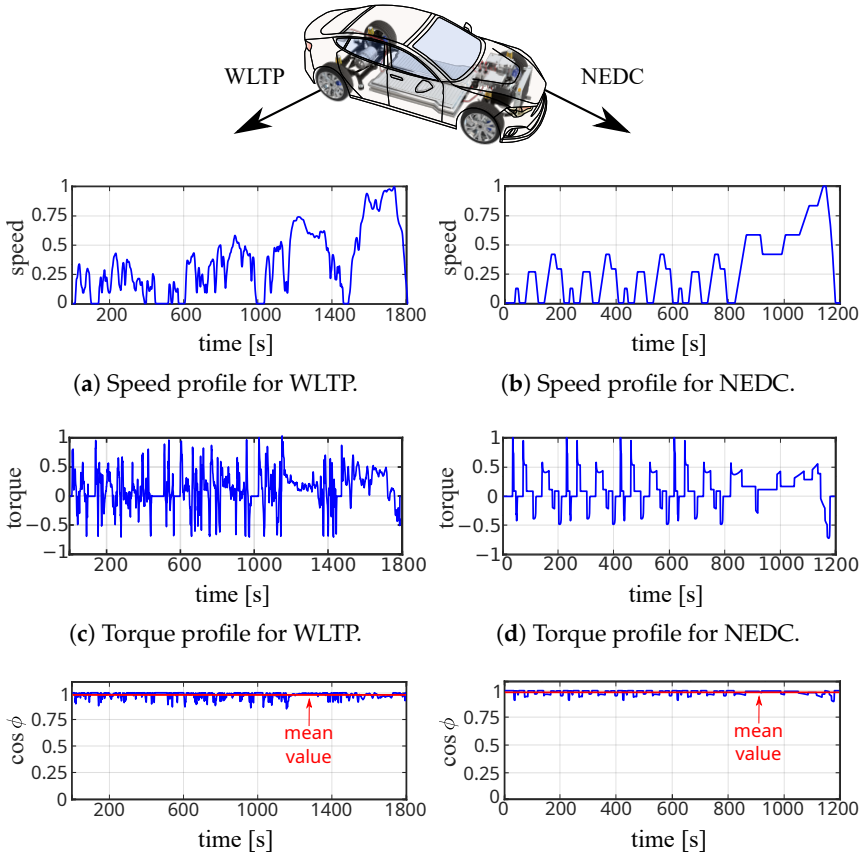
$$\phi_i = \begin{cases} \arctan(I_q/I_d), & \text{for IPMSMs} \\ \pi/2, & \text{for SPMSMs.} \end{cases} \tag{26}$$

To evaluate $\cos\phi$ over standardized driving cycles, an IPMSM has been tested, the parameters of which are listed in Table 1. Figure 7 presents the speed and torque profiles in addition to the $\cos\phi$ values corresponding to the worldwide harmonized light vehicles test procedure (WLTP) Class 3 and the new European driving cycle (NEDC) using this IPMSM. In order to make a fair comparison, torque and speed profiles are scaled according to the maximum and base values of the machine, which are shown in Table 1.

Table 1. Parameters of the dual three-phase IPMSM drive.

Parameter	Value	Parameter	Value
Number of pole pairs (N_p)	19	Stator resistance (R_s)	61.43 [mΩ]
d-axis inductance (L_d)	1.00 [mH]	q-axis inductance (L_q)	1.35 [mH]
PM flux linkage (Ψ_{PM})	0.038 [Wb]	DC bus nominal voltage (V_{DC})	400 [V]
Maximum torque (T_{max})	54 [N·m]	Base mech. speed (ω_b)	3000 [rpm]

As Figure 7 shows, the value of $\cos\phi$ over these standardized driving cycles is close to unity; more precisely, the average of $\cos\phi > 0.97$ over such cycles (Figure 7e,f). Therefore, $\cos\phi = 1$ will be assumed henceforth.



(**a**) Speed profile for WLTP. (**b**) Speed profile for NEDC.

(**c**) Torque profile for WLTP. (**d**) Torque profile for NEDC.

(**e**) $\cos\phi$ values corresponding to WLTP. (**f**) $\cos\phi$ values corresponding to NEDC.

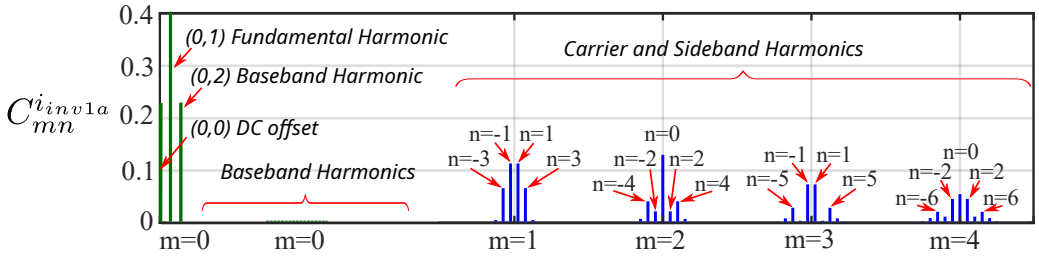
Figure 7. Speed and torque profiles in addition to the $\cos\phi$ values corresponding to WLTP and NEDC driving cycles.

3.2. Input Current Harmonic Analysis for SPWM Technique

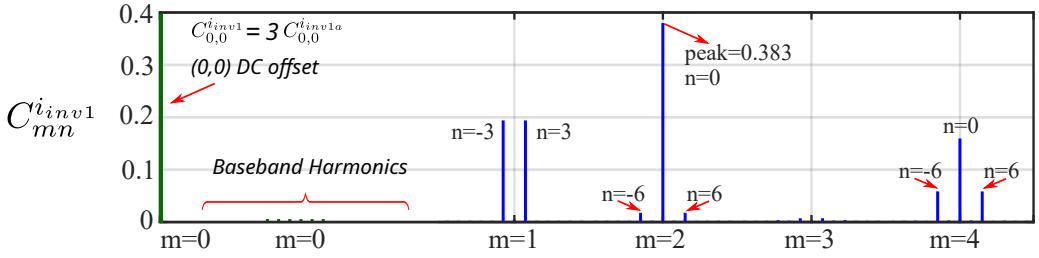
Figure 8 shows the high-frequency input current spectra for the SPWM technique, with $M = 0.9$ and $\cos\phi = 1$. Specifically, Figure 8a depicts the input current of one branch of the inverter (i.e., i_{inv1a}), Figure 8b shows it for the VSI$_1$ (i_{inv1}), and Figure 8c for the whole ADTP inverter (i_{inv}). Applying the SPWM technique (in which $v^{**}(y) = M\cos(y)$) to (7), the input current spectrum of one branch of the inverter (i.e., i_{inv1a}) can be expressed as

$$C_{mn}^{i_{inv1a}} = \frac{\hat{I}_{out}}{m\pi}\cos\left[(m+n)\frac{\pi}{2}\right]\left\{\cos\phi \times \left[J_{n+1}\left(mM\frac{\pi}{2}\right) - J_{n-1}\left(mM\frac{\pi}{2}\right)\right] + j\,\sin\phi \times \left[J_{n+1}\left(mM\frac{\pi}{2}\right) + J_{n-1}\left(mM\frac{\pi}{2}\right)\right]\right\} \quad (27)$$

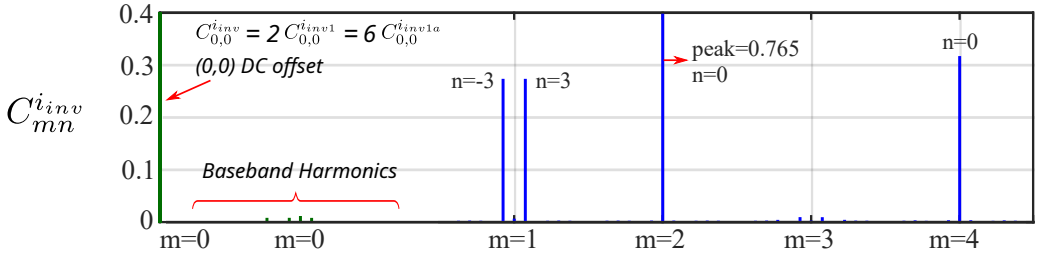
where $J_{n+1}(m\frac{\pi}{2}M)$ and $J_{n-1}(m\frac{\pi}{2}M)$ are the Bessel functions of order $n+1$ and $n-1$ with argument $m\frac{\pi}{2}M$ [77,78].



(**a**) Input current of one branch of VSI$_1$.



(**b**) Input current of VSI$_1$.



(**c**) Input current of the ADTP.

Figure 8. Normalized high-frequency input current spectrum amplitudes for one leg of VSI$_1$, the whole VSI$_1$, and the whole ADTP applying SPWM technique, $M = 0.9$ and $\cos\phi = 1$.

Equation (27) points out that the high-frequency carrier and sideband harmonics that exist in i_{inv1a}, and in turn in i_{inv1} (10) and i_{inv} (12), are those meeting that $m+n$ is an even number (Figure 8). From (10), it is also inferred that the only harmonics that prevail at i_{inv1} are multiples of $3\omega_1$ ($n = 3k\ \forall k \in \mathbb{Z}$) (Figure 8b). In addition, from (12) it is inferred that the $n = 6(2k+1)$ input current harmonics of i_{inv1} disappear from the input current spectrum of i_{inv} (Figure 8c). Regarding the carrier and sideband harmonics, the possible dominant harmonics for SPWM are assumed to exist among the pairs of (m,n) i.e., $(1,-3)$, $(1,3)$, and $(2,0)$.

Inserting (27) into (12), the amplitudes of these harmonic components for i_{inv} result in

$$|i_{inv}(1,-3)| = |i_{inv}(1,3)| = \frac{3\sqrt{2}\hat{I}_{out}}{\pi} \times \left| J_4\left(\frac{\pi}{2}M\right) - J_2\left(\frac{\pi}{2}M\right) \right|, \tag{28}$$

$$|i_{inv1}(2,0)| = \frac{6\hat{I}_{out}}{2\pi} \times |J_1(\pi M)|, \tag{29}$$

because the values of J_2 and J_4 are similar, the amplitudes of $|i_{inv}(1,-3)|$ and $|i_{inv}(1,3)|$ are almost neglectable compared to $|i_{inv}(2,0)|$. Therefore, the dominant harmonic component is $|i_{inv}(2,0)|$, i.e., the second-order switching harmonic, as can be confirmed in Figure 8c.

3.3. Input Current Harmonic Analysis for DZSI-PWM Techniques

The previous Fourier frequency-domain analysis makes it possible to obtain the normalized input current spectra ($i_{inv,norm} = i_{inv}/\hat{I}_{out}$) of the ADTP inverter (Figure 1, i_{inv}) for the DZSI-PWM techniques mentioned in Section 1 in addition to the SPWM technique. The current spectra for the above mentioned CB-PWM techniques have been checked by simulations on Matlab–Simulink R2020b in order to confirm that the previous Fourier double integral analysis (Section 2) is correct. The block diagram of the simulations carried out in Matlab–Simulink is represented in Figure 9. In order to match the results obtained by the analytical study on Matlab following the procedure of Section 2 (previously exposed in Figure 3), the same assumptions have been made: the output phase currents do not have any high-frequency ripple, and the DC-Link capacitor manages the whole ripple of the ADTP inverter current.

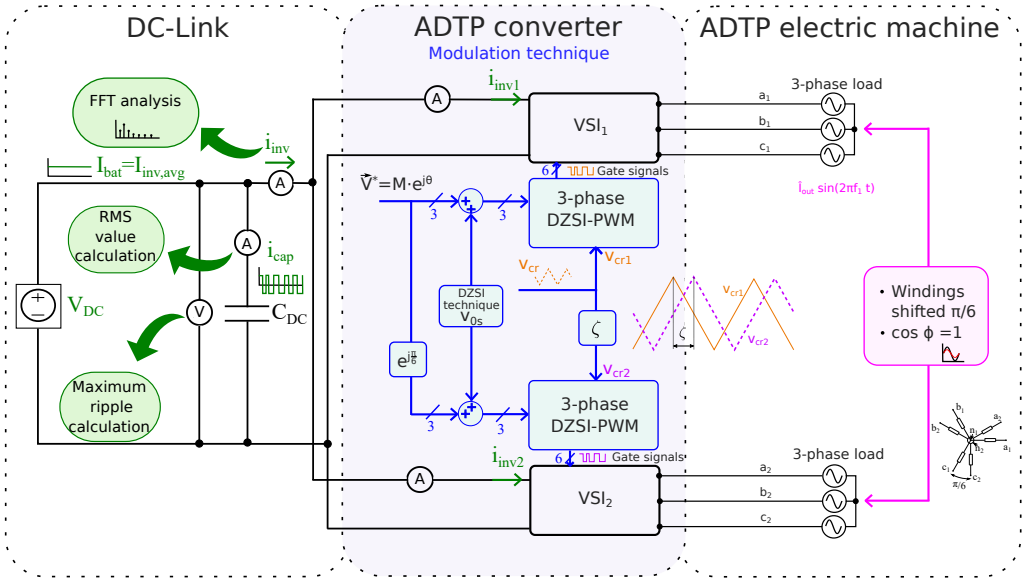


Figure 9. Block diagram of the simulations carried out in Matlab–Simulink for the determination of the input current of the ADTP system.

Figure 10 shows the current spectra of i_{inv} as a function of different vales of M, for the abovementioned CB-PWM techniques.

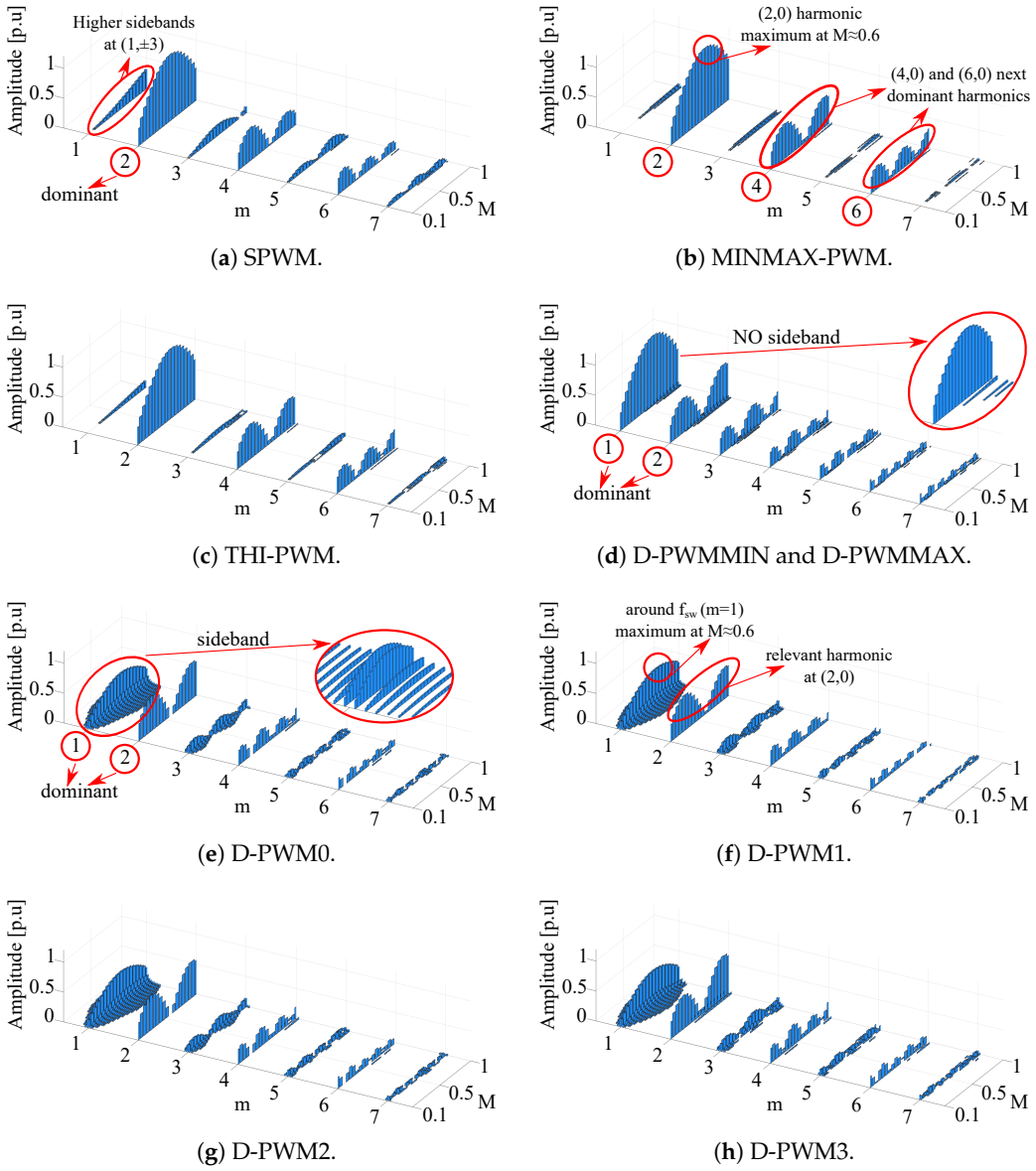
It highlights that for continuous modulations:

- The predominant (m,n) harmonic component is $(2,0)$ which corresponds to $2f_{sw}$. This harmonic component has a maximum at $M \approx 0.6$.
- The next dominant harmonics are situated at $(4,0)$ and $(6,0)$.
- SPWM exhibits higher sideband harmonics at $(1,\pm 3)$ than MINMAX-PWM and THI-PWM, which are quite similar in the full range of frequency and modulation index.

Regarding discontinuous modulations:

- All analysed discontinuous PWM techniques have a significant harmonic component around f_{sw} ($m = 1$). This harmonic component has a maximum at $M \approx 0.6$.
- D-PWM0, D-PWM1, D-PWM2, and D-PWM3 exhibit wide sideband harmonics around $m = 1$, which leads to having harmonic components at lower frequencies, and the harmonics with highest amplitude are placed at $(1, \pm 3)$ and $(2, 0)$.
- D-PWMMAX and D-PWMMIN are equivalent, the sideband harmonics around $m = 1$ are not so relevant, the predominant component lies at $(1, 0)$, and the next important harmonic is placed at $(2, 0)$.
- The relevant harmonic situated at $(2, 0)$ is negligible at $M \approx 0.6$.

The presence of harmonics influences the deterioration of the C_{DC}. Therefore, it is desirable to reduce them as much as possible. For this purpose, the interleaving of the two three-phase inverters which form the ADTP multiphase VSI is detailed in the next section.



(**a**) SPWM. (**b**) MINMAX-PWM.

(**c**) THI-PWM. (**d**) D-PWMMIN and D-PWMMAX.

(**e**) D-PWM0. (**f**) D-PWM1.

(**g**) D-PWM2. (**h**) D-PWM3.

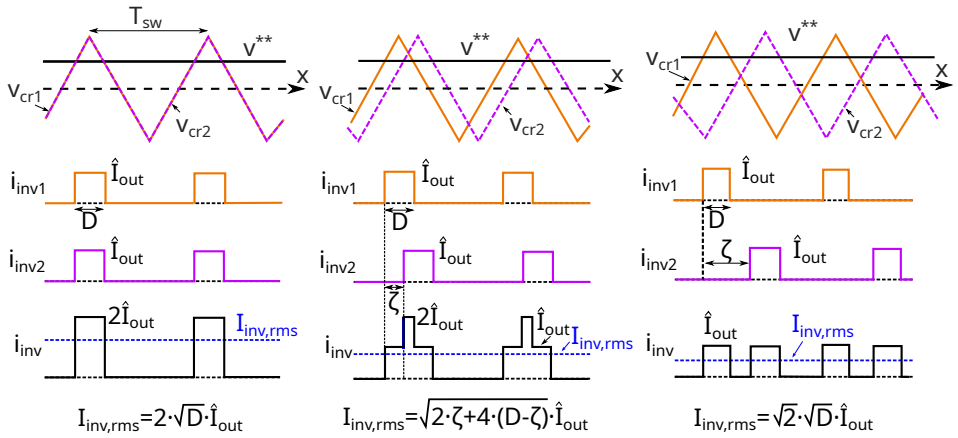
Figure 10. Normalized amplitudes of the high-frequency input current harmonic spectra $\left(|C_{mn}^{i_{inv}}|\right)$ as a function of the value of M for the analysed DZSI-PWM techniques with $\cos\phi = 1$.

4. Interleaving Schemes to Improve the Performance of ADTP Inverters

Published works on ADTP interleaving [49,60–62] do not provide enough insight into the frequency-domain description of the input current. The rms value of rectangu-

lar current pulses depends on the amplitude $\hat{I}_{out}$ and the square root of the duty cycle ($I_{inv1,rms} = \sqrt{D} \cdot \hat{I}_{out}$, Figure 11). When an interleaving angle $\zeta = 0$ rad is applied between two inverters, the current pulses of both VSIs are totally overlapped, and the resulting pulses are doubled in amplitude, which leads to a double rms current value of the interleaved inverter current ($I_{inv,rms} = 2 \cdot \sqrt{D} \cdot \hat{I}_{out}$). As the interleaving angle is increased, the overlap is reduced, and in turn, the rms value of the resulting waveform is reduced. When the interleaving angle between the pulses is large enough for them not to overlap ($\zeta \geq D$), the rms current is minimized ($I_{inv,rms} = \sqrt{2} \cdot \sqrt{D} \cdot \hat{I}_{out}$). This way, a reduction of the rms value is achieved with respect to the previous cases without interleaving (Figure 11).

In order to analyse the concept of interleaving in depth, three different schemes will be introduced: constant interleaving, dynamic interleaving, and optimal interleaving.



(**a**) No interleaving ($\zeta = 0°$). (**b**) Overlapping ($\zeta < D$). (**c**) No overlapping ($\zeta \geq D$).

Figure 11. Interleaving concept on rectangular current pulses.

4.1. Constant Interleaving: ζ_c

The concept of interleaving can be applied to the Fourier double series of the input current of the VSI_2 by adding an additional phase shift with respect to the input current of the VSI_1 (Figure 1). As Figure 11 shows, because $x(t)$ is the variable related to the carrier wave angle, the Fourier coefficients for branch '*a*' of the consecutive inverter '2' ($C_{mn}^{i_{inv2a}}$) can be calculated by taking (7) and replacing mx with $m(x + \zeta_c)$. This can be also represented as

$$C_{mn}^{i_{inv2a}} = C_{mn}^{i_{inv1a}} \cdot e^{jm\zeta_c}, \tag{30}$$

where $e^{jm\zeta_c}$ corresponds to the shifting caused by the interleaving of the second carrier signal (v_{cr2}, in Figure 11).

The introduction of this new parameter affects $C_{mn}^{i_{inv2}}$ of (11) and $C_{mn}^{i_{inv}}$ of (12), leading to

$$C_{mn}^{i_{inv2}} = C_{mn}^{i_{inv1a}} \cdot \left[1 + 2\cos\left(n\frac{2\pi}{3}\right)\right] \cdot e^{jn\frac{\pi}{6}} \cdot e^{jm\zeta_c}, \tag{31}$$

$$C_{mn}^{i_{inv}} = C_{mn}^{i_{inv1a}} \cdot \left[1 + 2\cos\left(n\frac{2\pi}{3}\right)\right] \cdot \left[1 + e^{j\left(n\frac{\pi}{6} + m\zeta_c\right)}\right]. \tag{32}$$

In (32), it can be observed that making the second term in brackets $\left[1 + e^{j\left(n\frac{\pi}{6} + m\zeta_c\right)}\right]$ equal to 0, an interleaving angle ζ_c that cancels some specific input current harmonics ($C_{mn}^{i_{inv}}$, (12)) is obtained:

$$\zeta_c = \frac{(2k+1) \cdot \pi - n\frac{\pi}{6}}{m} \qquad \forall k \in \mathbb{Z}^+. \tag{33}$$

In this sense, and because the dominant harmonic is the most important component when it comes to computing the rms value of the whole current spectrum through the capacitor, the interleaving angle (ζ_c) should eliminate this dominant harmonic. Table 2 summarizes the most significant constant interleaving angles and the harmonic orders cancelled. This table also points out when the most relevant input current harmonics are removed: letting $\zeta_c = \pi/2$ rad erases the $(2,0)$ and $(1,3)$ harmonics, whereas letting $\zeta_c = \pi$ rad erases the $(1,0)$ harmonic.

As a collateral effect, sometimes other harmonics can slightly increase their amplitude. Therefore, the angle which eliminates the dominant input current harmonic and the one which minimizes $I_{cap,rms}$ can be different. For example, Figure 12 shows the input current spectrum for the ADTP with SPWM technique, $M = 0.9$, $\cos\phi = 1$ and two interleaving angles ($\zeta_c = 0$ rad and $\zeta_c = \pi/2$ rad). For this case, it can be observed that the dominant harmonic $(2,0)$ has been cancelled out, but $(1,-3)$ and $(2,\pm 6)$ have increased their amplitude. Therefore, the selection of the interleaving angle has to be made carefully.

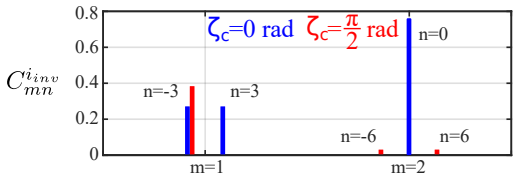


Figure 12. Input current spectrum for the ADTP with SPWM technique, $M = 0.9$, $\cos\phi = 1$ and two interleaving angles.

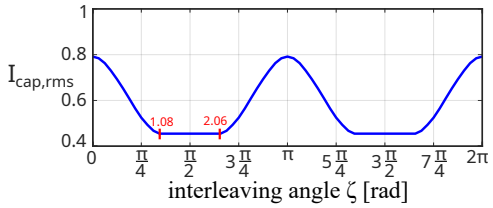
In view of this, numerical calculations have been carried out in Matlab following the procedure explained in Section 2 for each DZSI-PWM technique, by sweeping the modulation index M and the interleaving angle ζ_c. All these calculations show that the $\zeta_c = \pi/2$ rad constant angle minimizes $I_{cap,rms}$ regardless of the value of M for all the analysed DZSI-PWM techniques except for D-PWMMIN and D-PWMMAX, in which $\zeta_c = \pi$ rad is the best choice for any value of M. However, from the numerical analysis carried out, it has been seen that the constant angle applied for the entire period of the fundamental of D-PWMMIN and D-PWMMAX $\zeta_c = \pi$ is the best option only for $M \leqslant 0.75$; and for $M > 0.75$ the interleaving angle which minimizes the $I_{cap,rms}$ is only constant for each fundamental period but not for rest of the linear range. This is explained better in Section 4.3. This analysis coincides with the above performed input harmonic spectra of Figure 10, as well as with the removal of the dominant harmonics observed in Table 2.

Table 2. Eliminated (m,n) harmonics depending on ζ_c according to (33).

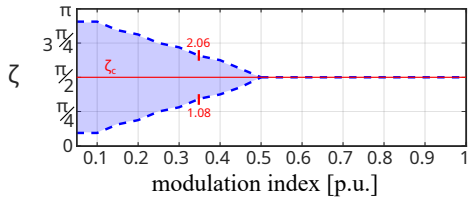
	$k = 0$	$k = 1$	$k = 2$
$\zeta_c = \pi/2$ rad	(2,0)	(6,0)	(10,0)
	(1,3)	(5,3)	(9,3)
	(3,−3)	(7,−3)	(11,−3)
$\zeta_c = \pi$ rad	(1,0)	(3,0)	(5,0)
	(2,6)	(4,6)	(6,6)
	(2,−6)	(4,−6)	(6,−6)

Finally, as an example of this analysis, Figure 13 shows the case of the SPWM technique. Here, note that for $M = 0.35$ (Figure 13a), $I_{cap,rms}$ is at minimum when ζ_c lies between 1.08 and 2.06 rad even though the current spectra is not the same (Figure 13c–e. Performing the same analysis in the whole linear region of M, for $0 \leqslant M < 0.5$, there is not a single ζ_c which minimizes $I_{cap,rms}$ but a range of values (Figure 13b); however, for $0.5 \leqslant M \leqslant 1$

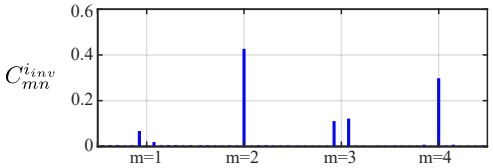
there is just one ζ_c value ($\pi/2$ rad) that is considered the best choice ζ_c in the entire range of M for the SPWM technique.



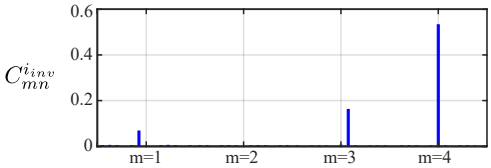
(**a**) Normalized $I_{cap,rms}$ as a function of the interleaving angle ζ for $M = 0.35$.



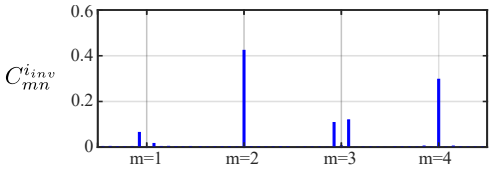
(**b**) Constant interleaving angle ζ_c for the whole linear range.



(**c**) Input current spectrum of the ADTP with $\zeta = 1.08$ rad and $M = 0.35$.



(**d**) Input current spectrum of the ADTP with $\zeta = \pi/2$ rad and $M = 0.35$.



(**e**) Input current spectrum of the ADTP with $\zeta = 2.06$ rad and $M = 0.35$.

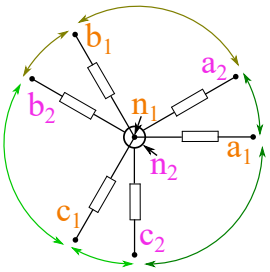
Figure 13. Input current under constant interleaving angle applying the SPWM technique.

4.2. Dynamic Interleaving Scheme for Discontinuous PWM Techniques: ζ_d

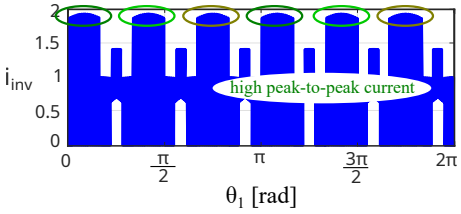
Unlike the constant interleaving scheme discussed above, a dynamic interleaving algorithm ζ_d applicable only for discontinuous PWM has been recently proposed in [63] to reduce the DC-Link current ripple of the ADTP. In this case, the interleaving angle of the proposed method is not constant. In some subintervals of the fundamental period cycle, ζ is set to π rad whereas the rest of the time it is 0 rad.

In any discontinuous PWM technique, the peak-to-peak value of the input current of the VSI without any interleaving rises significantly when any two nearby phases (Figure 14a) in the phasor diagram are clamped to ± 1. As an example, Figure 14 shows the operation basics of ζ_d for D-PWM1 and D-PWMMIN. Figure 14b,c show the input current of the VSI without interleaving ($\zeta = 0$ rad) for these discontinuous PWM techniques and Figure 14d,e their respective voltage references of the ADTP.

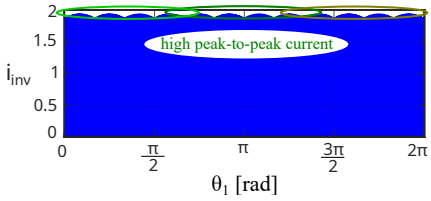
In the case of D-PWMMIN, two nearby phases in the phasor diagram are continuously clamped to ± 1 (Figure 14e). This leads to a continuous activation of the dynamic interleaving algorithm (Figure 14g, ζ_d in blue). This means that for this specific PWM technique, the dynamic interleaving scheme is exactly the same as applying a constant angle of $\zeta_c = \pi$ rad. The effect of applying this angle can be visualized in Figure 14f,g for D-PWM1 and D-PWMMIN, respectively. The peak-to-peak values of the input currents are reduced significantly comparing to the $\zeta = 0$ rad scenario of Figure 14b,c. The techniques D-PWM0, D-PWM2 and D-PWM3 follow the same pattern as D-PWM1, whereas D-PWMMAX behaves as D-PWMMIN in terms of full-time clamping. Therefore, for both D-PWMMIN and D-PWMMAX, applying the dynamic interleaving scheme would be exactly like applying the scheme $\zeta_c = \pi$ rad explained in the previous subsection.



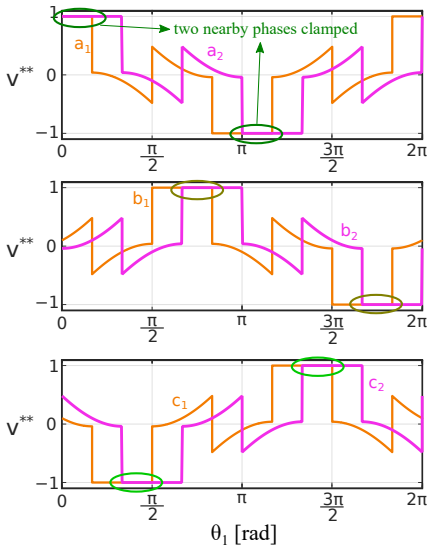
(**a**) ADTP phasor diagram.



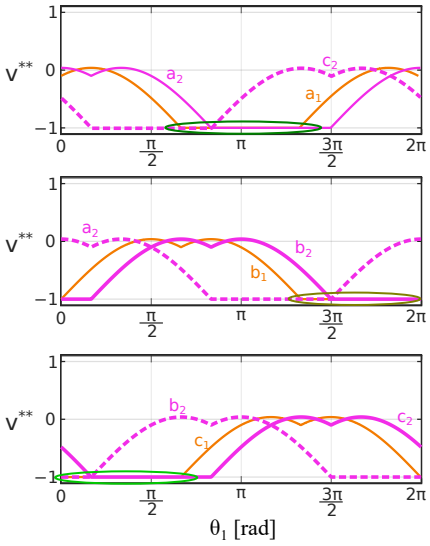
(**b**) Input current of the VSI without interleaving ($\zeta = 0$ rad) for D-PWM1.



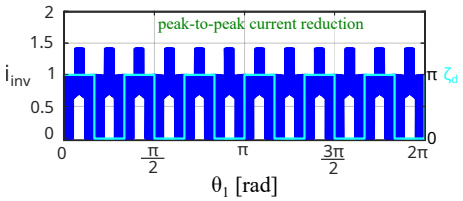
(**c**) Input current of the VSI without interleaving ($\zeta = 0$ rad) for D-PWMMIN.



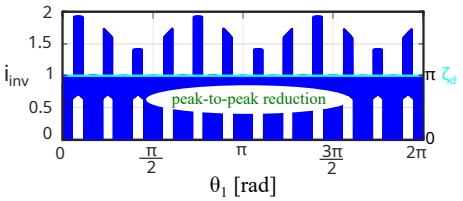
(**d**) Voltage references of the VSI of the ADTP for D-PWM1.



(**e**) Voltage references of the VSI of the ADTP for D-PWMMIN.



(**f**) Input current of the VSI and the instantaneous interleaving angle applying ζ_d for D-PWM1.



(**g**) Input current of the VSI and the instantaneous interleaving angle applying ζ_d for D-PWMMIN.

Figure 14. Dynamic interleaving method proposed in [63] for D-PWM1 and D-PWMMIN.

As a counterpart, this dynamic interleaving scheme (ζ_d) has some disadvantages compared to the constant interleaving (ζ_c); i.e., more computational resources are needed

in order to detect the voltage reference clampings between two nearby phases in the phasor diagram; in addition, it is only applicable for discontinuous PWM techniques.

4.3. Optimal Interleaving Scheme for any DZSI-PWM: ζ_{opt}

The optimal interleaving scheme (ζ_{opt}) can be defined as the one which minimizes $I_{cap,rms}$ over the entire linear region, $0 \leqslant M \leqslant 1$. In the case of continuous techniques, $\zeta_{opt} = \zeta_c$ because a dynamic interleaving scheme cannot be used. Therefore, the optimal interleaving angle can be considered $\zeta_c = \pi/2$ rad.

In the case of the D-PWMMIN and D-PWMMAX techniques, it is a bit more complex. First, it is worth remembering that as the dynamic interleaving is applied continuously, it is the same as applying a constant interleaving of $\zeta_c = \pi$ rad. In addition, following the numerical analysis described in Section 4.1 and as Figure 15 shows, $\zeta = \pi$ rad minimizes $I_{cap,rms}$ for $0 \leqslant M \leqslant 1$. However, for higher modulation indexes, the interleaving angle becomes smaller. This happens because in this range of M, although the $(1,0)$ harmonic is not completely cancelled, the harmonics that have great influence on the rms value of the current, such as $(1,0)$ and $(2,0)$, are considerably attenuated.

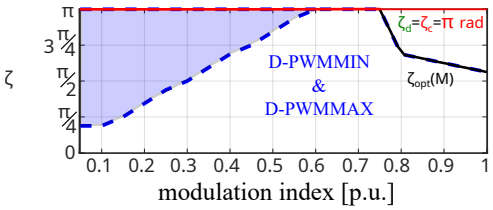


Figure 15. Constant and optimal interleaving angles for the whole linear range for D-PWMMIN and D-PWMMAX.

Finally, for the rest of discontinuous techniques (D-PWM0, D-PWM1, D-PWM2 and D-PWM3), the optimal interleaving scheme consists of comparing both interleaving algorithms and selecting the one which gives the smallest $I_{cap,rms}$ for each modulation index.

Therefore, the implementation of this optimal interleaving scheme is performed following the indications in Figure 16. The next section will show the results obtained for all the interleaving schemes.

DZSI-PWMs		Modulation index (M)				
		0-0.30	0.30-0.80	0.80-0.85	0.85-0.95	0.95-1
Continuous	SPWM	$\pi/2$				
	MINMAX-PWM					
	THI-PWM					
Discontinuous	D-PWMMIN	π or ζ_d		ζ as a function of M (Figure 15)		
	D-PWMMAX					
	D-PWM0	$\pi/2$ or ζ_d	ζ_d			$\pi/2$
	D-PWM1		ζ_d			
	D-PWM2		ζ_d			$\pi/2$
	D-PWM3		ζ_d		$\pi/2$	

Figure 16. Optimal interleaving scheme as a function of the selected DZSI-PWM technique and M for $\cos\phi = 1$.

5. Influence of Interleaving for DZSI-PWM Techniques on the Current Ripple and Voltage in the DC-Link Capacitor

The influence of DZSI-PWM techniques on $I_{cap,rms}$ and $\Delta v_{pp,max}$ has been identified through the interleaving schemes described in Section 4 as a function of M and for $\cos\phi = 1$ by using the methodology described in Figure 3.

In contrast to three-phase VSIs, where the rms current through the DC-Link capacitor is independent of the chosen PWM technique [67], in the ADTP with double zero sequence injection technique it is strongly dependent on it. This happens due to the 30° shifting between the two three-phase inverters forming the ADTP. The rms value of the input

current of either the first inverter or the second inverter do not depend on the modulation technique but their sum does:

$$I_{inv,rms} \neq I_{inv1,rms} + I_{inv2,rms}. \tag{34}$$

In general terms, in EV applications, the DC-Link capacitor is selected mainly considering the ripple current through the capacitor. As there are no low-frequency harmonic components as in single-phase converters, the voltage ripple is lower for a multiphase application with the same power rating. For this reason, the optimal interleaving angle must be selected based on the current profile and not on the basis of the voltage ripple. However, in any case, it is also interesting to analyse whether this optimal interleaving scheme which minimizes $I_{cap,rms}$ also reduces $\Delta v_{pp,max}$. The $I_{cap,rms}$ results shown in the following section were obtained by using the double Fourier integral analysis of Section 2 and the results that correspond to $\Delta v_{pp,max}$ were obtained by a numerical analysis in Matlab–Simulink. Finally, in Section 5.3 $I_{cap,rms}$ is simulated for EV dynamic conditions applying the WLTP driving cycle.

5.1. RMS Value of the Current Through DC-Link Capacitor at Static Operating Points

Figure 17 shows the rms current curves for the different DZSI-PWM techniques. Here, it can be observed that without using interleaving algorithm (in blue) D-PWM1, D-PWM0, D-PWM2, and D-PWM3 present the lowest $I_{cap,rms}$ (in that order) and continuous techniques, as well as D-PWMMIN and D-PWMMAX have the highest values of $I_{cap,rms}$. Although the differences between these two main PWM groups are bigger for central values of M ($0.4 < M < 0.7$), when M gets close to 1 ($M > 0.9$), all analysed PWM techniques tend to equalise. These continuous PWM techniques, as well as D-PWMMIN and D-PWMMAX, present a maximum value at $M \approx 0.6$.

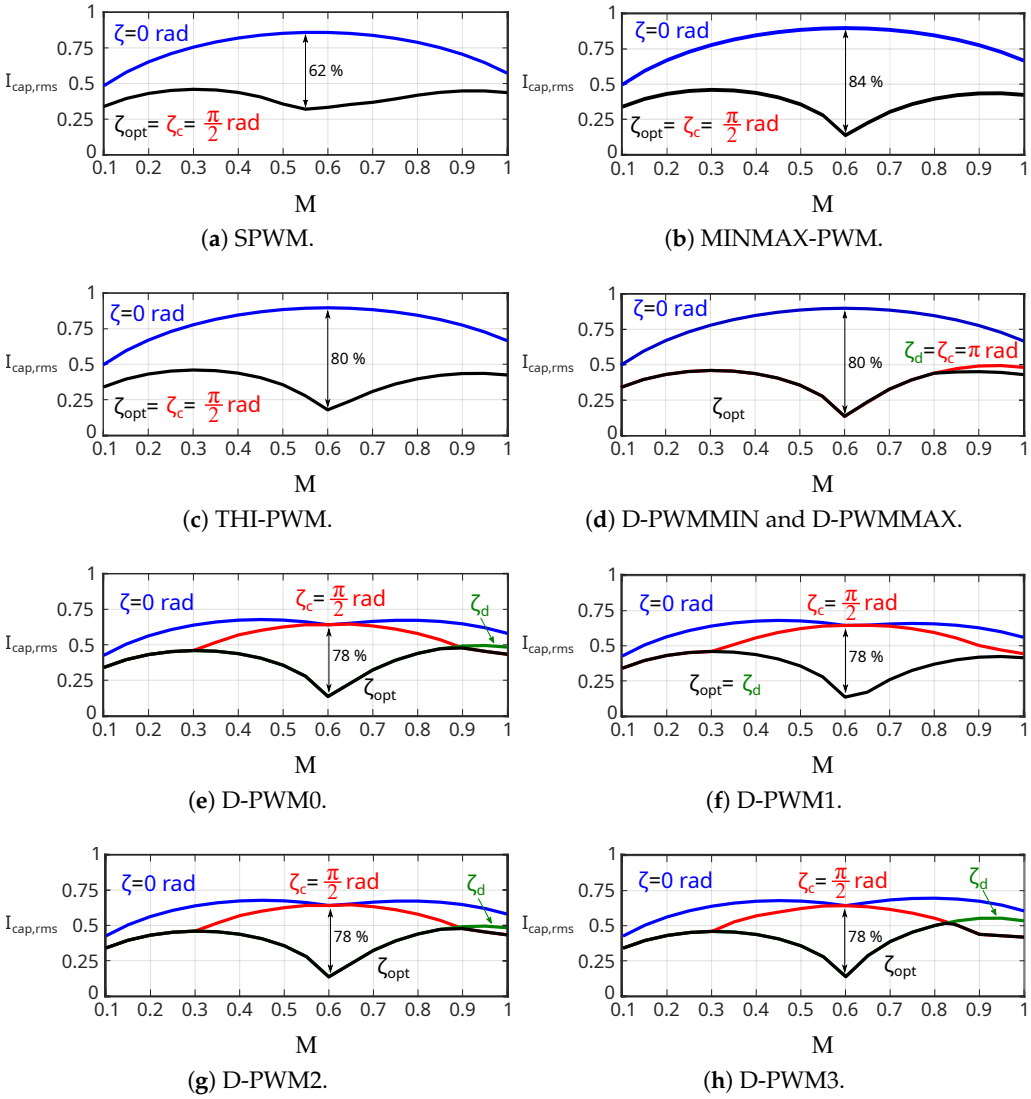
When the proposed optimal interleaving scheme is applied (Figure 17, in black), continuous modulations with $\zeta_{opt} = \pi/2$ rad reduce $I_{cap,rms}$ of up to 62% for SPWM, 84% for MINMAX-PWM and 80% for THI-PWM. For discontinuous modulations, reductions up to 80% for D-PWMMIN and D-PWMMAX and 78% for D-PWM0, D-PWM1, D-PWM2 and D-PWM3 are obtained. D-PWM1 and MINMAX-PWM provides the lowest values of $I_{cap,rms}$ (in that order).

5.2. Voltage Ripple in the DC-Link Capacitor at Static Operating Points

Even though the main idea of the interleaving approach is to reduce the rms value of the current through the DC-Link capacitor, Figure 18 shows that it also reduces the DC-Link voltage ripple ($\Delta v_{cap,max}$) for all DZSI-PWMs.

Unlike the rms value of the current through the DC-Link capacitor, when no interleaving ($\zeta = 0$ rad) is applied, continuous PWM techniques (MINMAX-PWM, THI-PWM and SPWM, in that order) present the lowest $\Delta v_{pp,max}$, and discontinuous techniques present the highest values of $\Delta v_{cap,max}$ (Figure 18). Specifically, MINMAX-PWM provides the smallest and D-PWM0 provides the highest voltage ripple among these noninterleaved DZSI-PWM techniques.

When the proposed optimal interleaving scheme ($\zeta = \zeta_{opt}$) is applied, the following maximum reductions of $\Delta v_{pp,max}$ are obtained: up to 64% for SPWM, 86% for MINMAX-PWM, 85% for THI-PWM, 90% for D-PWMMIN and D-PWMMAX, 88% for D-PWM0, 90% for D-PWM1, 90% for D-PWM2, and 91% for D-PWM3. The DZSI-PWM technique which presents the smallest $\Delta v_{pp,max}$ once the optimal interleaving scheme is applied is MINMAX-PWM.



(**a**) SPWM. (**b**) MINMAX-PWM.

(**c**) THI-PWM. (**d**) D-PWMMIN and D-PWMMAX.

(**e**) D-PWM0. (**f**) D-PWM1.

(**g**) D-PWM2. (**h**) D-PWM3.

Figure 17. Normalized DC-Link rms current for DZSI-PWM techniques as a function of *M*.

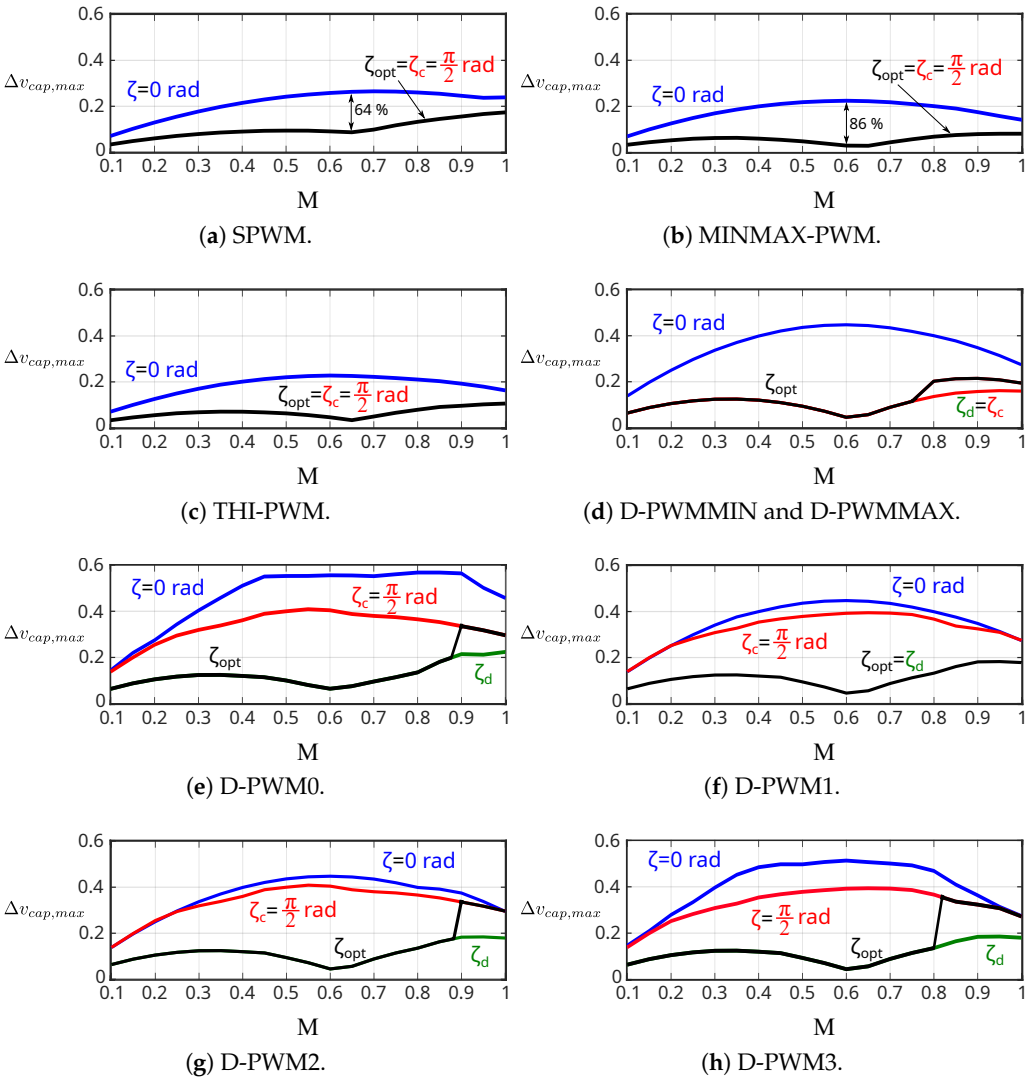
As has been seen in this section, the combination of the optimal interleaving scheme and DZSI-PWM techniques is a good alternative in order to reduce the stress variables on the DC-Link capacitors of the ADTP power converters for electric vehicles. However, it is enough to apply a constant interleaving scheme (ζ_c) in order to reduce the current stress on the DC-Link capacitor considerably.

5.3. RMS Value of the Current through DC-Link Capacitor during Standardized Driving Cycles

Figure 19 shows the block diagram of the ADTP platform and the simulation model used to obtain the results during EV dynamic conditions. The vehicle battery has been modelled as a 400 V DC source according to the typical values of electric vehicles [43]. The selected DC-Link capacitance has been 600 µF. The motor that has been modelled is the one indicated in Table 1 (Section 3.1). A maximum motor current of 25 A has been set and the base mechanical speed of the motor has been changed to 2400 rpm. Lastly, the control algorithm used is explained in detail in [79] and the switching frequency of the power devices has been set to 25 kHz.

Matlab–Simulink has been used to execute the simulation models, and they have been embedded on an OPAL-RT OP4510 high-performance, real-time platform, which has accelerated the simulation time considerably. The simulation step has been set to 1 µs. In addition, in order to visualize in a more didactic way and compare of the results with

and without interleaving, the results have been postprocessed with a moving average of 2000 samples.



(**a**) SPWM. (**b**) MINMAX-PWM.

(**c**) THI-PWM. (**d**) D-PWMMIN and D-PWMMAX.

(**e**) D-PWM0. (**f**) D-PWM1.

(**g**) D-PWM2. (**h**) D-PWM3.

Figure 18. Normalized maximum switching voltage ripple within one period of the fundamental.

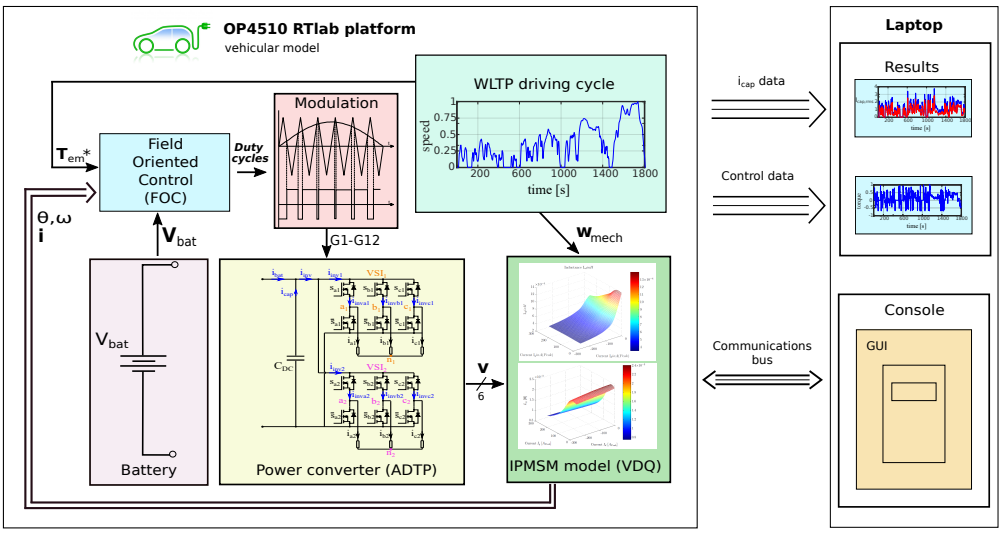
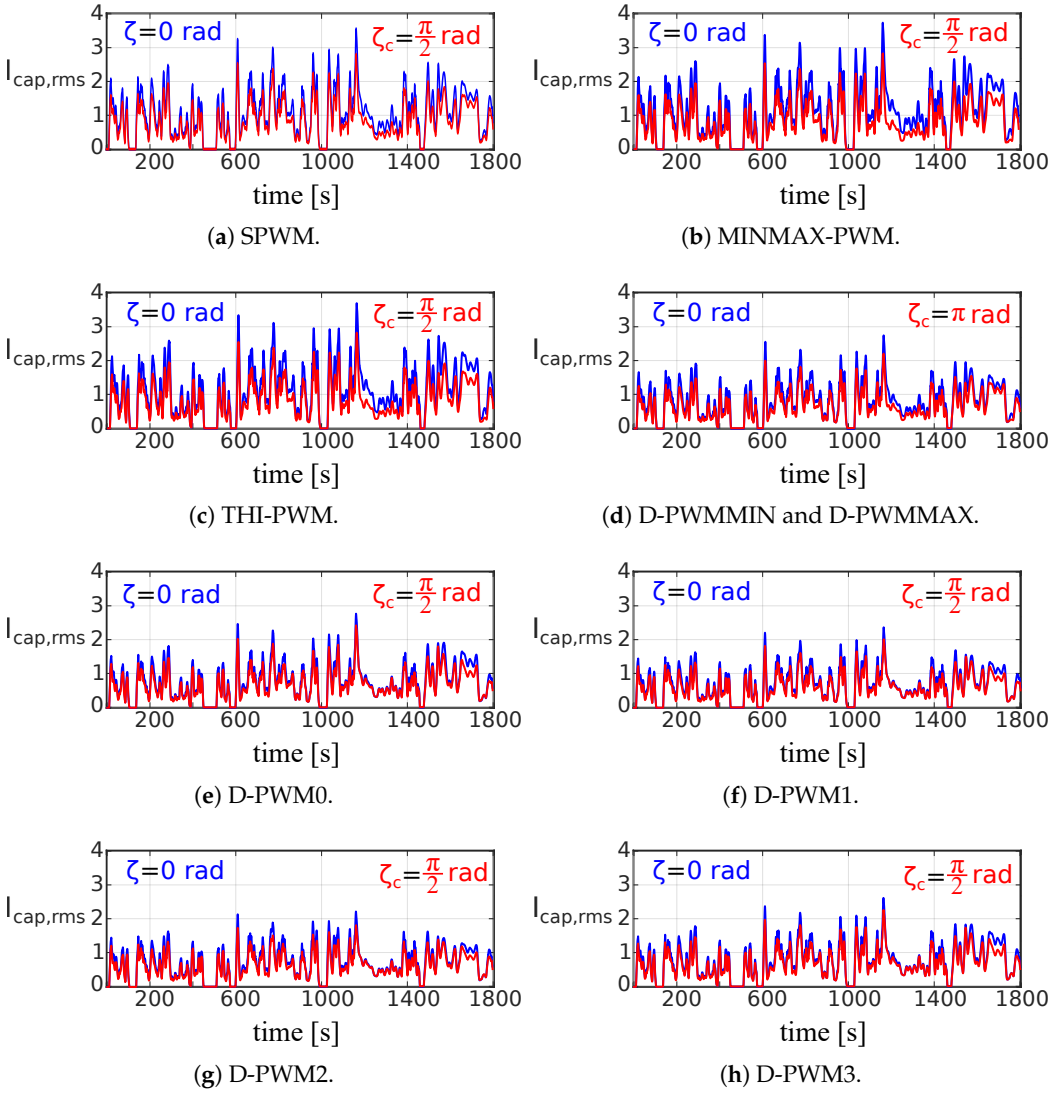


Figure 19. RTlab OP4510 simulation platform diagram for electric vehicle ADTP propulsion systems.

Figure 20 shows the results of $I_{cap,rms}$ in the whole WLTP driving cycle, with and without constant interleaving angle for each DZSI-PWM technique ($\zeta_c = \pi/2$ rad for the techniques SPWM, MINMAX-PWM, THI-PWM, D-PWM0, D-PWM1, D-PWM2, D-PWM3; and $\zeta_c = \pi$ rad for D-PWMIN and D-PWMMAX). Here, it can be observed that all the analysed PWM techniques reduce $I_{cap,rms}$ when the interleaving scheme is applied. Likewise, Table 3 shows the mean value of the rms current throughout the entire WLTP driving cycle. These results confirm that an adequate constant interleaving scheme reduces the current stress on the DC-Link capacitor considerably. These simulations show that reductions up to 26% can be achieved. The largest reductions are provided by continuous PWM techniques, and the lowest values of $I_{cap,rms}$ are found for discontinuous PWM techniques. However, these D-PWMs are not so often used in EV application because they worsen the quality of the output voltage waveform.



(**a**) SPWM. (**b**) MINMAX-PWM.

(**c**) THI-PWM. (**d**) D-PWMMIN and D-PWMMAX.

(**e**) D-PWM0. (**f**) D-PWM1.

(**g**) D-PWM2. (**h**) D-PWM3.

Figure 20. DC-Link RMS current for DZSI-PWM techniques in WLTP driving cycle with (in red) and without (in blue) constant interleaving schemes.

Table 3. DC-Link rms current ($I_{cap,rms}$) for noninterleaved DZSI-PWM techniques and using the correspondent constant interleaving angle ζ_c for the WLTP driving cycle.

	Noninterleaved (A)	Interleaved (A)	Reduction (%)
SPWM	1.06	0.82	22.94
MINMAX-PWM	1.13	0.82	27.48
THI-PWM	1.13	0.82	27.25
D-PWMMIN	0.82	0.64	21.23
D-PWMMAX	0.83	0.64	22.67
D-PWM0	0.78	0.65	16.01
D-PWM1	0.71	0.59	16.27
D-PWM2	0.72	0.61	16.01
D-PWM3	0.79	0.67	15.37

6. Conclusions

The ADTP has turned out to be one of the most successful multiphase arrangement in the short term for electric traction applications due to its intrinsic advantages, such as enhanced efficiency and fault-tolerant operation. In power converters in general, and therefore also in ADTP architecture, the DC-Link capacitor is a critical element that represents a considerable fraction of the volume and source of failures because it is responsible for up to a 40% of the total volume and 30% of the total failures in power electronic inverters.

This work focuses on the DC-Link stress reduction in order to benefit this capacitors by means of the following figures of merit: rms value of the ripple current through the DC-Link capacitor ($I_{cap,rms}$) and the maximum peak-to-peak voltage ripple ($\Delta v_{cap,max}$). For that purpose, the input current spectra of the ADTP arrangement have been analysed by using the double Fourier integral method for the DZSI-PWM techniques. Although each branch of the multiphase VSI presents certain input current harmonics, the interaction between the different branches inherent to the ADTP architecture cancels them out and changes the amplitude of some of these harmonics.

All these input current harmonics depend mainly on the selected DZSI-PWM technique, as well as on M and $\cos\phi$. For electric vehicle applications, the main vehicle standard driving cycles NEDC and WLTP using a PMSM demonstrate that the value of the power factor is $\cos\phi > 0.97$. Thus, the current spectra for these DZSI-PWM techniques have been obtained as a function of M and for $\cos\phi = 1$. Here, it has been observed that continuous PWM techniques (SPWM, MINMAX-PWM, and THI-PWM) have a predominant carrier wave harmonics at $2f_{sw}$; D-PWM0, D-PWM1, D-PWM2, and D-PWM3 have a wide sideband harmonic range around f_{sw}, even though their carrier wave harmonics at $2f_{sw}$ cannot be neglected; finally, D-PWMMIN and D-PWMMAX have their predominant current harmonics at f_{sw} and $2f_{sw}$.

Due to lack of in-depth research in the scientific literature about the interleaving schemes for this kind of ADTP arrangements, this work has analytically derived the relationship between the input current harmonic spectrum and the constant interleaving angle (ζ_c), as well as how this can be exploited in order to cancel certain dominant harmonics inherent to these DZSI-PWM techniques. As a result, the rms value of the ripple current through the DC-Link capacitor ($I_{cap,rms}$) and the maximum peak-to-peak voltage ripple ($\Delta v_{cap,max}$) has been reduced. This confirms that the elimination of the dominant input current harmonics is directly related to the minimization of $I_{cap,rms}$.

It has been concluded that for all continuous PWM techniques the optimal interleaving angle is $\zeta_c = \pi/2$ rad because it eliminates the dominant carrier harmonic at $2f_{sw}$. For discontinuous PWMs, a combination between the dynamic (only applicable for discontinuous PWM techniques) and the constant interleaving schemes is generally preferred. During the subinterval in which the constant interleaving scheme is applied, for D-PWM0, D-PWM1, D-PWM2, and D-PWM3 $\zeta_c = \pi/2$ rad is preferred because their $2f_{sw}$ carrier wave harmonic and $f_{sw} + 3f_1$ sideband harmonic are cancelled out. However, for D-PWMMIN

and D-PWMMAX, $\zeta_c \leqslant \pi$ rad is preferred because it eliminates or attenuates the f_{sw} dominant input current harmonic.

All the analysed PWM techniques have been shown to improve significantly their characteristics compared to conventional noninterleaved operation. In general, the major DC-Link stress reductions are obtained for continuous PWM techniques throughout the linear range with the same constant interleaving angle. More specifically, the largest reductions are obtained with MINMAX-PWM where $I_{cap,rms}$ is reduced up to 84% and $\Delta v_{cap,max}$ up to 86%.

These results favour continuous over discontinuous PWM techniques. These are the most widely used in electric vehicle propulsion systems. In addition, it must be considered that discontinuous modulation techniques have the intrinsic disadvantage of producing worse harmonic distortion in the load than continuous modulation techniques. Moreover, some of these techniques, such as D-PWM0 and D-PWM2, are mostly focused on more capacitive than inductive loads. All of these considerations lead the automotive industry to use continuous techniques. Finally, it can be said that the work carried out in this document allows the reader to identify the adequate interleaving angle both to reduce the stress of the DC-Link capacitor, and in general terms, to make electric vehicle propulsion systems more reliable.

Author Contributions: Conceptualization, A.D., E.R., U.U., I.M.d.A. and J.A.; methodology, A.D., E.R. and U.U.; software, A.D. and J.A.; validation, A.D., E.R, U.U., I.M.d.A. and J.A.; formal analysis, A.D and U.U.; investigation, A.D., E.R., U.U., I.M.d.A. and J.A.; resources, J.A. and I.M.d.A.; data curation, E.R. and U.U.; writing—original draft preparation, A.D., E.R., U.U., I.M.d.A. and J.A.; writing—review and editing, A.D., E.R., U.U., I.M.d.A. and J.A.; visualization, E.R.; supervision, U.U. and J.A.; project administration, I.M.d.A. and J.A.; funding acquisition, I.M.d.A. and J.A. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Government of the Basque Country within the fund for research groups of the Basque University system IT1440-22 and by the MCIN/AEI/10.13039/501100011033 within the project PID2020-115126RB-I00, as well as the support of the UPV/EHU pre-doctoral programme (PIF20-305).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: Applied Electronics Research Team (APERT) UPV/EHU.

Conflicts of Interest: Not applicable.

List of Abbreviations

The following abbreviations are used in this manuscript:

ADTP	Asymmetrical Dual Three-Phase
CB	Carrier-Based
C-PWM	Continuous PWM
DC	Direct Current
DOE	United States Department of Energy
D-PWM	Discontinuous PWM
DZSI	Double Zero Sequence Injection
ESR	Equivalent Series Resistance
EV	Electric Vehicle
HDF	Harmonic Distortion Factor
IPMSM	Interior Permanent Magnet Synchronous Motor
MINMAX-PWM	MIN-MAX PWM method
MTPA	Maximum Torque Per Ampere

MTPV	Maximum Torque Per Volt
NEDC	New European Driving Cycle
PM	Permanent Magnet
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse-Width Modulation
SPWM	Sinusoidal PWM
SPMSM	Surface-mounted Permanent Magnet Synchronous Motor
SV	Space Vector
THD	Total Harmonic Distortion
THI-PWM	Third Harmonic Injection PWM
UN ESCAP	United Nations' Economic and Social Commission for Asia and the Pacific
USCAR	The United States Council for Automotive Research
VSI	Voltage-Source Inverters
WBG	Wide BandGap
WLTP	Worldwide Harmonized Light vehicles Test Procedure

List of Symbols

The list of symbols with respective units, if applicable, used in this manuscript is the following:

A_{mn}, B_{mn}	Real and imaginary coefficients of a Double Fourier series expansion.
C_{mn}	Complex-valued Double Fourier coefficient, $C_{mn} = A_{mn} + jB_{mn}$.
$C_{mn}^{inv1a} \cdots C_{mn}^{inv2c}$	Complex-valued Double Fourier coefficients of $i_{inv1a} \cdots i_{inv2c}$ (A).
C_{DC}	DC-Link capacitance (F).
D	Duty cycle.
ESR	Equivalent Series Resistance of capacitor (Ω).
f_1	Fundamental frequency of modulating signal (Hz).
f_h	Harmonic frequency values, $f_h = nf_1 + mf_{sw}$ (Hz).
f_{sw}	Frequency of carrier signal (Hz).
g	Generic two-variable time-domain function, $g[x(t), y(t)]$.
i_d, i_q	Direct-, quadrature-axis currents of PMSM (A).
I_d, I_q	Steady-state values of i_d, i_q (A).
$i_{1a} \cdots i_{2c}$	Current flowing into loads $a \cdots c$ of each VSI (A).
$i_{inv1a} \cdots i_{inv2c}$	Current flowing into legs $a \cdots c$ of VSI1, VSI2 (A).
i_{inv1}, i_{inv2}	Total current flowing into each VSI1, VSI2 (A).
I_{bat}	Current coming from upstream DC source, $I_{bat} = I_{inv,avg}$ (A).
i_{cap}; $I_{cap,rms}$	Current flowing into capacitor, $i_{cap} = i_{inv,AC}$; its rms value (A).
i_{inv}; $i_{inv,AC}$	Total current flowing into both VSIs; its ripple component (A).
$I_{inv,avg}$; $I_{inv,rms}$	Average of i_{inv}; rms of $i_{inv,AC}$ (A).
$\hat{I}_{out}$	Amplitude of output phase currents (A).
$J_k(\cdot)$	Bessel function of the first kind and order k.
$K_0 \cdots K_3$	Parameters to tune the MTPA control strategy.
L_d, L_q	Direct-, quadrature-axis inductances of PMSM model (H).
M	Modulation index, $M = \hat{V}_1 / \frac{V_{DC}}{2}$.
N_p	Number of pole pairs of PMSM.
n, m	Baseband and carrier index variables, respectively.
R_S	Stator resistance of PMSM model (Ω).
T_1	Fundamental period, $T_1 = \frac{1}{f_1}$(s).
T_{em}	Electromagnetic torque produced by PMSM (Nm).
T_{max}	Maximum torque specification of the PMSM (Nm).
T_{sw}	Switching period, $T_{sw} = \frac{1}{f_{sw}}$ (s).
v_{0s}	Injected zero-sequence component.
v_{cr}	Carrier signal (triangle-shaped).
v^*	Modulating signal, $v^* = M \cos\theta_1$.
v^{**}	Modified modulating signal, $v^{**} = v^* + v_{0s}$.
v_d, v_q	Direct-, quadrature-axis voltages of PMSM (V).

V_d, V_q	Steady-state values of v_d, v_q (V).
$\hat{V}_1$	Peak value of phase-to-neutral voltage (V).
V_{DC}	DC-link voltage (V).
$x(t), y(t)$	Intermediate time-domain variables, $x(t) = \omega_{sw}t$, $y(t) = \omega_1 t$.
x_r, x_f	Integration limits for $x(t)$.
Δv_{cap}	Capacitor ripple voltage (V).
$\Delta v_{cap,max}$	Maximum $\Delta v_{cap,pp}$ over T_1 (V).
$\Delta v_{cap,pp}$	Peak-to-peak value of the DC-Link voltage ripple in T_{sw} (V).
ζ, ζ_c, ζ_d, ζ_{opt}	Interleaving angle: generic, constant, dynamic, optimal.
θ_1	Angular position of modulating signal, $\theta_1 = \omega_1 t$.
Φ_v, Φ_i	Partial phase lags given by V_q/V_d,I_q/I_r ratios (or equalling $\pi/2$).
ϕ	Lag with respect to θ_1 of current flowing into load 'a' of VSI1.
Ψ_{PM}	Permanent-magnet flux in PMSM model (Wb).
ω_1	Fundamental angular frequency of modulating signal (s^{-1}).
ω_e	Electrical speed of PMSM (s^{-1}).
ω_m	Mechanical speed of PMSM (s^{-1}).
ω_{sw}	Angular frequency of carrier signal (s^{-1}).

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