Analysis and modelling of IGBTs parallelization fundamentals

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***Abstract*— In some power electronic applications, with high current and voltage ranges, discrete devices are not enough unless parallelization techniques are employed. IGBTs are one of the most common and widespread power electronic semiconductors, to make a parallel design with them, either as a discrete devices, dies, individual cells or power modules, it is necessary to know their static and dynamic behaviour. Besides, operation temperature, device parameter tolerances, driver circuit and power layout, as well as different parasitic inductance also affect its performance. The objective of this article is to show and model how all the aforementioned parameters affect the behaviour and performance of a parallelized IGBT, and highlight the design keys for a successful parallelized design.**

***Index Terms*— Parallelization, IGBT, driver, layout, balance, parasitic inductance (L_σ), junction temperature (T_j), static and dynamic behaviour.**

I. Introduction

Nowadays, power electronics applications need high current and voltage ranges. These ranges are sometimes out of the operational maximum limits of both discrete devices and power modules. In order to solve this problem, parallel designs are used, e.g., AUIRGPS4067D1 IGBT discrete rates 600 V/160 A and FS800R07A2E3 IGBT rates 650 V/700 A. The power module drives four times more current because it is made of four parallel IGBTs.

The parallelization main aim is to increase current capacity, therefore, converter power capacity is also increased. To achieve this objective, current must be balanced, i.e., total current should be distributed equally for each parallelized device or module, as shown in figure 1. Nevertheless, there is always an imbalance between current levels of different branches, since there are many factors which interact between each other. Thus, figure 1 represents an ideal situation. To maintain the current imbalance as low as possible, it is required to identify its mayor causes, which are the following:

- Difference between the parameters which characterize each device or module to be parallelized ($V_{CE_{(sat)}}$, $t_{d_{off}}$, temperature coefficient, etc) [1]–[3].
- Driver circuit design, gate impedance behaviour (Z_g) is analysed, as well as various control strategies of common or separate gate [4]–[8].
- Power circuit layout design, parasitic inductance effects are studied, particularly, the effects of emitter inductance [8]–[10].
- Differences in thermal circuit of each semiconductor.

The impact over the current imbalance of each device of the aforementioned causes should be minimized to improve the parallelized converter performance. The present work analyses the main aspect of parallelization and provides simulation results, in Keysight ADS^{TM}, of performance in conduction and switching from on to off states and vice versa as a function of the driver design and the power layout.

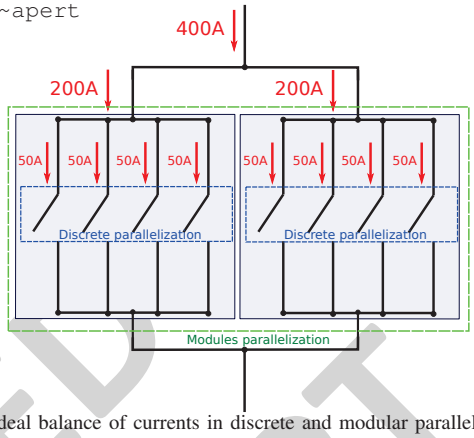


Fig. 1. Ideal balance of currents in discrete and modular parallelization.

II. Static behaviour

The static regime includes both conduction state and cut off state of semiconductor. The later is irrelevant for parallelization [1]. Thus, the main static parameters to be monitored are [2]:

- $V_{CE_{(sat)}}$, collector-emitter saturation voltage as a function of the junction temperature (T_j).
- $V_{GE_{(th)}}$, gate threshold voltage as a function of the junction temperature (T_j).
- V_{GE}, gate voltage.

The variation of the aformentioned parameters involves a current change (I_c) which flows through IGBT or module. If this variation is caused by a semiconductor temperature change, both current I_c and threshold voltage $V_{GE_{(th)}}$ are affected. It is going to be analysed the influence of T_j over threshold voltage $V_{GE_{(th)}}$ and saturation voltage $V_{CE_{(sat)}}$, as well as some design techniques to reduce current imbalance.

A. Temperature dependency on the semiconductor electrical parameters

$V_{CE_{(sat)}}$, V_{GE} and $V_{GE_{(th)}}$ and their temperature dependency are the key parameters to get a current balance between the parallelized devices in conduction state.

The expression (1) defines the dependency of the threshold voltage $V_{GE_{(th)}}$ on Fermi function (Φ_{FB}), which describes energy level and it is proportional to junction temperature (T_j) [2]:

$$V_{GE_{(th)}} = -V_{ms} - \frac{Q_{SS}}{C_{OX}} + 2\Phi_{FB} + \frac{\sqrt{2\varepsilon_0\varepsilon_{si}N_{A_{max}}(2\Phi_{FB})}}{C_{OX}}; \quad (1)$$

where V_{ms} is metal-semiconductor voltage, Q_{SS} extrinsic charge of energy states, C_{OX} gate oxide capacity, $\epsilon_0\varepsilon_{si}$ material

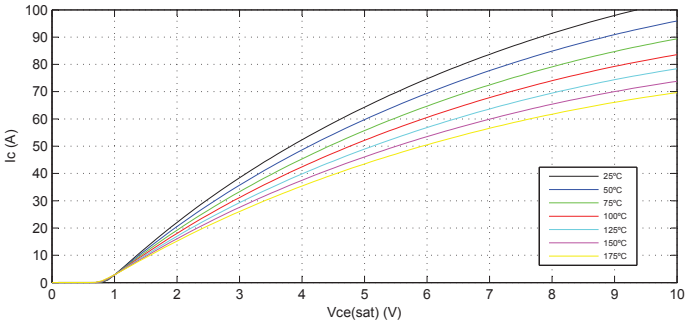


Fig. 2. Saturation voltage positive coefficient with $V_{GE} = 18\ V$.

permittivity and $N_{A_{max}}$ maximum concentration of carriers in the material. $V_{GE_{(th)}}$ decreases when T_j increases, i.e., the voltage has a negative coefficient with temperature [2].

On the other hand, collector-emitter saturation voltage ($V_{CE_{(sat)}}$) can be express as (2):

$$V_{CE_{(sat)}} = I_C \cdot R_{ch} = \frac{I_c \cdot l}{z\mu_{ns}C_{OX}(V_{GE} - V_{GE_{(th)}})}; \quad (2)$$

where R_{ch} is the channel resistance, l is the channel length, z the perpendicular channel width and μ_{ns} the carrier mobility in the channel. The parameter μ_{ns} decreases with T_j [2]. Considering that the voltage applied during turn on process (V_{GE}) is usually higher than gate threshold voltage $V_{GE_{(th)}}$, $V_{CE_{(sat)}}$ is a function with increasing behaviour with T_j.

Parallelization requires a voltage $V_{CE_{(sat)}}$ positive temperature coefficient (such as NPT, FS and trench FS IGBT devices), since the shared current is better balanced, thus there is an homogeneous temperature on parallel devices [11]. This static behaviour is modelled in figure 2 for the commercial device AUIRGPS4067D1 IGBT.

B. Current balance in conduction state

In order to balance the parallelized IGBTs of a power converter, it is necessary that the characteristic curve of all IGBTs were, approximately, the same current. Bearing in mind that $V_{CE_{(sat)}}$ vs I_c depends on the device temperature T_j.

When performing parallelization, unless all devices have the same voltage $V_{CE_{(sat)}}$, to balance them it is necessary:

1) The output characteristic curve, $V_{CE_{(sat)}}$ vs I_c, of all devices must approximately the same over the whole temperature range and with a positive temperature coefficient. To accomplish this, the IGBTs must belong to the same manufacturer, model and batch (same code bar). However, unless date and batch requirements can be satisfied, manufacturers don't guarantee that IGBT dies are from the same wafer. In any case, the characteristic curve is going to be almost equal and have the same temperature behaviour.
2) The devices which constitutes a parallelized set must have the same thermal behaviour, or be as close as possible. To achieve this, the thermal difference between IGBTs devices must be almost null in all temperature ranges (3) [3], [12].

$$|\Delta T_{j_{xy}}| \simeq 0^{o}C; \quad (3)$$

Therefore, the design of the thermal cooling circuit must provide the same thermal resistance and transient thermal impedances, so that the heat is distributed homogeneously.

If these two requirements are satisfied, parallel devices temperature will be similar, consequently, it will be possible to employ the same characteristic curve for all the parallel devices, and the current imbalance will be closed to nil (4) [3], [13].

$$|\Delta I_{c_{xy}}| \simeq 0\ V; \quad (4)$$

E.g., figure 3 presents different cases of current balance and imbalance according to aforementioned conditions. Figures 3(a) and 3(b) show that a great difference between characteristic curves creates big current difference between devices, regardless of temperature. On the other hand, figures 3(c) and 3(d) show that the current imbalance can be very high with a possible fail of the hottest IGBT if both devices work at different temperature (devices with same characteristic curve at different temperature).

III. Dynamic behaviour

During IGBTs switching, different effects can produce current imbalances. This imbalance is important, since switching frequencies are higher. The dynamic parameters to be considered are [2], [14]:

- $t_{d_{(on)}}$, turn on delay: from V_{GE} 10% to I_c 10%.
- t_r, rise delay: from 10% to 90% of I_c.
- $t_{d_{(off)}}$, turn off delay: from V_{GE} 90% to I_c 90%.
- t_f, fall delay: from 90% to 10% of I_c.

The temperature variation results in delay time variation, what produces a switching losses variation. At the same time, these losses variations change device junction temperature. Consequently, the operating point and current device are also modified, which cause an imbalance.

A. Temperature dependency on switching time

During switching processes the temperature variations produce, mainly, differences in IGBTs activation threshold voltage ($V_{GE_{(th)}}$) that influences the turn on ($t_{d_{(on)}}$) and turn off ($t_{d_{(off)}}$) delays. These delays affects parallel IGBTs current balance in transient states [1]:

$$t_{d_{(on)}} = -\tau_1 \cdot ln(1 - \frac{V_{GE_{(th)}}}{V_{GE}}); \quad (5)$$

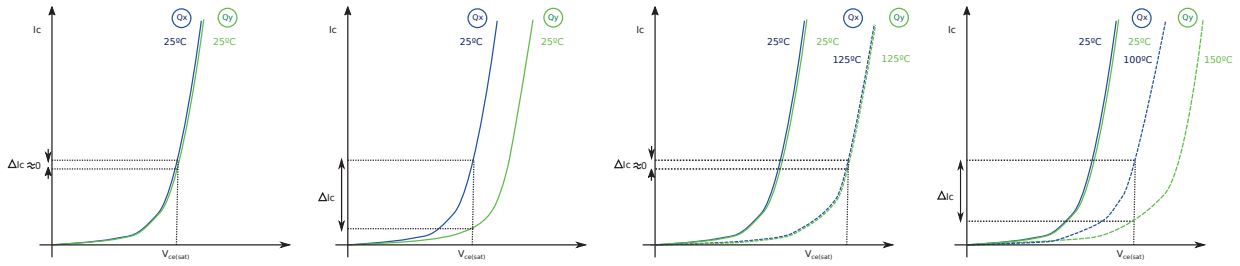
where time constant τ_1 is:

$$\tau_1 = R_G(C_{GE} + C_{GC}); \quad (6)$$

Equations (5) and (6) show that $t_{d_{(on)}}$, and similarly $t_{d_{(off)}}$, increases with T_j [2]. This temperature effect over switching transients is represented in the simulation example of automotive IGBT AUIRGPS4067D1 (figures 4(a) and 4(b)).

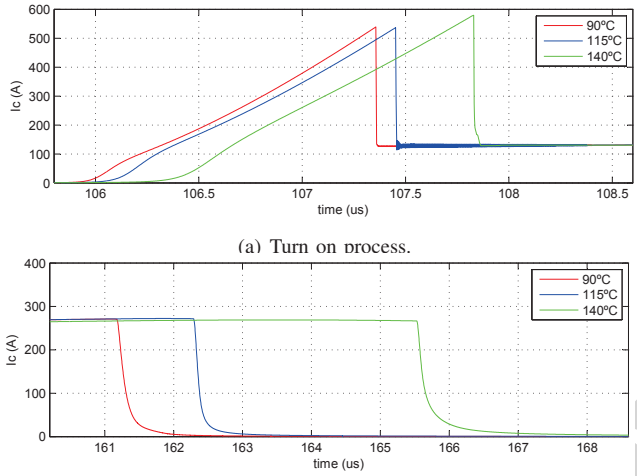
B. Current balance during switching

It is necessary to remove the factors which generate thermal imbalances to reduce temperature difference $\Delta T_{j_{xy}}$ during turn off. A way to reduce this variation is through layout [15] and thermal design. Considering that the parameters $t_{d_{(on)}}$ and $t_{d_{(off)}}$ increase with T_j, if parallel IGBTs work at different temperature, a current imbalance can be produced due to delay differences [2].



(a) Same characteristic curve. (b) Different characteristic curve. (c) Same temperature. (d) Different temperature.

Fig. 3. ΔI_c between two IGBTs according their characteristic curve and T_j.



(a) Turn on process.

(b) Turn off process.

Fig. 4. Switching behaviour with temperature variation.

IV. Control Circuit: Driver

Driver circuit gate design directly influences current balancing. Driver gate design must be symmetrical to avoid non-homogeneous switching that leads to current imbalance. Symmetrical design is done controlling gate resistance values (R_g), parasitic inductances ($L_{\sigma g}$) and gate voltage (V_{GE}), parameters that constitute driver output impedance (Z_g) (figure 5) [4].

A. Gate impedance

Both turn on process and conduction state are affected by PCB characteristics between driver and IGBT gate, thus it must be taken into account track length effects between driver and power semiconductors. In case of an asymmetrical design, the current imbalance increases, particularly during turn off, since delays responsible for current variations occurs, which increase losses [5].

Some references [6]–[8] recommend to connect IGBT gates to a resistance in order to reduce imbalances, and these resistances have to be connected to driver signal.

In [16] is described current imbalance consequences due to gate impedance variation that highlight the importance of the connection between driver and gate. A simulation of four parallel IGBTs are used to verified the aforementioned possible asymmetrical effects (figure 6(a)):

1) The use of gate resistances between IGBTs and driver can reduce the deviations between each IGBT to be parallelized. Gate voltage can be determined in each IGBT controlling resistance and parasitic gate values [16].

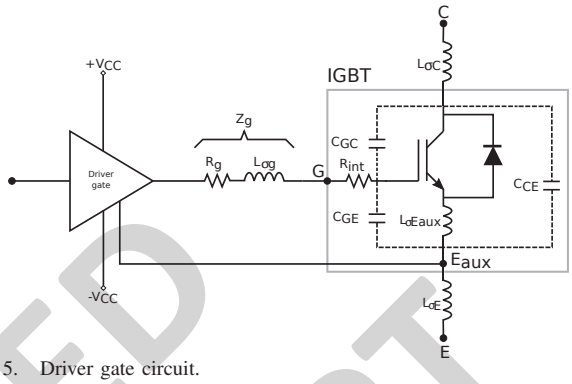


Fig. 5. Driver gate circuit.

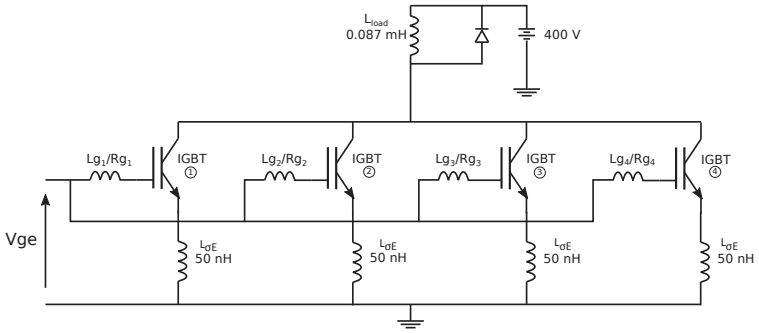
2) After analysis and simulate natural asymmetries which present AUIRGPS4067D1 IGBTs (with internal field stop architecture) to be parallelized, artificial elements are introduced:

- Symmetric gate resistances: the turn on and off behaviours are affected by small variations in control circuit. These variations are originated on internal resistances ($R_{G,int}$) and gate resistances (R_G) [16]. The different on and off gate voltage slopes produce dynamic imbalances (figure 6(b)) because of different voltage gate levels and delays.
- Gate resistance and inductance variation: in order to check asymmetric effects in IGBT ④ (with the higher current imbalance) gate resistance and inductance are changed and results are shown in figures 6(c) and 6(d) [16]. The figure 6(c) shows that a lower gate resistance produces a faster di_c/dt, so a higher current peak. However, the asymmetric effect is very smooth. In the figure 6(d) can be perceived that increasing gate parasitic inductance also produces a light deviation from the original test conditions [16]. Finally, figure 6(e) shows that combined effect of gate resistance and inductance variation ($R_g = 2.2\ \Omega$ and $L_g = 20\ nH$) has higher current imbalance than the others IGBTs.

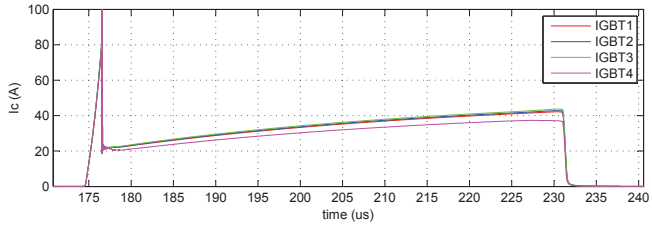
B. Gate design

The design must be as symmetrical as posible, but in several conditions, it is difficult to make full symmetrical designs due to physic restrictions of the circuit [11]. To implement the connection to the IGBT gate, there are two design strategies:

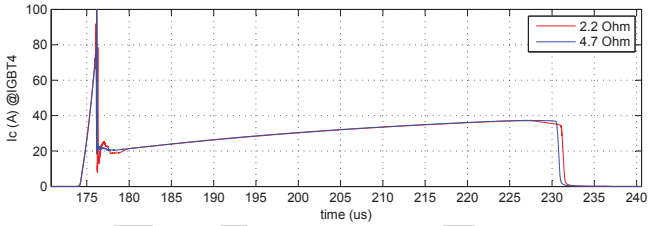
- A common gate connection for all IGBTs: this strategy substantially reduces different delays and voltage levels problems, because they have a significant impact on dynamic characteristic of IGBT devices [9]. However, the coupling between power part and control signals need to



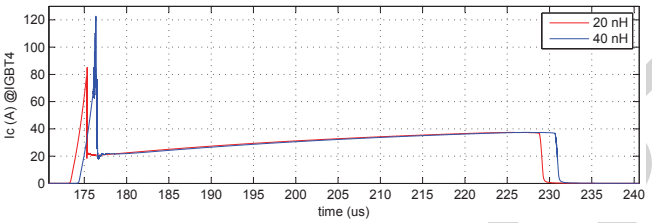
(a) Circuit with asymmetries for simulation.



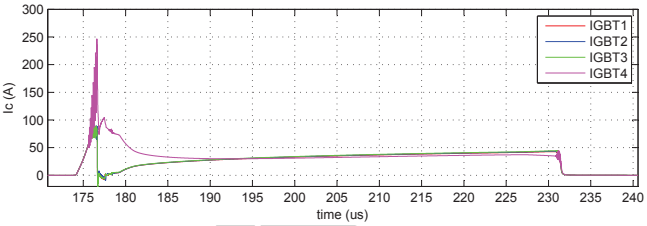
(b) Natural asymmetries in each IGBT.



(c) IGBT ④ gate resistance variation.



(d) IGBT ④ gate inductnace variation.



(e) Imbalance due to gate resistance and inductance.

Fig. 6. Asymmetries effects produce by gate connection on the current.

be optimized to avoid internal coupling problems between driver and power circuit [11].

- Separate gate connection for each IGBT: this technique allows to avoid coupling effects in parallel devices. However, conduction voltage levels have to be similar to prevent switching problems, since V_{CE} affects delays and operation point. For this reason, gate signal tracks, which connect each IGBT, has to be equal in all devices to avoid synchronization problems [11].

Therefore, the case of common driver gate has less energy mismatches than the case of separate driver gate [17]. This is due to gate signal time is determined by gate impedance connection.

V. Power Circuit: Layout

All circuits, both driver and layout power part, with parallel connections must be designed with minimum parasitic inductances and as symmetric as possible. Even bus DC tracks of power layout must have symmetry [7]. In order to achieve a symmetrical power layout, it is necessary:

- The impedance in connections between each die or discrete semiconductor has to be identical to allow conduction and switching of current without disturbances.
- The current which flows through parallel devices should not influence in the impedance of the adjacent device [11].
- Loop inductance values and layout symmetric design have to be equal in all power circuitry.
- Parallel IGBTs must be as close as possible between them to reduce parasitic inductances [9].
- Temperature variations have to be minmized to avoid current imbalances [10].
- Internal emitter inductance effects ($L_{E\sigma_{aux}} \simeq 5-10\ nH$), and emitter inductance ($L_{\sigma E} \simeq 20-50\ H$) must be analysed to obtain a low value of total parasitic inductance (L_σ).

The following sections provide a global view about parasitic inductances in the power circuit.

A. Parasitic inductances

All aspects of layout design such as DC capacitor design, DC bus, mechanic connection and power module have an important influence in parasitic impedance (Z_σ) of parallel IGBTs, especially the inductive component (L_σ). The figure 7 shows parasitic inductances in switching circuit for the specific case of a half bridge with two parallel IGBTs [4]. If parasitic inductance values are different, asymmetries will be generated during IGBT switching, so current imbalances will appear.

The total parasitic inductance (L_σ) should be considered to make a balanced design. This parasitic inductance (9) can be expressed as the sum of external circuit inductances, connections (7) and internal parasitic inductances of each IGBT (8):

$$L_{\sigma_{ext}} = \sum_n (L_{\sigma C} + L_{\sigma E}); \tag{7}$$

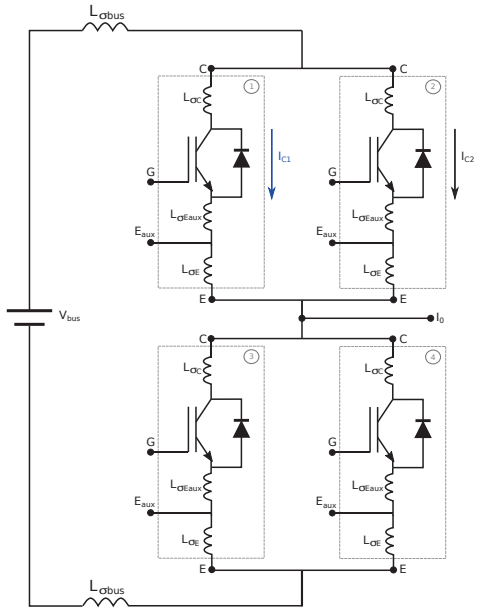


Fig. 7. Switching circuit with parasitic inductances.

$$L_{\sigma_{int}} = \sum_{n} L_{\sigma E_{aux\sigma}}; \tag{8}$$

$$L_{\sigma} = L_{\sigma_{ext}} + L_{\sigma_{int}} \tag{9}$$

In the case of custom design, using discrete devices or dies, all inductance values can be controlled with the exception of internal inductance ($L_{\sigma E_{aux}}$) which has each IGBT [7]. The following points explain the most important effects of parasitic inductances to get a balance current in the switching circuit (figure 7) [7]:

- Bus DC inductance ($L_{\sigma bus}$): the control of this inductance is fundamental and it must have the value as lower as possible. This is applied to both bus capacitor connection and connection between DC bus and power module. Laminated system adapted to converter layout is one technique that allows to get low values of inductance [7].
- Emitter inductance ($L_{\sigma E}$): this inductance affect both power circuit and driver (20 - 50 nH). Due to a faster di_c/dt of current, it induces a voltage which is added or subtracted in V_{GE} producing a feedback effect in the driver.

Because of the importance of emitter inductance the next sections are going to analyse the behaviour of auxiliary and external emitter parasitic inductances.

B. Auxiliary emitter parasitic inductance ($L_{\sigma E_{aux}}$)

The internal emitter inductance combined with IGBTs capacitances and driver circuit generate a close loop which can produce hard oscillations in IGBTs. The fast changes in emitter current during switching may induce a voltage through $L_{\sigma E_{aux}}$ which influences gate charging process (negative feedback) or discharging process (positive feedback), being critical for dynamic current distribution. As long as inductive $L_{\sigma E_{aux}}$ value cannot be modified, the way to improve the symmetry is with external emitter inductance ($L_{\sigma E}$), because switching speed can be balanced. Different values of $L_{\sigma E}$ affects turn off process, since it produces variation of switching losses [7]. Several examples of feedback are simulated in the figure 8:

1) Positive asymmetric feedback (figures 8(a) and 8(e)): they show different positive feedback levels, producing that IGBT ③ has faster turn on than IGBT ①:
$$V_{GE_3} = V_{GE} + 2 \cdot V_L > V_{GE_1} = V_{GE} \tag{10}$$

2) Positive and negative asymmetric feedback (figures 8(b) and 8(f)): results show how IGBT ② has a positive feedback, while IGBT ③ has a negative feedback (11).
$$V_{GE_2} = V_{GE} + V_L > V_{GE} > V_{GE_3} = V_{GE} - V_L \tag{11}$$

3) Negative asymmetric feedback (figures8(c) and 8(g)): different levels of negative feedback are produced, causing that IGBT ③ is turned on slower than IGBT ① (12).
$$V_{GE_3} = V_{GE} - 2 \cdot V_L < V_{GE_1} = V_{GE} \tag{12}$$

4) Negative symmetric feedback (figures 8(d) and 8(h)): each IGBT has approximately the same negative feedback, allowing synchronous switching of each IGBT (13).
$$V_{GE_1} = V_{GE_2} = V_{GE_3} = V_{GE} - V_L \tag{13}$$

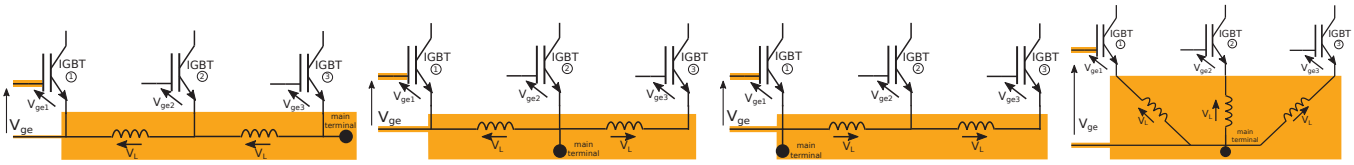
C. Emitter parasitic inductance ($L_{\sigma E}$)

Switching inductance circuit (L_{σ}) affects power semiconductors turning on and off (switching overvoltage). If switching circuits have different tracks, parallel IGBTs switching speed can be different between each device, producing a dynamic asymmetry which can a have higher impact than any current imbalance due to devices with unequal parameters. Although IGBTs have equal L_{σ} inductances, any small difference between emitter inductances $L_{\sigma E}$ can produce an unequal current distribution, thus an asymmetric switching losses and even some oscillations in the IGBTs [7].

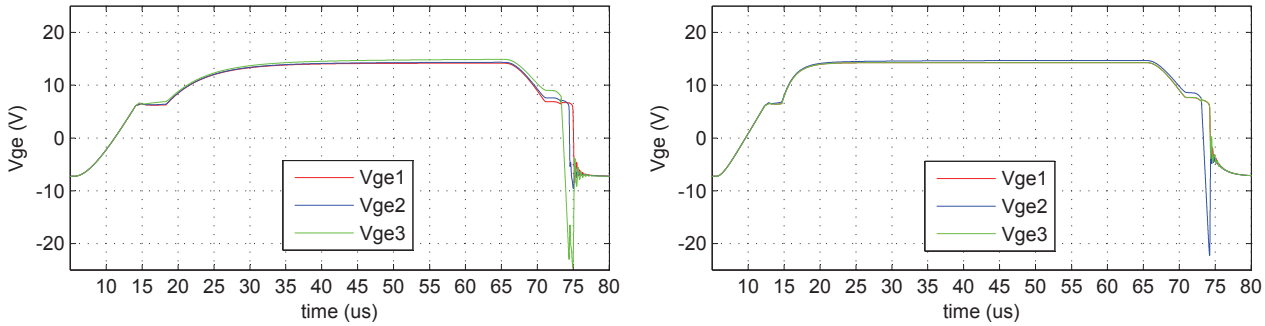
In the example of two symmetrical parallel modules [8], in which both total inductance value and resistance are equivalent, an imbalance can be produced (approximately 2%), because of different values of $L_{\sigma E}$. This imbalance is due to different internal parameters of each IGBT which has higher impact effect over the static current than to the dynamic current [8]. Therefore, this imbalance is acceptable because do not cause mayor drawbacks in the power layout design.

VI. Conclusions

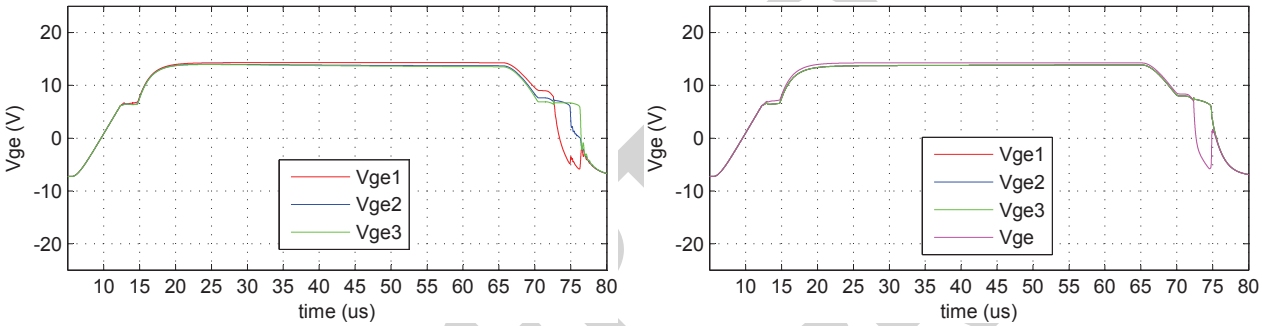
In order to achieve the parallelization, it is necessary to use devices or modules which present the same characteristic curve $V_{CE_{(sat)}}$ vs I_c, as well as a same $V_{GE_{(th)}}$, with temperature T_j. This way, it is possible to reduce temperature variation $|\Delta T_{xy}|$ between devices and also reduce static current imbalance. Moreover, devices delays, $t_{d_{(on)}}$ and $t_{d_{(on)}}$ temperature T_j dependent, must be as equal as possible between them to avoid current dynamic imbalances. For this reason, semiconductors or modules must belong to same batch, which guaranties similar internal parameters and temperature variation. In reference to driver circuit, it is advisable to use a common gate design in all



(a) Positive asymmetry. (b) Negative and positive asymmetry. (c) Negative asymmetries. (d) Negative symmetry.



(e) Positive asymmetry results. (f) Negative and positive asymetry results.



(g) Negative asymmetry results. (h) Negative symmetry results.

Fig. 8. Feedback examples between power circuit and driver.

parallel IGBTs to reduce delays and voltage level problems, and control resistance R_g and parasitic inductance $L_{\sigma g}$ values to get current I_c balance. Finally, the power layout requires minimize parasitic inductance effects, especially $L_{\sigma E_{aux}}$ and $L_{\sigma E}$, since it may produce some feedback effects which imbalance, and eventually, destroy the system. The simulation results show that the design must be as symmetric as possible to reduce imbalance effects.

VII. Acknowledgement

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